Product Overview

MC100LVEL38: 3.3 V ECL ÷·2, ÷·4/6 Clock Generator Chip

For complete documentation, see the data sheet.

The MC100LVEL38 is a low skew w 2, w 4/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended input signal.

The common enable (EN) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

The Phase_Out output will go HIGH for one clock cycle whenever the w 2 and the w 4/6 outputs are both transitioning from a LOW to a HIGH. This output allows for clock synchronization within the system.

Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple LVEL38s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one LVEL38, the MR pin need not be exercised as the internal divider design ensures synchronization between the w 2 and the w 4/6 outputs of a single device.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 5F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

Features

- 50 ps Maximum Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC} = 3.0 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = -3.0 V to -3.8 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34

For more features, see the data sheet

Part Electrical Specifications

Product	Compliance	Status	Type	Input Level	Output Level	V_{CC} Typ (V)	f_{Max} Typ (MHz)	t_{pd} Typ (ns)	t_R & t_F Max (ps)	Package Type
MC100LVEL38DWG	Pb-free Halide free	Active	Divider	HSTL ECL	ECL	3.3	1200	0.95	550	SOIC-20W
MC100LVEL38DWR2G	Pb-free Halide free	Active	Divider	ECL HSTL	ECL	3.3	1200	0.95	550	SOIC-20W

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Created on: 6/17/2019