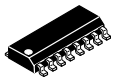
Programmable 3-PLL Clock Generator IC

FS6377



SOIC−16
CASE 751BA

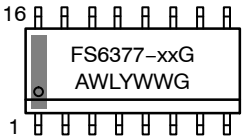
General Description

The FS6377 is a CMOS clock generator IC designed to minimize cost and component count in a variety of electronic systems. Three I^2C−programmable phase locked loops (PLLs) feeding four programmable muxes and post dividers provide a high degree of flexibility.

Features

- Three On−Chip PLLs with Programmable Reference and Feedback Dividers
- Four Independently Programmable Muxes and Post Dividers
- I^2C−Bus Serial Interface
- Programmable Power−Down of All PLLs and Output Clock Drivers
- One PLL and Two Mux/Post−Divider Combinations can be Modified by SEL_CD Input
- Tristate Outputs for Board Testing
- 5 V to 3.3 V Operation
- Accepts 5 MHz to 27 MHz Crystal Resonators
- Commercial and Industrial Temperature Ranges Offered
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MARKING DIAGRAM



xx = 01 or 01i
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
FS6377−01G−XTD	SOIC−16 (Pb-Free)	48 Units / Tube
FS6377−01G−XTP	SOIC−16 (Pb-Free)	3000 / Tape & Reel
FS6377−01iG−XTD	SOIC−16 (Pb-Free)	48 Units / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

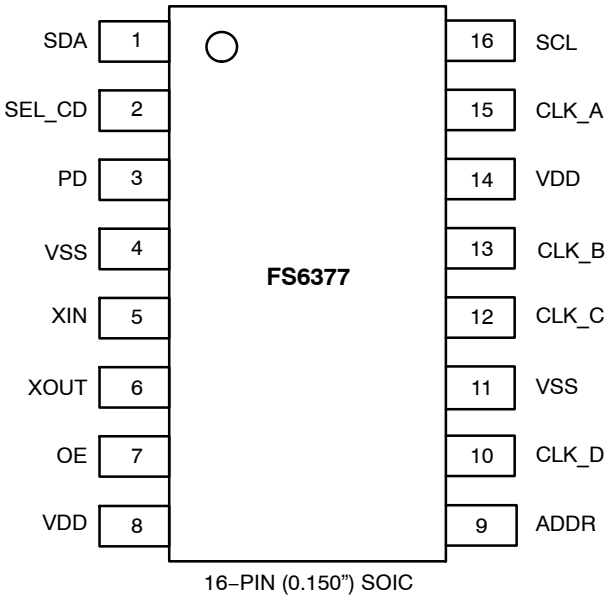


Figure 1. Pin Configuration

Table 1. PIN DESCRIPTION (Note 1)

Pin	Type	Name	Description
1	$DI^{U}O$	SDA	Serial interface data input/output
2	DI^{U}	SEL_CD	Selects one of two PLL C, mux D/C and post divider C/D combinations
3	DI^{U}	PD	Power-down input
4	P	VSS	Ground
5	AI	XIN	Crystal oscillator input
6	AO	XOUT	Crystal oscillator output
7	DI^{U}	OE	Output enable input
8	P	VDD	Power supply (5 V to 3.3 V)
9	DI^{U}	ADDR	Address select
10	DO	CLK_D	D clock output
11	P	VSS	Ground
12	DO	CLK_C	C clock output
13	DO	CLK_B	B clock output
14	P	VDD	Power supply (5 V to 3.3 V)
15	DO	CLK_A	A clock output
16	DI^{U}	SCL	Serial interface clock output

1. Key: AI: Analog Input; AO = Analog Output; DI = Digital Input; DI^{U} = Input with Internal Pull−up; DI^{D} = Input with Internal Pull−down; DIO = Digital Input/Output; DI−3 = Three−level Digital Input; DO = Digital Output; P = Power/Ground; # = Active Low Pin.

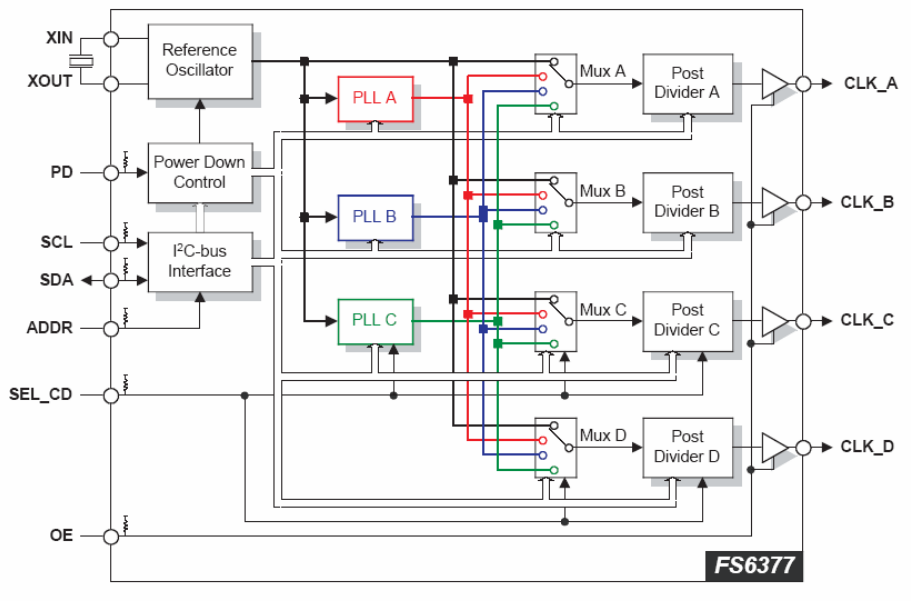


Figure 2. Block Diagram

FUNCTIONAL BLOCK DESCRIPTION

Phase Locked Loops (PLLs)

Each of the three on−chip PLLs is a standard phase− and frequency−locked loop architecture that multiplies a reference frequency to a desired frequency by a ratio of integers. This frequency multiplication is exact.

As shown in Figure 3 each PLL consists of a reference divider, a phase−frequency detector (PFD), a charge pump, an internal loop filter, a voltage−controlled oscillator (VCO), and a feedback divider.

During operation, the reference frequency (f_{REF}), generated by the on−board crystal oscillator, is first reduced by the reference divider. The divider value is called the "modulus," and is denoted as N_R for the reference divider. The divided reference is then fed into the PFD.

The PFD controls the frequency of the VCO (f_{VCO}) through the charge pump and loop filter. The VCO provides a high speed, low noise, continuously variable frequency clock source for the PLL. The output of the VCO is fed back to the PFD through the feedback divider (the modulus is denoted by N_F) to close the loop.

The PFD will drive the VCO up or down in frequency until the divided reference frequency and the divided VCO frequency appearing at the inputs of the PFD are equal. The input/output relationship between the reference frequency and the VCO frequency is:

$$f_{VCO} = f_{REF}\left(\frac{N_F}{N_R}\right) \qquad \text{(eq. 1)}$$

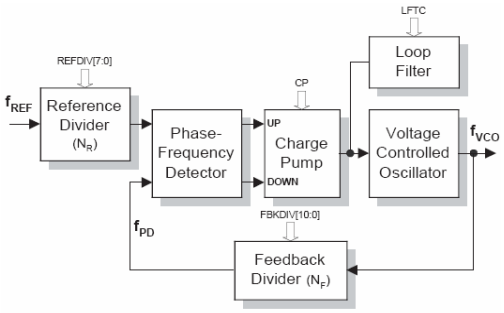


Figure 3. PLL Diagram

Reference Divider

The reference divider is designed for low phase jitter. The divider accepts the output of the reference oscillator and provides a divided− down frequency to the PFD. The reference divider is an 8−bit divider, and can be programmed for any modulus from 1 to 255 by programming the equivalent binary value. A divide−by−256 can also be achieved by programming the eight bits to 00h.

Feedback Divider

The feedback divider is based on a dual−modulus prescaler technique. The technique allows the same granularity as a fully programmable feedback divider, while still allowing the programmable portion to operate at low speed. A high−speed pre−divider (also called a prescaler) is placed between the VCO and the programmable feedback

divider because of the high speeds at which the VCO can operate. The dual−modulus technique insures reliable operation at any speed that the VCO can achieve and reduces the overall power consumption of the divider.

For example, a fixed divide−by−eight could be used in the feedback divider. Unfortunately, a divide−by−eight would limit the effective modulus of the entire feedback divider to multiples of eight. This limitation would restrict the ability of the PLL to achieve a desired input− frequency−to−output frequency ratio without making both the reference and feedback divider values comparatively large.

A large feedback modulus means that the divided VCO frequency is relatively low, requiring a wide loop bandwidth to permit the low frequencies. A narrow loop bandwidth tuned to high frequencies is essential to minimizing jitter; therefore, divider moduli should always be as small as possible.

To understand the operation, refer to Figure 4. The M−counter (with a modulus always equal to M) is cascaded with the dual−modulus prescaler. The A−counter controls the modulus of the prescaler. If the value programmed into the A−counter is A, the prescaler will be set to divide by N+1 for A prescaler outputs. Thereafter, the prescaler divides by N until the M−counter output resets the A−counter, and the cycle begins again. Note that N=8 and A and M are binary numbers.

Suppose that the A−counter is programmed to zero. The modulus of the prescaler will always be fixed at N; and the entire modulus of the feedback divider becomes MxN.

Next, suppose that the A−counter is programmed to a one. This causes the prescaler to switch to a divide−by−N+1 for its first divide cycle and then revert to a divide−by−N. In effect, the A−counter absorbs (or “swallows”) one extra clock during the entire cycle of the feedback divider. The overall modulus is now seen to be equal to MxN+1.

This example can be extended to show that the feedback divider modulus is equal to MxN+A, where A<M.

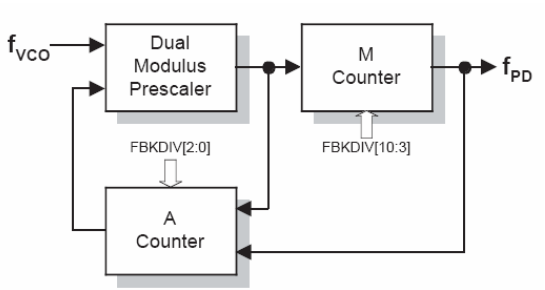


Figure 4. Feedback Divider

Feedback Divider Programming

For proper operation of the feedback divider, the A−counter must be programmed only for values that are less than or equal to the M− counter. Therefore, not all divider moduli below 56 are available for use. The selection of divider values is listed in Table 2.

Above a modulus of 56, the feedback divider can be programmed to any value up to 2047.

Table 2. FEEDBACK DIVIDER MODULUS UNDER 56

M−Counter: FBKDIV[10:3]	A−Counter: FBKDIV[2:0]							
	000	001	010	011	100	101	110	111
00000001	8	9						
00000010	16	17	18					
00000011	24	25	26	27				
00000100	32	33	34	35	36			
00000101	40	41	42	43	44	45		
00000110	48	49	50	51	52	53	54	
00000111	56	57	58	59	60	61	62	63
Feedback Divider Modulus								

Post Divider Muxes

As shown in Figure 2, an input mux in front of each post divider stage can select from any one of the PLL frequencies or the reference frequency. The frequency selection is done via the I^2C−bus.

The input frequency on two of the four muxes (mux C and D in Figure 2 can be changed without reprogramming by a logic−level input on the SEL_CD pin.

Post Dividers

The post divider performs several useful functions. First, it allows the VCO to be operated in a narrower range of speeds compared to the variety of output clock speeds that the device is required to generate. Second, it changes the basic PLL equation to

$$f_{CLK} = f_{REF}\left(\frac{N_F}{N_R}\right)\left(\frac{1}{N_P}\right) \quad \text{(eq. 2)}$$

where N_F, N_R and N_P are the feedback, reference and post divider moduli respectively, and f_{CLK} and f_{REF} are the output and reference oscillator frequencies. The extra integer in the denominator permits more flexibility in the programming of the loop for many applications where frequencies must be achieved exactly.

The modulus on two of the four post dividers muxes (post dividers C and D in Figure 2) can be altered without reprogramming by a logic level on the SEL_CD pin.

DEVICE OPERATION

The FS6377 powers up with all internal registers cleared to zero, delivering the crystal frequency to all outputs. For operation to occur, the registers must be loaded in a most significant−bit (MSB) to least−significant−bit (LSB) order. The register mapping of the FS6377 is shown in Table 3, and I^2C−bus programming information is detailed in I^2C−bus Control Interface section.

Control of the reference, feedback and post dividers is detailed in Table 5. Selection of these dividers directly controls how fast the VCO will run. The maximum VCO speed is noted in Table 13.

SEL_CD Input

The SEL_CD pin provides a way to alter the operation of PLL C, muxes C and D and post dividers C and D without having to reprogram the device. A logic−low on the SEL_CD pin selects the control bits with a “C1” or “D1” notation, per Table 3. A logic−high on the SEL_CD pin selects the control bits with “C2” or “D2” notation, per Table 3.

Note that changing between two running frequencies using the SEL_CD pin may produce glitches in the output, especially if the post− divider(s) is/are altered.

Power−Down and Output Enable

A logic−high on the PD pin powers down only those portions of the FS6377 which have their respective power−down control bits enabled. Note that the PD pin has an internal pull−up.

When a post divider is powered down, the associated output driver is forced low. When all PLLs and post dividers are powered down the crystal oscillator is also powered down. The XIN pin is forced low, and the XOUT pin is pulled high.

A logic−low on the OE pin tristates all output clocks. Note that this pin has an internal pull−up.

Oscillator Overdrive

For applications where an external reference clock is provided (and the crystal oscillator is not required), the reference clock should be connected to XOUT and XIN should be left unconnected (float).

For best results, make sure the reference clock signal is as jitter−free as possible, can drive a 40 pF load with fast rise and fall times and can swing rail−to−rail.

If the reference clock is not a rail−to−rail signal, the reference must be AC coupled to XOUT through a 0.01 μF or 0.1 μF capacitor. A minimum 1 V peak−to−peak signal is required to drive the internal differential oscillator buffer.

I^2C−BUS CONTROL INTERFACE

This device is a read/write slave device meeting all Philips I^2C−bus specifications except a “general call.” The bus has to be controlled by a master device that generates the serial clock SCL, controls bus access and generates the START and STOP conditions while the device works as a slave. Both master and slave can operate as a transmitter or receiver, but the master device determines which mode is activated. A device that sends data onto the bus is defined as the transmitter, and a device receiving data as the receiver.

I^2C−bus logic levels noted herein are based on a percentage of the power supply (V_{DD}). A logic−one corresponds to a nominal voltage of VDD, while a logic−zero corresponds to ground (V_{SS}).

Bus Conditions

Data transfer on the bus can only be initiated when the bus is not busy. During the data transfer, the data line (SDA) must remain stable whenever the clock line (SCL) is high. Changes in the data line while the clock line is high will be interpreted by the device as a START or STOP condition. The following bus conditions are defined by the I^2C−bus protocol.

Not Busy

Both the data (SDA) and clock (SLC) lines remain high to indicate the bus is not busy.

*START Data Transfe*r

A high to low transition of the SDA line while the SCL input is high indicates a START condition. All commands to the device must be preceded by a START condition.

STOP Data Transfer

A low to high transition of the SDA line while SCL is held high indicates a STOP condition. All commands to the device must be followed by a STOP condition.

Data Valid

The state of the SDA line represents valid data if the SDA line is stable for the duration of the high period of the SCL line after a START condition occurs. The data on the SDA line must be changed only during the low period of the SCL signal. There is one clock pulse per data bit.

Each data transfer is initiated by a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is determined by the master device, and can continue indefinitely. However, data that is overwritten to the device after the first sixteen bytes will overflow into the first register, then the second, and so on, in a first−in, first−overwritten fashion.

Acknowledge

When addressed, the receiving device is required to generate an acknowledge after each byte is received. The master device must generate an extra clock pulse to coincide

with the acknowledge bit. The acknowledging device must pull the SDA line low during the high period of the master acknowledge clock pulse. Setup and hold times must be taken into account.

The master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been read (clocked) out of the slave. In this case, the slave must leave the SDA line high to enable the master to generate a STOP condition.

I²C−Bus Operation

All programmable registers can be accessed randomly or sequentially via this bi−directional two wire digital interface. The device accepts the following I²C−bus commands.

Slave Address

After generating a START condition, the bus master broadcasts a seven−bit slave address followed by a R/W bit. The address of the device is:

A6	A5	A4	A3	A2	A1	A0
1	0	1	1	X	0	0

where X is controlled by the logic level at the ADDR pin.

The variable ADDR bit allows two different devices to exist on the same bus. Note that every device on an I²C−bus must have a unique address to avoid bus conflicts. The default address sets A2 to one via the pull−up on the ADDR pin.

Random Register Write Procedure

Random write operations allow the master to directly write to any register. To initiate a write procedure, the R/W bit that is transmitted after the seven−bit device address is a logic−low. This indicates to the addressed slave device that a register address will follow after the slave device acknowledges its device address. The register address is written into the slave's address pointer. Following an acknowledge by the slave, the master is allowed to write eight bits of data into the addressed register. A final acknowledge is returned by the device, and the master generates a STOP condition.

If either a STOP or a repeated START condition occurs during a register write, the data that has been transferred is ignored.

Random Register Read Procedure

Random read operations allow the master to directly read from any register. To perform a read procedure, the R/W bit that is transmitted after the seven−bit address is a logic−low, as in the register write procedure. This indicates to the addressed slave device that a register address will follow after the slave device acknowledges its device address. The register address is then written into the slave's address pointer.

Following an acknowledge by the slave, the master generates a repeated START condition. The repeated START terminates the write procedure, but not until after the slave's address pointer is set. The slave address is then resent, with the R/W bit set this time to a logic−high, indicating to the slave that data will be read. The slave will acknowledge the device address, and then transmits the eight−bit word. The master does not acknowledge the transfer but does generate a STOP condition.

Sequential Register Write Procedure

Sequential write operations allow the master to write to each register in order. The register pointer is automatically incremented after each write. This procedure is more efficient than the random register write if several registers must be written.

To initiate a write procedure, the R/W bit that is transmitted after the seven−bit device address is a logic−low. This indicates to the addressed slave device that a register address will follow after the slave device acknowledges its device address. The register address is written into the slave's address pointer. Following an acknowledge by the slave, the master is allowed to write up to sixteen bytes of data into the addressed register before the register address pointer overflows back to the beginning address. An acknowledge by the device between each byte of data must occur before the next data byte is sent.

Registers are updated every time the device sends an acknowledge to the host. The register update does not wait for the STOP condition to occur. Registers are therefore updated at different times during a sequential register write.

Sequential Register Read Procedure

Sequential read operations allow the master to read from each register in order. The register pointer is automatically incremented by one after each read. This procedure is more efficient than the random register read if several registers must be read.

To perform a read procedure, the R/W bit that is transmitted after the seven−bit address is a logic−low, as in the register write procedure. This indicates to the addressed slave device that a register address will follow after the slave device acknowledges its device address. The register address is then written into the slave's address pointer.

Following an acknowledge by the slave, the master generates a repeated START condition. The repeated START terminates the write procedure, but not until after the slave's address pointer is set. The slave address is then resent, with the R/W bit set this time to a logic−high, indicating to the slave that data will be read. The slave will acknowledge the device address, and then transmits all 16 bytes of data starting with the initial addressed register. The register address pointer will overflow if the initial register address is larger than zero. After the last byte of data, the master does not acknowledge the transfer but does generate a STOP condition.

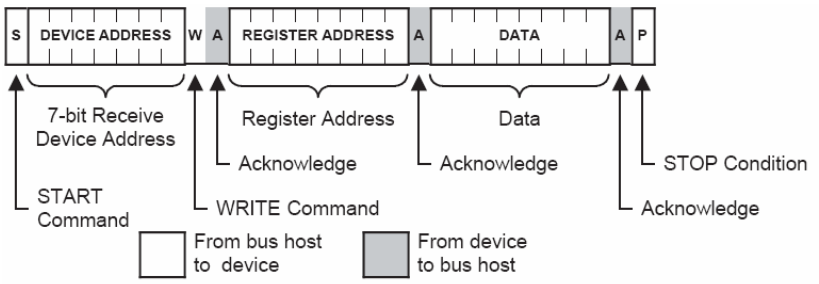


Figure 5. Random Register Write Procedure

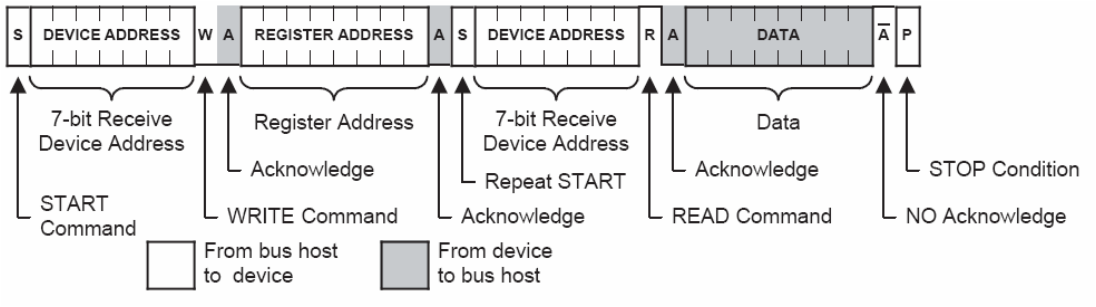


Figure 6. Random Register Read Procedure

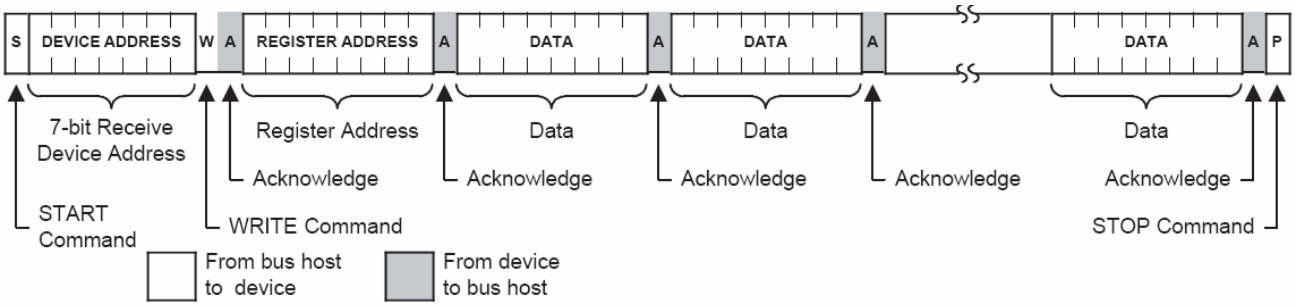


Figure 7. Sequential Register Write Procedure

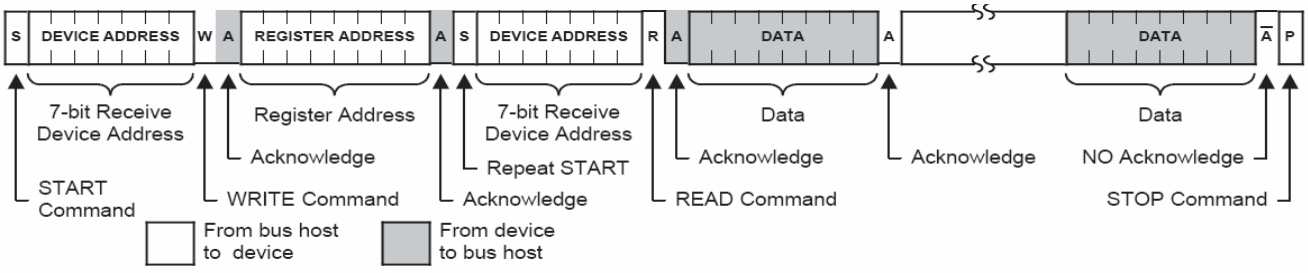


Figure 8. Sequential Register Read Procedure

PROGRAMMING INFORMATION

Table 3. REGISTER MAP

Address	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Byte 15	MUX_D2[1:0] (selected via SEL_CD = 1)		MUX_C2[1:0] (selected via SEL_CD = 1)		PDPOST_D	PDPOST_C	PDPOST_B	PDPOST_A
Byte 14	POST_D2[3:0] (selected via SEL_CD = 1)				POST_C2[3:0] (selected via SEL_CD = 1)			
Byte 13	POST_D1[3:0] (selected via SEL_CD = 0)				POST_C1[3:0] (selected via SEL_CD = 0)			
Byte 12	POST_B[3:0]				POST_A[3:0]			
Byte 11	MUX_D1[1:0] (selected via SEL_CD = 0)		Reserved (0)	LFTC_C2 (SEL_CD = 1)	CP_C2 (SEL_CD = 1)	FBKDIV_D2[10:8] *M−Counter* (selected via SEL_CD pin = 1)		
Byte 10	FBKDIV_C2[7:3] *M−Counter* (selected via SEL_CD pin = 1)					FBKDIV_C2[2:0] A−Counter (selected via SEL_CD pin = 1)		
Byte 9	REFDIV_C2[7:0] (selected via SEL_CD pin = 1)							
Byte 8	MUX_C1[1:0] (selected via SEL_CD = 0)		PDPLL_C	LFTC_C1 (SEL_CD = 0)	CP_C1 (SEL_CD = 0)	FBKDIV_c1[10:8] *M−Counter* (selected via SEL_CD = 0)		
Byte 7	FBKDIV_C1[7:3] *M−Counter* (selected via SEL_CD = 0)					FBKDIV_C1[2:0] A−Counter (selected via SEL_CD = 1)		
Byte 6	REFDIV_C1[7:0] (selected via SEL_CD = 0)							
Byte 5	MUX_B[1:0]		PDPLL_B	LFTC_B	CP_B	FBKDIV_B[10:8] *M−Counter*		
Byte 4	FBKDIV_B[7:3] *M−Counter*					FBKDIV_B[2:0] *A−Counter*		
Byte 3	REFDIV_B[7:0]							
Byte 2	MUX_A[1:0]		PDPLL_A	LFTC_A	CP_A	FBKDIV_A[10:8] *M−Counter*		
Byte 1	FBKDIV_A[7:3] *M−Counter*					FBKDIV_A[2:0] *A−Counter*		
Byte 0	REFDIV_A[7:0]							

NOTE: All register bits are cleared to zero on power−up.

Control Bit Assignment

If any PLL control bit is altered during device operation, including those bits controlling the reference and feedback dividers, the output frequency will slew smoothly (in a glitch−free manner) to the new frequency. The slew rate is related to the programmed loop filter time constant

However, any programming changes to any mux or post divider control bits will cause a glitch on an operating clock output.

Power−Down

All power−down functions are controlled by enable bits. The bits select which portions of the device to power−down when the PD input is asserted.

Table 4. POWER−DOWN BITS

Name	Description	
Power−Down PLL A		
PDPLL_A (Bit 21)	Bit = 0 Bit = 1	Power on Power off
Power−Down PLL B		
PDLL_B (Bit 45)	Bit = 0 Bit = 1	Power on Power off
Power−Down PLL C		
PDLL_C (Bit 69)	Bit = 0 Bit = 1	Power on Power off
Reserved (0) (Bit 69)	Set these reserved bits to zero (0)	
Power−Down POST Divider A		
PDPOSTA (Bit 120	Bit = 0 Bit = 1	Power on Power off
Power−Down POST Divider B		
PDPOSTB (Bit 121)	Bit = 0 Bit = 1	Power on Power off
Power−Down POST Divider C		
PDPOSTC (Bit 122)	Bit = 0 Bit = 1	Power on Power off
Power−Down POST Divider D		
PDPOSTD (Bit 123)	Bit = 0 Bit = 1	Power on Power off

Table 5. DIVIDER CONTROL BITS

Name	Description	
REFDIV_A[7:0] (Bits 7−0)	Reference Divider A (N_R)	
REFDIV_B[7:0] (Bits 31−24)	Reference Divider B (N_R)	
REFDIV_C1[7:0] (Bits 55−48)	Reference Divider C1 (N_R) *selected when the SEL_CD pin = 0*	
REFDIV_C2[7:0] (Bits 79−72)	Reference Divider C2 (N_R) *selected when the SEL_CD pin = 1*	
Feedback Divider A (N_F)		
FBKDIV_A[10:0] (Bits 18−8)	FBKDIV_A[2:0] FBKDIV_A[10:3]	A−Counter value M−Counter value
Feedback Divider B (N_F)		
FBKDIV_B[10:0] (Bits 42−32)	FBKDIV_B[2:0] FBKDIV_B[10:3]	A−Counter value M−Counter value
Feedback Divider C1 (N_F) *selected when the SEL_CD pin = 0*		
FBKDIV_C1[10:0] (Bits 66−56)	FBKDIV_C1[2:0] FBKDIV_C1[10:3]	A−Counter value M−Counter value
Feedback Divider C2 (N_F) *selected when the SEL_CD pin = 1*		
FBKDIV_C2[10:0] (Bits 90-80)	FBKDIV_C2[2:0] FBKDIV_C2[10:3]	A−Counter value M−Counter value

Table 6. DIVIDER CONTROL BITS

Name	Description
POST_A[3:0] (Bits 99−96)	POST divider A (see Table 7)
POST_B[3:0] (Bits 103−100)	POST divider B (see Table 7)
POST_C1[3:0] (Bits 107−104)	POST divider C1 (see Table 7) *selected when the SEL_CD pin = 0*
POST_C2[3:0] (Bits 115−112)	POST divider C2 (see Table 7) *selected when the SEL_CD pin = 1*
POST_D1[3:0] (Bits 111−108)	POST divider D1 (see Table 7) *selected when the SEL_CD pin = 0*
POST_D2[3:0] (Bits 119−116)	POST divider D2 (see Table 7) *selected when the SEL_CD pin = 1*

Table 7. POST DIVIDER MODULUS

BIT [3]	BIT [2]	BIT [1]	BIT [0]	Divide By
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	8
0	1	1	1	9
1	0	0	0	10
1	0	0	1	12
1	0	1	0	15
1	0	1	1	16
1	1	0	0	18
1	1	0	1	20
1	1	1	0	25
1	1	1	1	50

Table 8. PLL TUNING BITS

Name	Description	
Loop Filter Time Constant A		
LFTC_A (Bit 20)	Bit = 0 Bit = 1	Short time constant: 7 μs Long time constant: 20 μs
Loop Filter Time Constant B *selected when the SEL_CD pin = 0*		
LFTC_B (Bit 44)	Bit = 0 Bit = 1	Short time constant: 7 μs Long time constant: 20 μs
Loop Filter Time Constant C1 *selected when the SEL_CD pin = 1*		
LFTC_C1 (Bit 68)	Bit = 0 Bit = 1	Short time constant: 7 μs Long time constant: 20 μs
Loop Filter Time Constant C2		
LFTC_C2 (Bit 92)	Bit = 0 Bit = 1	Short time constant: 7 μs Long time constant: 20 μs
Charge Pump A		
CP_A (Bit 19)	Bit = 0 Bit = 1	Current = 2 μA Current = 10 μA
Charge Pump B		
CP_B (Bit 43)	Bit = 0 Bit = 1	Current = 2 μA Current = 10 μA
Charge Pump C1 *selected when the SEL_CD pin = 0*		
CP_C1 (Bit 67)	Bit = 0 Bit = 1	Current = 2 μA Current = 10 μA
Charge Pump C2 *selected when the SEL_CD pin = 1*		
CP_C2 (Bit 91)	Bit = 0 Bit = 1	Current = 2 μA Current = 10 μA

Table 9. MUX SELECT BITS

Name	Description		
Mux A Frequency Select			
MUX_A[1:0] (Bits 23−22)	Bit 23	Bit 22	
	0	0	Reference frequency
	0	1	PLL A frequency
	1	0	PLL B frequency
	1	1	PLL C frequency
Mux B Frequency Select			
MUX_B[1:0] (Bits 47−46)	Bit 47	Bit 46	
	0	0	Reference frequency
	0	1	PLL A frequency
	1	0	PLL B frequency
	1	1	PLL C frequency
Mux C1 Frequency Select *selected when the SEL_CD pin = 0*			
MUX_C1[1:0] (Bits 71−70)	Bit 71	Bit 70	
	0	0	Reference frequency
	0	1	PLL A frequency
	1	0	PLL B frequency
	1	1	PLL C frequency
Mux C2 Frequency Select *selected when the SEL_CD pin = 1*			
MUX_C2[1:0] (Bits 125−124)	Bit 125	Bit 124	
	0	0	Reference frequency
	0	1	PLL A frequency
	1	0	PLL B frequency
	1	1	PLL C frequency
Mux D1 Frequency Select *selected when the SEL_CD pin = 0*			
MUX_D1[1:0] (Bits 95−94)	Bit 95	Bit 94	
	0	0	Reference frequency
	0	1	PLL A frequency
	1	0	PLL B frequency
	1	1	PLL C frequency
Mux D2 Frequency Select *selected when the SEL_CD pin = 1*			
MUX_D2[1:0] (Bits 127−126)	Bit 127	Bit 126	
	0	0	Reference frequency
	0	1	PLL A frequency
	1	0	PLL B frequency
	1	1	PLL C frequency

ELECTRICAL SPECIFICATIONS

Table 10. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Minimum	Maximum	Unit
V_{DD}	Supply voltage, dc (V_{SS} = ground)	V_{SS} − 0.5	7	V
V_1	Input voltage, dc	V_{SS} − 0.5	V_{DD} + 0.5	V
V_O	Output voltage, dc	V_{SS} − 0.5	V_{DD} + 0.5	V
I_{IK}	Input clamp current, dc (V_I < 0 or V_I > $V_{DD)}$	−50	50	mA
I_{OK}	Output clamp current, dc (V_I < 0 or V_I > V_{DD})	−50	50	mA
T_S	Storage temperature range (non−condensing)	−65	150	°C
T_A	Ambient temperature range, under bias	−55	125	°C
T_J	Junction temperature		150	°C
	Re−flow solder profile			Per IPC/JEDEC J−STD−020B
	Input static discharge voltage protection (MIL−STD 883E, Method 3015.7)		2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

WARNING: ELETROSTATIC SENSITIVE DEVICE
Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high−energy electrostatic discharge.

Table 11. RECOMMENDED OPERATING RANGES

Symbol	Parameter	Description	Min	Type	Max	Unit
V_{DD}	Supply voltage	5V ± 10% 3.3V ± 10%	4.5 3	5 3.3	5.5 3.6	V
T_A	Ambient operating temperature range	Commercial Industrial	0 −40		70 85	°C
f_{XIN}	Crystal resonator frequency		5		27	MHz
C_{XL}	Crystal resonator load capacitance	Parallel resonant, AT cut		18		pF
	Serial data transfer rate	Standard mode	10		100	kb/s
C_L	Output driver load capacitance				15	pF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 12. DC CHARACTERISTICS

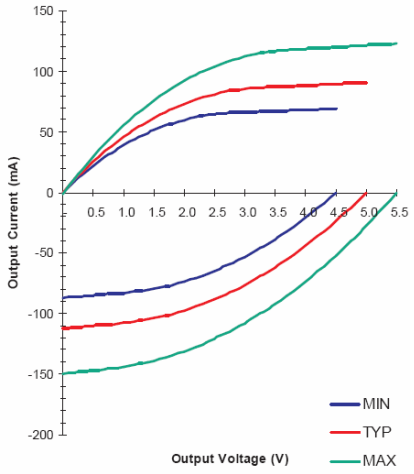
(Unless otherwise stated, V_{DD} = 5.0 V ±10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested on any specific limits. Min. and max. characterization data are ±3σ from typical. Negative currents indicate current flows out of the device.)

Symbol	Parameter	Characteristic	Min	Typ	Max	Unit
OVERALL						
I_{DD}	Supply current, dynamic, with load outputs	V_{DD} = 5.5 V, f_{CLK} = 50 MHz, C_L = 15 pF See Figure 10 for more information		43		mA
I_{DDL}	Supply current, static	V_{DD} = 5.5 V, device powered down		0.3		mA
POWER−DOWN, OUTPUT ENABLE PINS (PD, OE)						
V_{IH}	High−level input voltage	V_{DD} = 5.5 V V_{DD} = 3.6 V	3.85 2.52		V_{DD} + 0.3 V_{DD} + 0.3	V
V_{IL}	Low−level input voltage	V_{DD} = 5.5 V V_{DD} = 3.6 V	V_{SS} − 0.3 V_{SS} − 0.3		1.65 1.08	V
V_{hys}	Hysteresis voltage	V_{DD} = 5.5 V V_{DD} = 3.6 V		2.20 1.44		V
I_{IH}	High−level input current		−1		1	μA
I_{IL}	Low−level input current (pull−up)	V_{IL} = 0 V	−20	−36	−80	μA
SERIAL INTERFACE I/O (SCL, SDA)						
V_{IH}	High−level input voltage	V_{DD} = 5.5 V V_{DD} = 3.6 V	3.85 2.52		V_{DD} + 0.3 V_{DD} + 0.3	V
V_{IL}	Low−level input voltage	V_{DD} = 5.5 V V_{DD} = 3.6 V	V_{SS} − 0.3 V_{SS} − 0.3		1.65 1.08	V
V_{hys}	Hysteresis voltage	V_{DD} = 5.5 V V_{DD} = 3.6 V		2.20 1.44		V
I_{IH}	High−level input current		−1		1	μA
I_{IL}	Low−level input current (pull−up)	V_{IL} = 0 V	−20	−36	−80	μA
I_{OL}	Low−level output sink current (SDA)	V_{OL} = 0.4 V, V_{DD} = 5.5 V		26		mA
MODE AND FREQUENCY SELECT INPUTS (ADDR, SEL_CD)						
V_{IH}	High−level input voltage	V_{DD} = 5.5 V V_{DD} = 3.6 V	2.4 2.0		V_{DD} + 0.3 V_{DD} + 0.3	V
V_{IL}	Low−level input voltage	V_{DD} = 5.5 V V_{DD} = 3.6 V	V_{SS} − 0.3 V_{SS} − 0.3		0.8 0.8	V
I_{IH}	High−level input current		−1		1	μA
I_{IL}	Low−level input current (pull−up)		−20	−36	−80	μA
CRYSTAL OSCILLATOR FEEDBACK (XIN)						
V_{TH}	Threshold bias voltage	V_{DD} = 5.5 V V_{DD} = 3.6 V		2.9 1.7		V
I_{IH}	High−level input current	V_{DD} = 5.5 V V_{DD} = 5.5 V, oscillator powered down	5	54	15	μA mA
I_{IL}	Low−level input current	V_{DD} = 5.5 V	−25	−54	−75	μA
$C_{L(xtal)}$	Crystal loading capacitance*	As seen by an external crystal connected to XIN and XOUT		18		pF
$C_{L(XIN)}$	Input loading capacitance*	As seen by an external clock driver on XOUT; XIN unconnected		36		pF

Table 12. DC CHARACTERISTICS (continued)
(Unless otherwise stated, V_{DD} = 5.0 V ±10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested on any specific limits. Min. and max. characterization data are ±3σ from typical. Negative currents indicate current flows out of the device.)

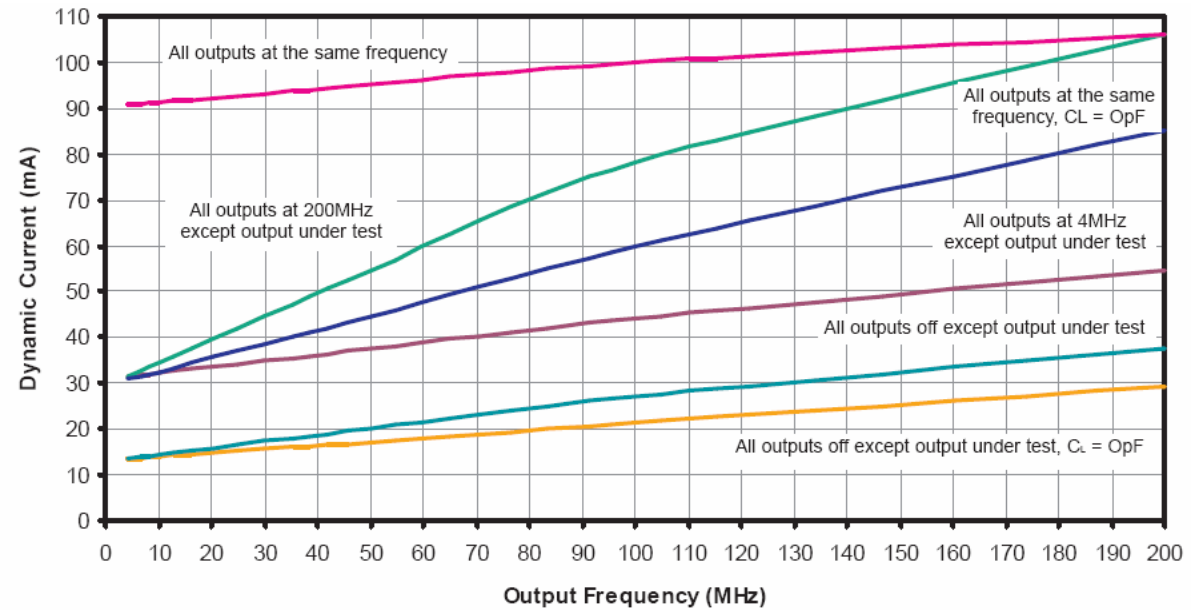
Symbol	Parameter	Characteristic	Min	Typ	Max	Unit
CRYSTAL OSCILLATOR DRIVER (XOUT)						
I_{OH}	High−level output source current	V_{DD} = $V_{(XIN)}$ = 5.5V, V_O = 0 V	10	21	30	mA
I_{OL}	Low−level output sink current	V_{DD} = 5.5 V, $V_{(XIN)}$ = 0 V, V_O = 5.5 V	−10	−21	−30	mA
CLOCK OUTPUTS (CLK_A, CLK_B, CLK_C, CLK_D)						
I_{OH}	High−level output source current	V_O = 2.4 V		−125		mA
I_{OL}	Low−level output sink current	V_O = 0.4 V		23		mA
Z_{OH} Z_{OL}	Output impedance	V_O = 0.5 VDD Output driving high Output driving low		 29 27		Ω
I_Z	Tristate output current		−10		−10	μA
I_{SCH}	Short circuit source current*	V_{DD} = 5.5 V, V_O = 0 V; shorted for 30 s, max.		−150		mA
I_{SCL}	Short circuit sink current*	V_{DD} = V_O = 5.5 V; shorted for 30 s, max.		123		mA

Low Drive Current (mA)				High Drive Current (mA)			
Voltage (V)	Min.	Typ.	Max.	Voltage (V)	Min.	Typ.	Max.
0	0	0	0	0	−87	−112	−150
0.2	9	11	12	0.5	−85	−110	−147
0.5	22	25	29	1	−83	−108	−144
0.7	29	34	40	1.5	−80	−104	−139
1	39	46	55	2	−74	−97	−131
1.2	44	52	64	2.5	−65	−88	−121
1.5	51	61	76	2.7	−61	−84	−116
1.7	55	66	83	3	−53	−77	−108
2	60	73	92	3.2	−48	−71	−102
2.2	62	77	97	3.5	−39	−62	−92
2.5	65	81	104	3.7	−32	−55	−85
2.7	65	83	108	4	−21	−44	−74
3	66	85	112	4.2	−13	−36	−65
3.5	67	87	117	4.5	0	−24	−52
4	68	88	119	4.7		−15	−43
4.5	69	89	120	5		0	−28
5		91	121	5.2			−11
5.5			123	5.5			0

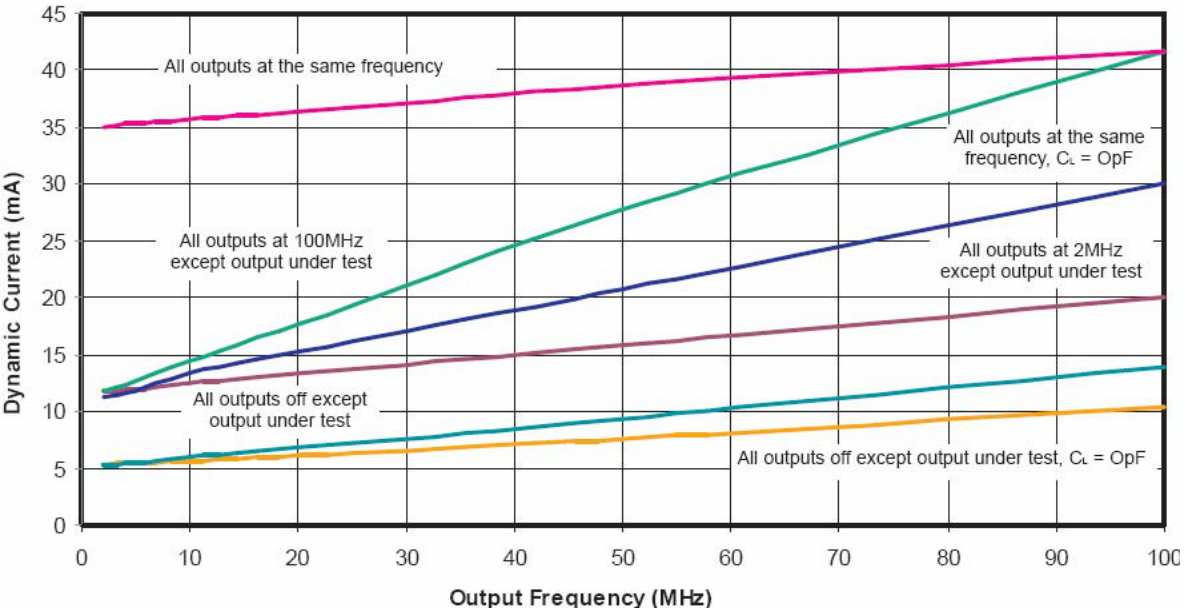


The data in this table represents nominal characterization data only.

Figure 9. CLK_A, CLK_B, CLK_C, CLK_D Clock Outputs



V_{DD} = 5.0V; Reference Frequency = 27.00MHz; VCO Frequency= 200MHz, C_L = 17$_p$F except where noted



V_{DD} = 3.3V; Reference Frequency = 27.00MHz; VCO Frequency = 100MHz, C_L = 17$_p$F except where noted

Figure 10. Dynamic Current vs Output Frequency

Table 13. AC TIMING SPECIFICATIONS

(Unless otherwise stated, V_{DD} = 5.0 V ±10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. Min. and max. characterization data are ±3σ from typical.)

Symbol	Parameter	Characteristic	Clock	Min	Typ	Max	Unit
OVERALL							
f_O	Output frequency*	V_{DD} = 5.5 V V_{DD} = 3.6 V		0.8 0.8		150 100	MHz
f_{VCO}	VCO frequency*	V_{DD} = 5.5 V V_{DD} = 3.6 V		40 40		230 170	MHz
A_{VCO}	VCO gain*				400		MHz/V
	Loop filter time constant*	LFTC bit = 0 LFTC bit = 1			7 20		μs
t_r	Rise time*	V_O = 0.5 V to 4.5 V; C_L = 15 pF V_O = 0.3 V to 3.0 V; C_L = 15 pF			1.9 1.6		ns
t_r	Fall time*	V_O = 4.5 V to 0.5 V; C_L = 15 pF V_O = 3.0 V to 0.3 V; C_L = 15 pF			1.8 1.5		ns
t_{PZL}, t_{PZH}	Tristate enable delay*			1		8	ns
t_{PZL}, t_{PZH}	Tristate disable delay*			1		8	ns
t_{STB}	Clock stabilization time*	Output active from power−up, via PD pin After last register is written			100	 1	μs ms
DIVIDER MODULUS							
N_F	Feedback divider	See Table 2		8		2047	
N_R	Reference divider			1		255	
N_P	Post divider	See Table 8		1		50	
CLOCK OUTPUTS (PLL A CLOCK VIA CLK_A PIN) APPROXIMATE							
	Duty cycle*	Ratio of pulse width (as measured from rising edge to next falling edge at 2.5 V) to one clock period	100	45		55	%
$t_{j(LT)}$	Jitter, long term (σy(τ))*	On rising edges 500 μs apart at 2.5 V relative to an ideal clock, C_L = 15 pF, f_{XIN} = 14.318 MHz, N_F = 220, N_R = 63, N_{PX} = 50, no other PLLs active On rising edges 500 μs apart at 2.5 V relative to an ideal clock, C_L = 15 pF, f_{XIN} = 14.318 MHz, N_F = 220, N_R = 63, N_{PX} = 50, all other PLLs active (B = 60 MHz, C = 40 MHz, D = 14.318 MHz)	100 50		45 165		ps
$t_{j(\Delta P)}$	Jitter, period (peak−peak)*	From rising edge to the next rising edge at 2.5 V, C_L = 15 pF, f_{XIN} = 14.318 MHz, N_F= 220, N_R = 63, N_{PX} = 50, no other PLLs active From rising edge to the next rising edge at 2.5 V, C_L = 15 pF, f_{XIN} = 14.318 MHz, N_F = 220, N_R = 63, N_{PX} = 50, all other PLLs active (B = 60 MHz, C = 40 MHz, D = 14.318 MHz)	100 50		110 390		ps
CLOCK OUTPUTS (PLL B CLOCK VIA CLK_B PIN) APPROXIMATE							
	Duty cycle*	Ratio of pulse width (as measured from rising edge to next falling edge at 2.5 V) to one clock period	100	45		55	%
$t_{j(LT)}$	Jitter, long term (σy(τ))*	On rising edges 500 μs apart at 2.5 V relative to an ideal clock, C_L = 15 pF, f_{XIN} = 14.318 MHz, N_F = 220, N_R = 63, N_{PX} = 50, no other PLLs active On rising edges 500 μs apart at 2.5 V relative to an ideal clock, C_L = 15 pF, f_{XIN} = 14.318MHz, N_F = 220, N_R = 63, N_{PX} = 50, all other PLLs active (A = 50 MHz, C = 40 MHz,D = 14.318 MHz)	100 60		45 75		ps

Table 13. AC TIMING SPECIFICATIONS (continued)
(Unless otherwise stated, V_{DD} = 5.0 V ±10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. Min. and max. characterization data are ±3σ from typical.)

Symbol	Parameter	Characteristic	Clock	Min	Typ	Max	Unit
CLOCK OUTPUTS (PLL B CLOCK VIA CLK_B PIN) APPROXIMATE							
$t_{j(\Delta P)}$	Jitter, period (peak–peak)*	From rising edge to the next rising edge at 2.5 V, C_L = 15 pF, f_{XIN} = 14.318 MHz, N_F = 220, N_R = 63, N_{PX} = 50, no other PLLs active	100		120		ps
		From rising edge to the next rising edge at 2.5 V, C_L = 15pF, f_{XIN} = 14.318MHz,N_F = 220, N_R = 63, N_{PX} = 50, all other PLLs active (A = 50 MHz, C = 40 MHz, D = 14.318 MHz)	60		400		
CLOCK OUTPUTS (PLL C CLOCK VIA CLK_C PIN) APPROXIMATE							
	Duty cycle*	Ratio of pulse width (as measured from rising edge to next falling edge at 2.5 V) to one clock period	100	45		55	%
$t_{j(LT)}$	Jitter, long term (σy(τ))*	On rising edges 500 μs apart at 2.5 V relative to an ideal clock, C_L = 15 pF, f_{XIN} = 14.318 MHz, N_F = 220, N_R = 63, N_{PX} = 50, no other PLLs active	100		45		ps
		On rising edges 500 μs apart at 2.5V relative to an ideal clock, C_L = 15 pF, f_{XIN} = 14.318 MHz, N_F= 220, N_R = 63, N_{PX} = 50, all other PLLs active (A = 50 MHz, B = 60 Mhz,D = 14.318 MHz)	40		105		
$t_{j(\Delta P)}$	Jitter, period (peak–peak)*	From rising edge to the next rising edge at 2.5 V, C_L = 15 pF, f_{XIN} = 14.318 MHz, N_F = 220, N_R = 63,N_{PX} = 50, no other PLLs active	100		120		ps
		From rising edge to the next rising edge at 2.5 V, C_L = 15 pF, f_{XIN} = 14.318 MHz, N_F = 220, N_R = 63, N_{PX} = 50, all other PLLs active (A = 50 MHz, B = 60 MHz, D = 14.318 MHz)	40		440		
CLOCK OUTPUTS (CRYSTAL OSCILLATOR VIA CLK_D PIN) APPROXIMATE							
	Duty cycle*	Ratio of pulse width (as measured from rising edge to next falling edge at 2.5 V) to one clock period	14.318	45		55	%
$t_{j(LT)}$	Jitter, long term (σy(τ))*	On rising edges 500 μs apart at 2.5 V relative to an ideal clock, C_L = 15 pF, f_{XIN} = 14.318 MHz, no other PLLs active	14.318		20		ps
		From rising edges to the next at 2.5 V, C_L = 15 pF, f_{XIN} = 14.318 MHz, all other PLLs active (A = 50 MHz, B = 60 MHz, C = 40 MHz)	14.318		40		
$t_{j(\Delta P)}$	Jitter, period (peak–peak)*	From rising edge to the next rising edge at 2.5 V, C_L = 15 pF, f_{XIN} = 14.318 MHz, no other PLLs active	14.318		90		ps
		From rising edge to the next rising edge at 2.5 V, C_L = 15 pF, f_{XIN} = 14.318 MHz, all other PLLs active (A = 50 MHz, B = 60 MHz, C = 40 MHz)	14.318		450		

Table 14. SERIAL INTERFACE TIMING SPECIFICATIONS

(Unless otherwise stated, all power supplies = 3.3 V ± 5%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. Min. and max. characterization data are ±3σ from typical.)

Symbol	Parameter	Characteristic	Min	Max	Unit
			Standard Mode		
f_{SCL}	Clock frequency	SCL	0	100	kHz
t_{BUF}	Bus free time between STOP and START		4.7		μs
$t_{su:STA}$	Set−up time, START (repeated)		4.7		μs
$t_{nd:STA}$	Hold time, START		4.0		μs
$t_{su:DAT}$	Set−up time, data input	SDA	250		ns
$t_{hd:DAT}$	Hold time, data input	SDA	0		μs
t_{AA}	Output data valid from clock	Minimum delay to bridge undefined region of the falling edge of SCL to avoid unintended START or STOP		3.5	μs
t_R	Rise time, data and clock	SDA, SCL		1000	ns
t_F	Fall time, data and clock	SDA, SCL		300	ns
t_{HI}	High time, clock	SCL	4.0		μs
t_{LO}	Low time, clock	SCL	4.7		μs
$T_{su:STO}$	Set−up time, STOP		4.0		μs

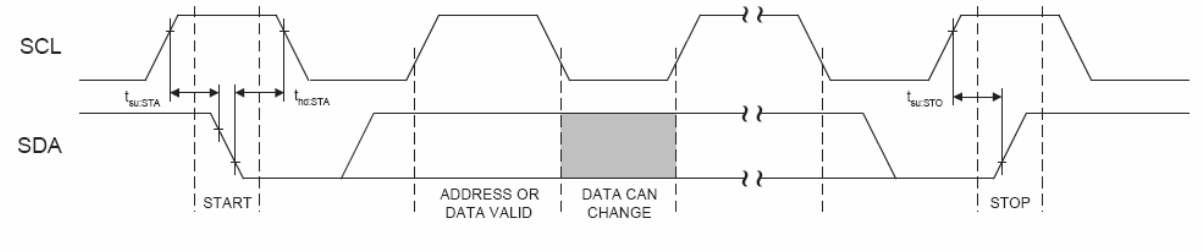


Figure 11. Bus Timing Data

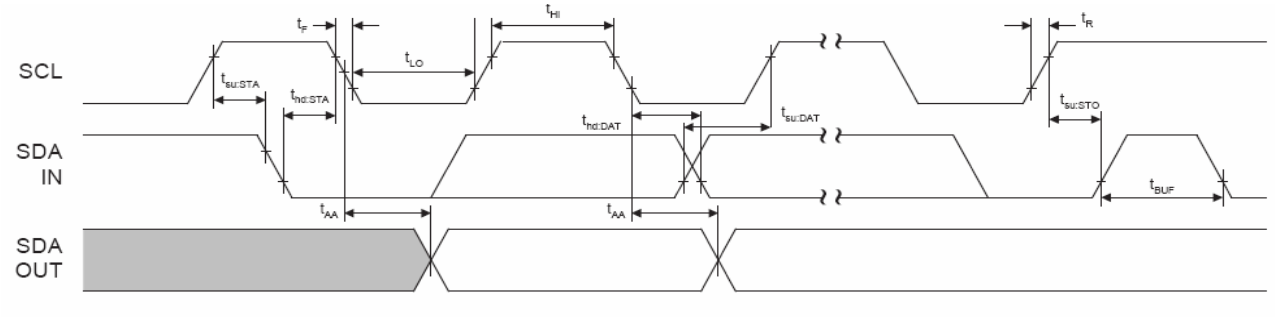


Figure 12. Data Transfer Sequence

Table 15. 16−PIN SOIC (0.150”) PACKAGE CHARACTERISTICS

Symbol	Parameter	Description	Type	Unit
ΘJA	Thermal impedance, junction to free− air16−pin 0.150” SOIC	Air flow = 0m /s	110	°C/W
L11	Lead inductance, self	Corner lead Center lead	4.0 3.0	nH nH
L12	Lead inductance, mutual	Any lead to any adjacent lead	0.4	nH
C11	Lead capacitance, bulk	Any lead to V_{SS}	0.5	pF

DEMONSTRATION SOFTWARE

Windows XP− (and earlier) based software is available from **onsemi** that illustrates the capabilities of the FS6377 and aids in application development.

Contact your local sales representative for more information.

Software Requirements

- PC running MS Windows 95/98, 98 SE, ME, NT4, 2000, XP Home Edition, or XP Professional Edition.
- 1.8MB available space on hard drive C.

Demo Program Operation

Launch the demo program from the website. Note that the parallel port cannot be accessed if your machine is not connected to the demo board. A warning message will appear as shown in Figure 13.

Clicking “Ignore” starts the program for calculation only.

The FS6377 demo hardware is available on a limited basis for demonstration by an **onsemi** field applications engineer, but is no longer available for purchase..

The opening screen is shown in Figure 14.

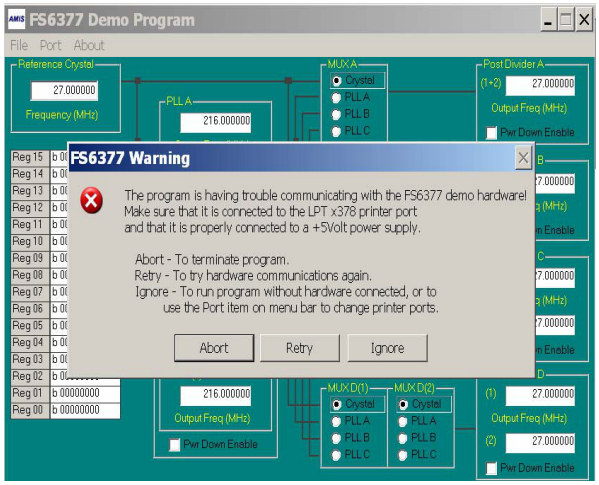


Figure 13. Warning Message− Click “Ignore”

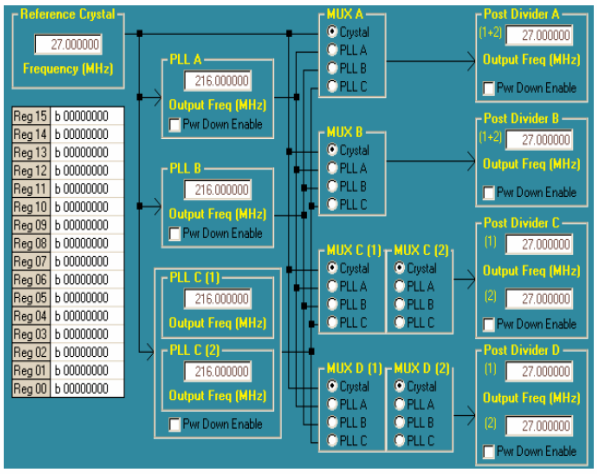


Figure 14. Opening Screen

Example Programming

Type a value for the crystal resonator frequency in MHz in the reference crystal box. This frequency provides the basis for all of the PLL calculations that follow.

Next, click on the PLL A box. A pop−up screen similar to Figure 15 should appear. Type in a desired output clock frequency in MHz, set the operating voltage (3.3 V or 5 V) and the desired maximum output frequency error. Pressing Calculate Solutions generates several possible divider and VCO−speed combinations.

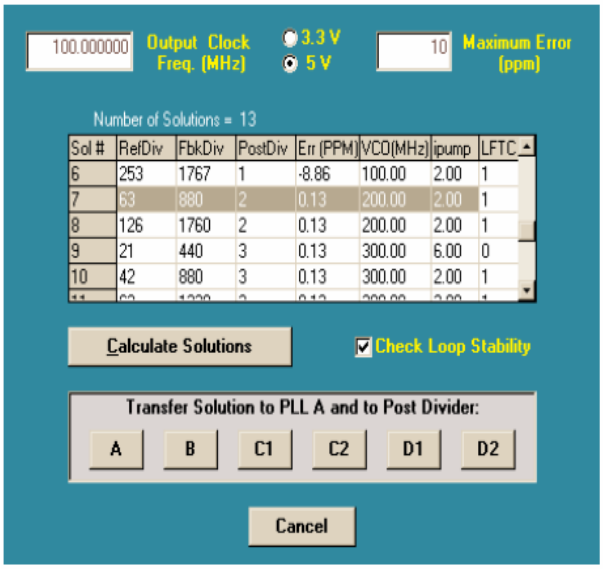


Figure 15. PLL Screen

For a 100 MHz output, the VCO should ideally operate at a higher frequency, and the reference and feedback dividers should be as small as possible. In this example, highlight Solution #7. Notice the VCO operates at 200 MHz with a post divider of two to obtain an optimal 50 percent duty cycle.

Now choose which mux and post divider to use (that is, choose an output pin for the 100 MHz output). Selecting A places the PostDiv value in Solution #7 into post divider A and switches mux A to take the output of PLL A.

The PLL screen should disappear, and now the value in the PLL A box is the new VCO frequency chosen in Solution #7. Also note that mux A has been switched to PLL A and the post divider A has the chosen 100 MHz output displayed.

Repeat the steps for PLL B.

PLL C supports two different output frequencies depending on the setting of the SEL_CD pin. Both mux C and mux D are also affected by the logic level on the SEL_CD pin, as are the post dividers C and D.

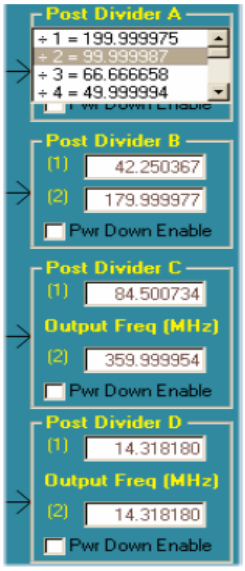


Figure 16. Post Divider Menu

Click on PLL C1 to open the PLL screen. Set a desired frequency, however, now choose the post divider B as the output divider. Notice the post divider box has split in two (as shown in Figure 16). The post divider B box now shows that the divider is dependent on the setting of the SEL_CD pin for as long as mux B is the PLL C output.

Clicking on post divider A reveals a pull−down menu provided to permit adjustment of the post divider value independently of the PLL screen. A typical menu is shown in Figure 16. The range of possible post divider values is also given in Table 7.

The register settings are shown to the left in the screen shown in Figure 14. Clicking on a register location displays a screen shown in Figure 17. Individual bits can be poked, or the entire register value can be changed.

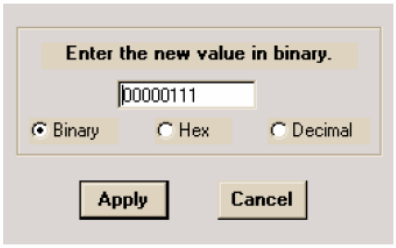


Figure 17. Register Screen

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