Product Overview

MC100EP35: ECL JK Flip-Flop

For complete documentation, see the data sheet.

The MC10EP35 is a higher speed/low voltage version of the EL35 JK flip flop. The JK data enters the master portion of the flip flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The reset pin is asynchronous and is activated with a logic HIGH.The 100 Series contains temperature compensation.

Features

- 410 ps Propagation Delay
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operatio Range: VCC = 3.0 V to 5.5 V with VEE = 0 V
- NECL Mode Operating Range: VCC = 0 V with VEE = -3.0V to -5.5V
- Open Input Default State
- Q Output will default LOW with inputs open or at VEE
- Pb-Free Packages are Available

Applications

- Using ECL Logic technologies for reducing system clock skew over the alternative CMOS and TTL technologies.

Part Electrical Specifications

Product	Pricing ($/Unit)	Compliance	Status	Type	Bits	Input Level	Output Level	V_{CC} Typ (V)	t_{Jitter} Typ (ps)	t_{pd} Typ (ns)	t_{su} Min (ns)	t_h Min (ns)	t_{rec} Typ (ns)	t_R & t_F Max (ps)	f_{Toggle} Typ (MHz)	Package Type
MC100EP35DTG		Pb-free Halide free	Active	JK-Type	1	CML ECL	ECL	5 3.3	0.2	0.41	0.15	0.15	0.15	170	3000	TSSOP-8
MC100EP35DTR2G		Pb-free Halide free	Active	JK-Type	1	ECL CML	ECL	5 3.3	0.2	0.41	0.15	0.15	0.15	170	3000	TSSOP-8

For more information please contact your local sales support at www.onsemi.com.

Created on: 1/28/2020