Description
The NB3N502 Evaluation Board was designed to provide a flexible and convenient platform to quickly evaluate, characterize and verify the performance and operation of the NB3N502 PLL Clock Multiplier. This user’s manual provides detailed information on the board’s contents, layout and use, and it should be used in conjunction with the NB3N502 data sheet which contains full technical details on device specifications and operation (www.onsemi.com).

Board Features
• Fully Assembled Evaluation Board
• Accommodates the Electrical Characterization of the NB3N502 in the SOIC–8 Package
• Supports the Use of a 5 MHz to 27 MHz Through–hole or Surface Mount Crystal
• SMA Connectors are Provided for Auxiliary Input and Output Interfaces
• Incorporates Onboard Slide Switch Controlled Multiplier Select Pins, Minimizing Excess Cabling

This Evaluation Board Manual Contains
• Information on the NB3N502 Evaluation Board
• Appropriate Lab Setup
• Evaluation Board Layout
• Bill of Materials
**Basic Equipment**
- Signal Generator (for External Reference Clock Input)
- Oscilloscope
- Power Supply
- Voltmeter
- High-Speed Cables with SMA Connectors
- High-Impedance Probe

**Power Supply Connections**
External power supply of +3 V to +5.5 V must be provided to the board.

The NB4N502 has a positive supply pin, VDD, and a ground pin, GND. Connect a single power supply to the evaluation board (see Figure 2.) by connecting VDD to the positive supply, +3 V to +5.5 V, and GND to 0 V. Power supply banana plug connectors for VDD and GND are provided at the top corners of the board.

<table>
<thead>
<tr>
<th>Supply</th>
<th>Value</th>
<th>Connector</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>+3 to +5.5 V</td>
<td>Red Banana Plug</td>
</tr>
<tr>
<td>GND</td>
<td>0 V</td>
<td>Black Banana Plug</td>
</tr>
</tbody>
</table>

**Table 1. POWER SUPPLY CONNECTIONS**

**External Reference Clock**
An SMA connector is provided for X1/CLK if an external clock source is used on Pin 1. The metal trace at the package pin is intentionally open for crystal use and must be shorted for a connection to Pin 1 for external clock use.

**Crystal and Crystal Load Capacitors Selection Guide**
A through-hole or surface mount crystal can be used. The metal traces at the crystal pins are intentionally open for crystal use and will have no impedence effect on the crystal pins.

The total on–chip capacitance is approximately 12 pF per pin (CIN1 and CIN2). A parallel resonant, fundamental mode crystal should be used. The evaluation board includes pads for small capacitors from X1/CLK to ground and from X2 to ground. These capacitors, CL1 and CL2, are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance (CLOAD (crystal)). Crystal load capacitors must be connected from each of the pins X1 and X2 to ground. The load capacitance of the crystal (CLOAD (crystal)) must be matched by total load capacitance of the oscillator circuitry network, CINX, CSX and CLX, as seen by the crystal (see Figure 3 and equations below).

\[
CLOAD1 = CIN1 + CS1 + CL1 \quad \text{[Total capacitance on X1/CLK]}
\]

\[
CLOAD2 = CIN2 + CS2 + CL2 \quad \text{[Total capacitance on X2]}
\]

\[
CIN1 \approx CIN2 \approx 12 \text{ pF (Typ) [Internal capacitance]}
\]

\[
CS1 \approx CS2 \approx 5 \text{ pF (Typ) [External PCB stray capacitance]}
\]

\[
CLOAD1,2 = 2 – CLOAD (Crystal)
\]

\[
CL2 = CLOAD2 – CIN2 – CS2 \quad \text{[External load capacitance on X2]}
\]

\[
CL1 = CLOAD1 – CIN1 – CS1 \quad \text{[External load capacitance on X1/CLK]}
\]

**Control and Select Pins**
The NB4N502 evaluation board is equipped with SMA connectors to control the static input logic levels of the Multiplier Select pins, S0 and S1 (see Table 2).

Pin S1 defaults to M when left open. Pin S0 defaults to H when left open.

3–Position slide switches are also provided to control the Multiplier Select pins. To use the switches, headers JMP3 and JMP4 must be shorted.
1. **Using the SMA Connectors**
   a. SMA connectors J3 and J4 (DUT.6 and DUT.7) should be pulled to VCC for logic level HIGH, pulled to GND for logic level LOW, and left OPEN for logic level M.

2. **Using the Slide Switches**
   a. Header pins JMP3 and JMP4 enable the slide switches for the clock multiplier select lines, S0 and S1, and should be jumpered.
   b. Switches SW3 (DUT.6) and SW4 (DUT.7) are used to select the clock multiplier value (see Table 2).
   c. The H position of the slide switch asserts a logic HIGH on the assigned pin, the L asserts a logic LOW and the M is an open where the pin “floats” to a mid-logic level by way of the device’s internal pullup and pulldown resistors.

<table>
<thead>
<tr>
<th>S1*</th>
<th>S0**</th>
<th>Multiplier</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>2X</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>5X</td>
</tr>
<tr>
<td>M</td>
<td>L</td>
<td>3X</td>
</tr>
<tr>
<td>M</td>
<td>H</td>
<td>3.33X</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>4X</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>2.5X</td>
</tr>
</tbody>
</table>

L = GND, H = VDD, M = OPEN (unconnected)
*Pin S1 defaults to M when left open
**Pin S0 defaults to H when left open

### Table 3. HEADER PIN CONDITIONS

<table>
<thead>
<tr>
<th>Header</th>
<th>Slide Switch Multiplier Control</th>
<th>SMA Multiplier Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>JMP1</td>
<td>Open</td>
<td>Open</td>
</tr>
<tr>
<td>JMP2</td>
<td>Open</td>
<td>Open</td>
</tr>
<tr>
<td>JMP3</td>
<td>Jumper (Short Pins)</td>
<td>Open</td>
</tr>
<tr>
<td>JMP4</td>
<td>Jumper (Short Pins)</td>
<td>Open</td>
</tr>
</tbody>
</table>

### Output Connections
Connect the CMOS/TTL outputs, REF and CLKOUT, to the oscilloscope.

### Table 4. OUTPUT CONNECTORS

<table>
<thead>
<tr>
<th>Outputs</th>
<th>Board Connector</th>
</tr>
</thead>
<tbody>
<tr>
<td>REF</td>
<td>J1 (DUT.4)</td>
</tr>
<tr>
<td>CLKOUT</td>
<td>J2 (DUT.5)</td>
</tr>
</tbody>
</table>

![Figure 4. NB3N502 Logic Diagram](http://onsemi.com)
Open Traces (Intentional) For Crystal Use

If using the slide switches instead of provided SMA connectors, short JMP3 and JMP4 (see Table 3).

Real Time Oscilloscope High-Z Probe

Table 5. PARTS LIST

<table>
<thead>
<tr>
<th>Ref. Number</th>
<th>Qty</th>
<th>Description</th>
<th>Manufacturer (Notes 1 and 2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
<td>1</td>
<td>Not populated</td>
<td></td>
</tr>
<tr>
<td>R2</td>
<td>1</td>
<td>Not populated</td>
<td></td>
</tr>
<tr>
<td>R3</td>
<td>1</td>
<td>Not populated</td>
<td></td>
</tr>
<tr>
<td>C1</td>
<td>1</td>
<td>Not populated</td>
<td></td>
</tr>
<tr>
<td>C2</td>
<td>1</td>
<td>Not populated</td>
<td></td>
</tr>
<tr>
<td>C9</td>
<td>1</td>
<td>22 μF ± 10%, Size &quot;C&quot; Tantalum Capacitor, T494C226K016AT</td>
<td>KEMET</td>
</tr>
<tr>
<td>C10</td>
<td>1</td>
<td>0.01 μF ± 10%, (0603), Ceramic Capacitors, 06035C103KAT2A</td>
<td>AVX</td>
</tr>
<tr>
<td>C11</td>
<td>1</td>
<td>0.1 μF ± 10%, (0603), Ceramic Capacitors, 06035C104KAT2A</td>
<td>AVX</td>
</tr>
<tr>
<td>Y1</td>
<td>1</td>
<td>25 MHz Crystal</td>
<td></td>
</tr>
<tr>
<td>U1</td>
<td>1</td>
<td>NB3N502, 8 pin SOIC (Pb–Free)</td>
<td>ON Semiconductor</td>
</tr>
<tr>
<td>SW1 – SW4</td>
<td>4</td>
<td>Slide Switches, 3 Position Miniature, OS103011MS8QP1</td>
<td>C&amp;K</td>
</tr>
<tr>
<td>J1 – J6</td>
<td>6</td>
<td>SMA Edge Mount Connectors, 142–0711–821</td>
<td>Johnson</td>
</tr>
<tr>
<td>JMP1–JMP4</td>
<td>4</td>
<td>Jumper Header, 100 mil, 2 pins, 1 row, SPC20485</td>
<td>SPC</td>
</tr>
<tr>
<td>VDD Plug</td>
<td>1</td>
<td>Banana Plug, Red, 571–0500</td>
<td>Deltron</td>
</tr>
<tr>
<td>GND Plug</td>
<td>1</td>
<td>Banana Plug, Black, 571–0100</td>
<td>Deltron</td>
</tr>
</tbody>
</table>

1. Specified parts are RoHS Compliant.
2. Only RoHS compliant parts may be substituted.
The evaluation board is constructed with Getek material with 50 Ω trace impedances and is designed to minimize noise, achieve high bandwidth and minimize crosstalk.

**Layer Stack**
- L1 Signal
- L2 Ground
- L3 \(V_{DD}\)
- L4 Signal

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**Figure 6. NB3N502 Evaluation Board Top (Component) Layer**

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**Figure 7. NB3N502 Evaluation Board SMA – Ground Layer**
Figure 8. NB3N502 Evaluation Board Power Layer

Figure 9. NB3N502 Evaluation Board Bottom Layer
Figure 10. NB3N502 Evaluation Board Top Assembly

Figure 11. NB3N502 Evaluation Board Bottom Assembly
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