AND9291/D

Boot Mode Configuration of LC823450 Series for Audio Applications

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APPLICATION NOTE

Introduction

This application note describes the procedure to determine boot device, boot mode and how to control boot mode during development phase.

Intended audience is customers who are building audio application using LC823450 Series (called LC823450 hereafter).

BACkGROUND

Boot mode

LC823450 has fifteen Boot modes (refer to Appendix A) which enable to boot from five kinds of devices described in Table 1 and update user program in the boot devices from two update means described in Figure 1. LC823450 boot code in internal ROM can recognize these boot modes by using pull-up and pull-down registor on BMODE[1:0] as described in Table 2.

Table 1. Boot device

Boot device	device operation mode
eMMC	Boot Partition
	User Area
Serial Flash	SPI (1-bit bus)
	QSPI (4-bit bus)
External ROM (Parallel ROM, Flash, etc)	16-bit bus

Figure 1. update device

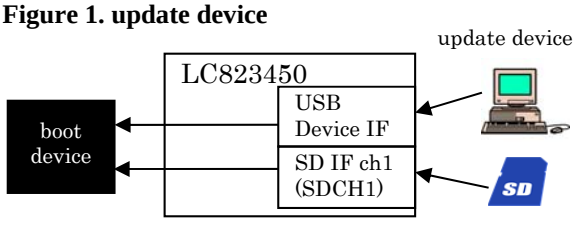

Table 2. BMODE[1:0] input options

BMODE1	PD 470 kΩ	PU 470 kΩ	PD 1 kΩ	PU 1 kΩ
BMODE0	PD 470 kΩ	PU 470 kΩ	PD 1 kΩ	PU 1 kΩ

PU means pull-up the BMODE terminal to power supply through resistor.
PD means pull-down the BMODE terminal to GND through resistor.

If customers select Serial Flash as boot device, Serial Flash can be used on SPI Boot or QSPI Boot of LC823450 is limited (refer to Appendix B). Because the Communication protocol for serial Flash had been stored in internal ROM of LC823450 in advance in order that the Initial Program Loader (IPL) in internal ROM retrieves a program from the boot device just after hardware reset.

Some boot mode names in Appendix A consist of prefix which expresses boot device, and suffix which expresses update device. For example, we can understand “eMMC Physical Boot USB” mode uses Boot Partition of eMMC as boot device and USB Device as update device.

Some boot mode which names have “Delete” or “Erase” are used to force to delete or erase the valid user programs in the boot device to be update after this operation.

The remaining is “External memory IF terminal release” which is used to write user program in the boot device on board by forcing LC823450 terminals to hi-impedance to enable some equipments to control the signals of the boot device and write user program to the boot device directly.

Boot sequence

Our sample application for LC823450 has been adopted multi stage boot system except for the case of using QSPI mode with Serial Flash or External ROM Boot mode.

The Initial Program Loader (IPL) is implemented in internal ROM of LC823450, and it retrieves IPL2 from the boot device based on the BMODE[1:0] status just after hardware reset. If IPL finds the valid IPL2 in the boot device, IPL loads IPL2 to internal SRAM and jumps to start address of IPL2. If IPL can’t find the valid IPL2 in the boot device, IPL becomes the write mode. IPL checks the update device and tries to transfer IPL2 in the update device to the boot device.

After IPL2 is loaded to internal SRAM, IPL2 usually needs to load additional application program into internal SRAM because maximum size of IPL2 is only 128 kByte. Then, the IPL2 retrieves application program from the boot device, and downloads it into internal SRAM.

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Finally, application program is executed from internal SRAM.

In the QSPI mode with Serial Flash, IPL jumps to Serial Flash memory connected to S-Flash IF by direct fetch.

In the External ROM Boot mode, IPL jumps to External memory connected to external memory controller by direct fetch.

DETERMINE BOOT DEVICE/MODE

determine boot device

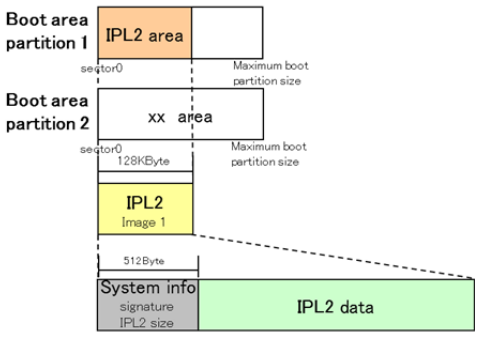
Typical audio product has eMMC built-in and uses it as a storage device of music contents. LC823450 has the function to store some programs to eMMC in addition to music contents. This function contributes to low cost due to no requirement of additional non-volatile memory to store program.

Especially, if cunstomers use eMMC supporting physical boot mode, it is possible to use “eMMC Physical Boot” mode, and otherwise, “User Area Boot” mode. In “eMMC Physical Boot” mode, LC823450 can offer to store some programs to hidden area of eMMC in addition to music contents in visible area that end users can see.

On the other hand, if the product doesn’t have eMMC built-in, customers may use Serial Flash or Parallel ROM (or other non-volatile memory).

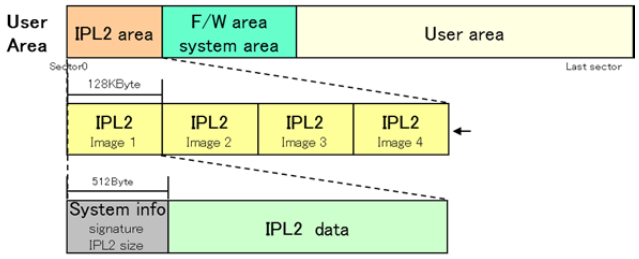
Storage area of “eMMC Physical Boot” is decsribed in Figure 2. The maximum code size of IPL2 is 127.5 kByte + 512 Byte, and IPL2 is placed from the start address of Partition 1. Partition 2 can be used for other purpose, not used for boot.

Figure 2. eMMC Physical boot layout



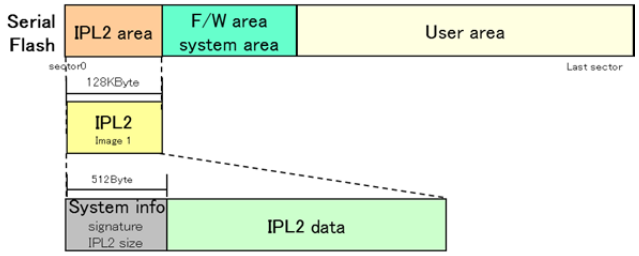
Storage area of “eMMC User Area” is described in Figure 3. The maximum code size of IPL2 is 127.5 kByte + 512 Byte, but IPL2 is placed by repetition four times from the start address of User Area. Four same images of IPL2 enable IPL to retry three times against IPL2 corruption.

Figure 3. eMMC User Area boot layout



Storage area of Serial Flash is described in Figure 4. The maximum code size of IPL2 is 127.5 kByte + 512 Byte, and IPL2 is placed from the start address of Serial Flash.

Figure 4. Serial Flash boot layout



determine update device

Typical audio product has USB device interface, and we recommend to use it to update user program to boot device. If product doesn’t support USB device interface, customers can use SD Card as the update device through SD IF ch1 (SDCH1). LC823450 offers these two update devices in all boot device except “External ROM Boot” mode.

CONTROL BOOT MODE

boot mode control

In application development phase, customers need to update user program many times. The control of BMODE[1:0] is required to update the valid IPL2 in boot device because IPL cannot enter update process if the valid IPL2 exists in the boot device.

In this case, at first customers need to delete (or erase) the current IPL2 in boot device. The boot modes (delete/erase mode) described in Table 3 are used to delete or erase contents in the boot device corresponding to the boot device operation mode.

Table 3. boot mode (delete/erase mode)

device	device operation mode	device delete/erase mode
eMMC	Boot Partition	Partition Delete or SDCH0 All Erase
	User Area	User Area Delete or SDCH0 All Erase
Serial Flash	SPI	S-Flash SPI All Erase
	QSPI	S-Flash QSPI All Erase
Parallel ROM, Flash, etc	16 bit bus	N/A

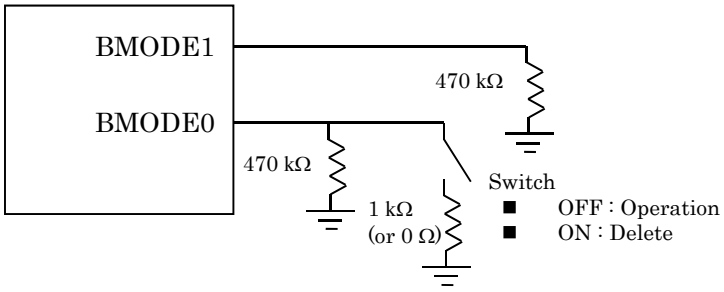
For example, in the “eMMC Physical Boot USB” mode BMODE1 and BMODE0 must be configured as PD 470 kΩ and PD 470 kΩ for device operation mode, and PD 470 kΩ and PD 1 kΩ for delete mode as described in Table 4. In development phase, customers need to change configuration of BMODE1 and BMODE0 between these two modes to update program including IPL2 in boot device.

Table 4. BMODE resistor (example)

device	device operation mode device delete/erase mode	BMODE1 BMODE0
eMMC	Boot Partition USB	PD 470 kΩ PD 470 kΩ
	Partition Delete	PD 470 kΩ PD 1 kΩ

We suggest customers to design the inputs of BMODE1 and BMODE0 terminal as described in Figure 4 on evaluation board so that customers can change between two modes easily.

Figure 4. BMODE board design (example)



Appendix A

BMODE[1]	BMODE[0]	Boot mode	Function
PD470 kΩ	PU1 kΩ	S-Flash SPI Boot SD	IPL loads IPL2 to internal SRAM from Serial Flash memory (S-Flash) connected to S-Flash IF, and jump to IPL2. IPL supports program write function to S-Flash from SDCH1.
PD470 kΩ	PU470 kΩ	eMMC Physical Boot SD * boot area partiton1	IPL loads IPL2 to internal SRAM from boot area partition1 of eMMC connected to SDCH0, and jump to IPL2. IPL supports program write function to boot area partition1 from SDCH1.
PD470 kΩ	PD470 kΩ	eMMC Physical Boot USB * boot area partiton1	IPL loads IPL2 to internal SRAM from boot area partition1 of eMMC connected to SDCH0, and jump to IPL2. IPL supports program write function to boot area partition1 from USB device. XT1 is required for this mode.
PD470 kΩ	PD1 kΩ	Partition Delete	IPL deletes boot area partiton1. After boot mode operation, IPL can write IPL2 again at next eMMC Physical Boot.
PU1 kΩ	PU1 kΩ	External memory IF terminal release	IPL forces the terminals of External memory controller, SDCH0 and S-Flash IF to Hiz state. XT1 and XTRTC are dispensable for the boot.
PU1 kΩ	PU470 kΩ	S-Flash QSPI Boot USB	IPL jumps to Serial Flash memory (S-Flash) connected to S-Flash IF by direct fetch. IPL supports program direct write function by using DD commands to S-Flash from USB device. XT1 is required for this mode.
PU1 kΩ	PD470 kΩ	S-Flash QSPI Boot SD	IPL jumps to Serial Flash memory (S-Flash) connected to S-Flash IF by direct fetch. IPL supports program write function to S-Flash from SDCH1.
PU1 kΩ	PD1 kΩ	S-Flash QSPI All Erase	IPL deletes Serial Flash data. In case of QSPI device, this mode should be used.
PU470 kΩ	PU1 kΩ	S-Flash SPI All Erase	IPL deletes Serial Flash data. In case of SPI device, this mode should be used.
PU470 kΩ	PU470 kΩ	S-Flash SPI Boot USB	IPL loads IPL2 to internal SRAM from Serial Flash memory (S-Flash) connected to S-Flash IF, and jump to IPL2. IPL supports program write function to S-Flash from USB device. XT1 is required for this mode.
PU470 kΩ	PD470 kΩ	External ROM Boot	IPL jumps to memory by direct fetch connected to external memory controller mapped to external memory0 area. XT1 and XTRTC are dispensable for the boot.
PU470 kΩ	PD1 kΩ	User Area Boot SD * User Area	IPL loads IPL2 to internal SRAM from user area of eMMC connected to SDCH0, and jump to IPL2. IPL supports program write function to boot area partition1 from SDCH1.
PD1 kΩ	PU1 kΩ	User Area Delete	IPL deletes User Area. After this boot mode operation, IPL can write IPL2 again at next User Area Boot.
PD1 kΩ	PU470 kΩ PD470 kΩ	User Area Boot USB * User Area	IPL loads IPL2 to internal SRAM from User Area of eMMC connected to SDCH0, and jump to IPL2. IPL supports program write function to User Area from USB device. XT1 is required for this mode.
PD1 kΩ	PD1 kΩ	SDCH0 All Erase	IPL deletes eMMC data. In case of eMMC, partiton area will be deleted, too. This operation takes much time to be completed.

PU means pull-up the BMODE terminal to power supply through resistor.
PD means pull-down the BMODE terminal to GND through resistor.

Appendix B

Manufacturer	Part number	Voltage	Capacity	Boot mode
Macronix	MX25L8036E	3 V	1 MByte	SPI/QSPI
Macronix	MX25L1633E	3 V	2 MByte	SPI/QSPI
Macronix	MX25L1635D	3 V	2 MByte	SPI/QSPI
Macronix	MX25L1636E	3 V	2 MByte	SPI/QSPI
Macronix	MX25L1673E	3 V	2 MByte	SPI/QSPI
Macronix	MX25L3235E	3 V	4 MByte	SPI/QSPI
Macronix	MX25L6435E	3 V	8 MByte	SPI/QSPI
Macronix	MX25L12835F	3 V	16 MByte	SPI/QSPI
Macronix	MX25U2033E	1.8V	256 kByte	SPI/QSPI
Macronix	MX25U4033E	1.8V	512 kByte	SPI/QSPI
Macronix	MX25U8035E	1.8V	1 MByte	SPI/QSPI
Macronix	MX25U1635E	1.8V	2 MByte	SPI/QSPI
Macronix	MX25U3235F	1.8V	4 MByte	SPI/QSPI
Macronix	MX25U6435F	1.8V	8 MByte	SPI/QSPI
Macronix	MX25U12835F	1.8V	16 MByte	SPI/QSPI
Winbond	W25Q20CL	3 V	256 kByte	SPI/QSPI
Winbond	W25Q40CL	3 V	512 kByte	SPI/QSPI
Winbond	W25Q80DV	3 V	1 MByte	SPI/QSPI
Winbond	W25Q16DV	3 V	2 MByte	SPI/QSPI
Winbond	W25Q32FV	3 V	4 MByte	SPI/QSPI
Winbond	W25Q64FV	3 V	8 MByte	SPI/QSPI
Winbond	W25Q128FV	3 V	16 MByte	SPI/QSPI
Winbond	W25Q20BW	1.8V	256 kByte	SPI
Winbond	W25Q40BW	1.8V	512 kByte	SPI/QSPI
Winbond	W25Q80BW	1.8V	1 MByte	SPI/QSPI
Winbond	W25Q16DW	1.8V	2 MByte	SPI/QSPI
Winbond	W25Q64FW	1.8V	8 MByte	SPI/QSPI
Winbond	W25Q128FW	1.8V	16 MByte	SPI/QSPI

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