

## Board Mounting Notes for NIS6111 Leadless Package (QFN)

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### APPLICATION NOTE

#### Introduction

Various ON Semiconductor components are packaged in an advanced Quad Flat-Pack No-Lead Package (QFN) or commonly referred to as a Leadless Package. Because the QFN (Leadless) platform represent the latest in surface mount packaging technology, it is important that the design of the Printed Circuit Board (PCB), as well as the assembly process, follow the suggested guidelines outlined in this document.

#### NIS6111 Package Overview

The QFN platform offers a versatility, which allows either a single or multiple semiconductor devices to be connected together within a leadless package.

In this case the NIS6111 Package contains multiple semiconductor devices within one package. This package style was chosen due to its excellent thermal dissipation and reduced electrical parasitics.

When surface mounting this package onto a PCB, two critical issues must be considered:

1. Printed Circuit Board Design
2. Board Mounting Process.

This document will address both of these critical issues.

#### Printed Circuit Board Design Considerations

##### SMD and NSMD Pad Configurations

There are two different types of PCB pad configurations commonly used for surface mount leadless QFN style packages. These different I/O configurations are:

1. Non-Solder Masked Defined (NSMD)
2. Solder Masked Defined (SMD).

As their titles describe, the NSMD contact pads have the solder mask pulled away from the solderable metallization,

while the SMD pads have the solder mask over the edge of the metallization, as shown in Figure 1. With the SMD Pads, the solder mask restricts the flow of solder paste on the top of the metallization which prevents the solder from flowing along the side of the metal pad. This is different from the NSMD configuration where the solder will flow around both the top and the sides of the metallization.

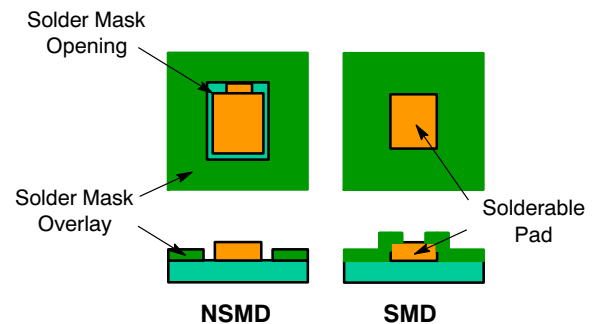


Figure 1. Comparison of NSMD vs. SMD Pads

Typically, the NSMD pads are preferred over the SMD configuration since defining the location and size of the copper pad is easier to control than the solder mask. This is based on the fact that the copper etching process is capable of a tighter tolerance than the solder masking process.

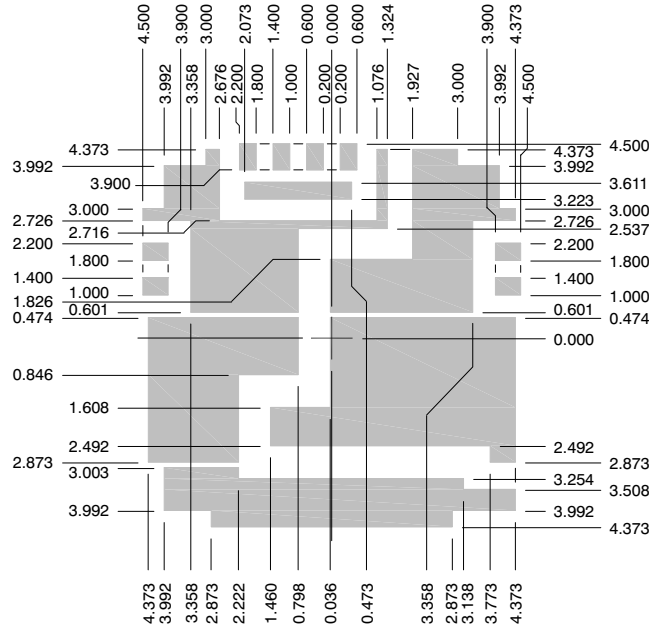
In addition, the SMD pads will inherently create a stress concentration point where the solder wets to the pad on top of the lead. This stress concentration point is eliminated when the solder is allowed to flow down the sides of the leads in the NSMD configuration.

**NSMD Pad Configurations**

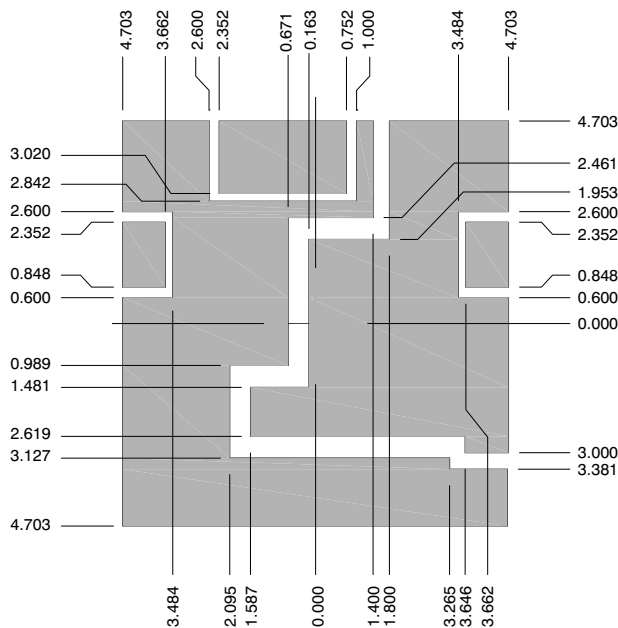
When dimensionally possible, the solder mask should be located at least a  $\pm 0.076$  mm (0.003 in) away from the edge of the solderable pad. This spacing is used to compensate for the registration tolerances of the solder mask, as well as to insure that the solder is not inhibited by the mask as it reflows along the sides of the metal pad.

The dimensions of the recommended solder stencil, copper area and solder mask are shown in Figures 2, 3,

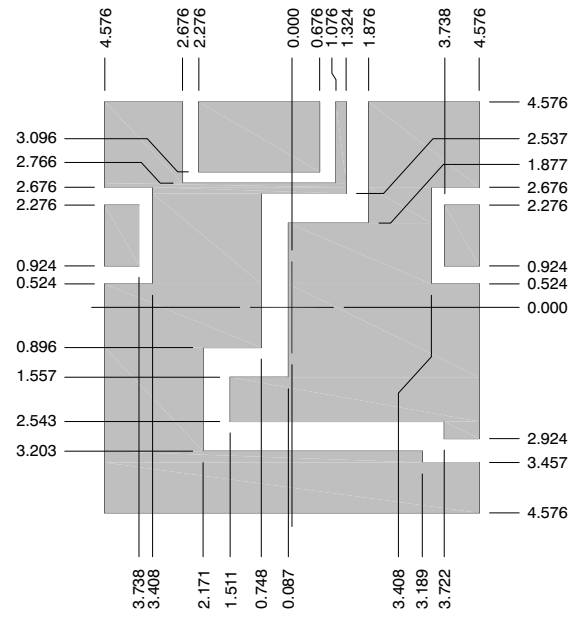
and 4. PCB's solderable pads should match those of the pads on the package as shown in Figures 3 and 4. Please note that NIS6111 footprint shows smaller exposed pad openings compared with the recommended PCB layout. Die attach pads on the footprint were divided into smaller exposed pads to help reduce the risk of solder voiding during surface mounting to the package



**Figure 2. Solder Paste Stencil**



**Figure 3. NIS6111 PCB Footprint**



**Figure 4. NIS6111 Solder Mask Pattern**

### Thermal/Electrical Vias

If vias are to be used on the pad area they should be placed on the larger die attach pads to improve electrical and thermal performance. If vias are required on the larger die attach pads, our recommendation is to use filled-vias. Filled-vias will help prevent the solder from flowing down into the holes, thereby reducing the solder volume required for the solder joint of this die attach pad. Filled-vias are normally filled with some type of conductive epoxy.

If through-hole vias are used, we recommend that the via size be less than or equal to 0.25 mm (10 mils). The number of vias placed over the die attach pad is also critical and should not exceed 25% of the total exposed area of the copper pattern. In other words, excessive through-hole vias will allow the solder to flow down into the via and thereby decrease the solder volume needed to have a sufficient solder joint.

### NIS6111 Board Mounting Process

The board mounting process is optimized by first defining and controlling the following processes:

1. Creating and maintaining a solderable metallization on the PCB contacts
2. Choosing the proper solder paste
3. Screening/stenciling the solder paste onto the PCB
4. Placing the package onto the PCB
5. Reflowing the solder paste
6. Final solder joint inspection.

Recommendations for each of these processes are located below.

### PCB Solderable Metallization

There are two common plated solderable metallizations, which are used for PCB surface mount devices. In either case, it is imperative that the plating is uniform, conforming, and free of impurities to insure a consistent solderable system.

The first metallization consists of an Organic Solderability Preservative (OSP) coating over the copper plated pad. The organic coating assists in reducing oxidation in order to preserve the copper metallization for soldering.

The second recommended solderable metallization consists of plated electroless nickel over the copper pad, followed by immersion gold. The thickness of the electroless nickel layer is determined by the allowable internal material stresses and the temperature excursions the board will be subjected to throughout its lifetime. Even though the gold metallization is typically a self-limiting process, the thickness should be at least 0.05 mm thick, and not consist of more than 5% of the overall solder volume. Having excessive gold in the solder joint can create gold embitterment which may affect the reliability of the joint.

### Solder Type

Solder paste such as Cookson Electronics' WS3060 with a Type 3 or smaller sphere size is recommended. The WS3060 has a water-soluble flux for cleaning. Cookson Electronics' PNC0106A can be used if a no-clean flux is preferred.

### Solder Screening onto the PCB

Stencil screening the solder onto the PCB board is commonly used in the industry. The recommended stencil thickness to be used is 0.075 mm (0.003 in) and the sidewalls of the stencil openings should be tapered approximately 5 degrees to facilitate the release of the paste when the stencil is removed from the PCB. Note: 0.127 mm (0.005 in) thick stencil may be used also, but will require smaller stencil openings to reduce the amount of solder applied to equal the amount of solder applied using the 0.075 mm thick stencil.

For a typical edge PCB terminal pad, the stencil opening should be the same size as the pad size on the package. However, in cases where the die pad is soldered to the PCB, the stencil opening must be divided into smaller openings as shown in Figure 4. Dividing the larger die pads into smaller screen openings reduces the risk of solder voiding and allows the solder joints for the smaller terminal pads to be at the same height as the larger ones.

### Package Placement onto the PCB

Pick and place equipment with the standard tolerance of  $\pm 0.05$  mm or better is recommended. The package will tend to center itself and correct for slight placement errors during the reflow process due to the surface tension of the solder.

### Solder Reflow

Once the package is placed on the PCB along with the solder paste, a standard surface mount reflow process can be used to mount the part. Figure 5 is an example of a standard reflow profile. The exact profile will be determined, and is available, by the manufacture of the paste since the chemistry and viscosity of the flux matrix will vary. These variations will require small changes in the profile in order to achieve an optimized process.

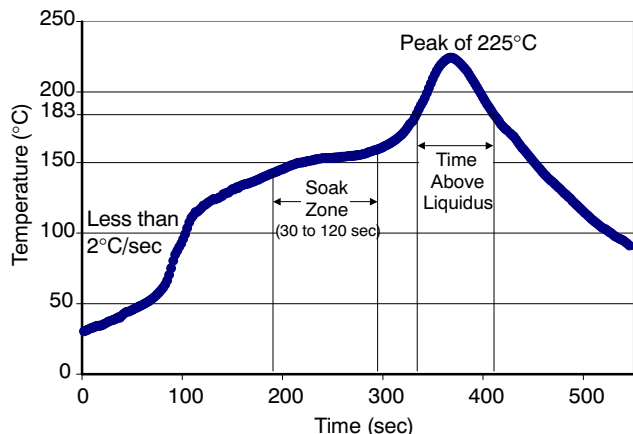


Figure 5. Typical reflow profile for eutectic tin/lead solder.

In general, the temperature of the part should be raised not more than 2°C/sec during the initial stages of the reflow profile. The soak zone then occurs when the part is approximately 150°C and should last for 30 to 120 seconds. Typically, extending the time in the soak zone will reduce the risk of voiding within the solder. The temperature is then raised and will be above the liquidus of the solder for 30 to 100 seconds depending on the mass of the board. The peak temperature of the profile should be between 205 and 225°C for eutectic Sn/Pb solder.

If required, removal of the residual solder flux can be completed by using the recommended procedures set forth by the flux manufacturer.

### Final Solder Inspection

The inspection of the solder joints is commonly performed with the use of an X-ray inspection system. With this tool, one can locate defects such as shorts between pads, open contacts, voids within the solder as well as any extraneous solder.

In addition to searching for defects, the mounted device should be rotated on its side to inspect the sides of the solder joints with an X-ray inspection system. The solder joints

Standard SMT rework systems are recommended for this procedure since the airflow and temperature gradients can be carefully controlled. It is also recommend that the PC board be placed in an oven at 125°C for 4 to 8 hours prior to heating the parts to remove excess moisture from the packages. In order to control the region, which will be exposed to reflow temperatures, the board should be heated to a 100°C by conduction through the backside of the board in the location of the NIS6111 QFN Package. Typically, heating nozzles are then used to increase the temperature locally.

Once the NIS6111's solder joints are heated above their liquidus temperature, the package is quickly removed and the pads on the PC board are cleaned. The cleaning of the pads is typically performed with a blade-style conductive tool with a de-soldering braid. A no clean flux is used during this process in order to simplify the procedure.

Solder paste is then deposited or screened onto the site in preparation of mounting a new device. Due to the close proximity of the neighboring packages in most PC board configurations, a miniature stencil for the individual

should have enough solder volume with the proper stand-off height so that an "Hour Glass" shaped connection is not formed as shown in Figure 6. "Hour Glass" solder joints are a reliability concern and must be avoided.

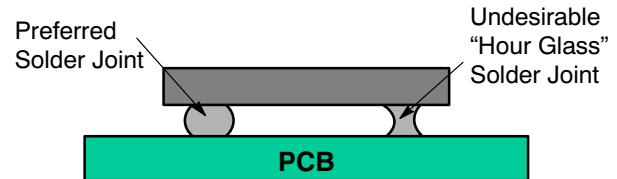


Figure 6. Side view of NIS6111 illustrating preferred and undesirable solder joints.


### Rework Procedure

Due to the fact that the NIS6111 is a leadless device, the entire package must be removed from the PC board if there is an issue with the solder joints. It is important to minimize the chance of overheating neighboring devices during the removal of the package since the devices are typically in close proximity with each other.

component is typically required. The same stencil design that was originally used to mount the package can be applied to the mini-stencil for redressing the pad.

Due to the small pad configurations of the NIS6111, and since the pads are on the underside of the package, a manual pick and place procedure without the aid of magnification is not recommended. A dual image optical system where the underside of the package can be aligned to the PC board should be used instead.

Reflowing the component onto the board can be accomplished by either passing the board through the original reflow profile, or by selectively heating the NIS6111 package with the same process that was used to remove it. The benefit with subjecting the entire board to a second reflow is that the packages will be mounted consistently and by a profile that is already defined. The disadvantage is that all of the other devices mounted with the same solder type will be reflowed for a second time. If subjecting all of the parts to a second is either a concern or unacceptable for a specific application, than the localized reflow option would be the recommended procedure.

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