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# Understanding Challenges in Powering High Resolution, High Frame Rate CMOS Image Sensors

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# Understanding Challenges in Powering High Resolution, High Frame Rate CMOS Image Sensors

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## Abstract

Understanding critical challenges in powering today's high resolution, high frame rate CMOS image sensors are the key elements in proposing an optimized power system solution with LDO (DC−DC, PMIC) that can meet the requirements of every design engineer. Power system designers need to know how different the power solution is for, let's say, an 8−megapixel (MP) versus a 50−MP camera, or how the frame rate (30 fps, 60 fps, 120 fps) changes their power design, what are the frequencies that need high PSRR, etc. This paper intends to highlight essential considerations before identifying a solution to power any of today's image sensors.

## Introduction

Any CMOS imaging system consists of an active pixel area and photodetector sections that capture photons and convert them into a very small photocurrent or electrons. Different sections read out the data, including ADC, analog signal processing, user interface digital logic, timing, etc. The small amount of photodiode current in the Femto amp range is integrated during the exposure time (opening of the shutter) into a small amount of charge converted to a readable voltage by the ADC.

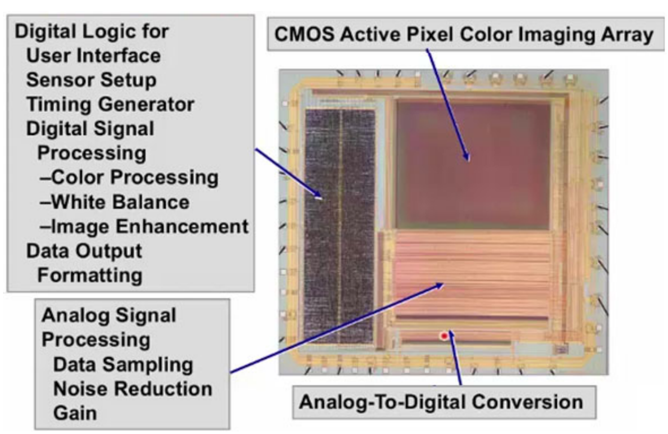


**Figure 1. Typical CMOS Imager Construction**

## Pixels, Resolution & Transistor Design

Each pixel also has a fill factor that depends on the percentage of the total pixel area used and has two sections, photosensitive and non−photosensitive sections. The Photosensitive area captures light versus the non−photosensitive area used for ADC, digital blocks, interfaces, and other functions.

The remaining areas are used for horizontal or vertical readout where a typical READ or WRITE sequence begins by the master, which generates a start condition on the bus.

The resolution for CMOS image sensors is the total number of pixels array made up of many columns and rows. For example, a typical 2 MP camera can have a pixel array of 1600 x 1200.

| Camera Megapixels | Horizontal Pixels | Vertical Pixels | Total # of pixels | Apect Ratio |
|---|---|---|---|---|
| 1.3 MPix | 1280 | 1080 | 1382400 | 1.19 |
| 2.0 MPix | 1600 | 1200 | 1920000 | 1.33 |
| 2.0 MPix | 2048 | 1080 | 2211840 | 1.90 |
| 3.0 Mpix | 2048 | 1536 | 3145728 | 1.33 |
| 4.0 Mpix | 2560 | 1600 | 4096000 | 1.60 |
| 5.0 Mpix | 2560 | 1920 | 4915200 | 1.33 |
| 8.0 Mpix | 3264 | 2448 | 7990272 | 1.33 |
| 8.0 Mpix | 4096 | 2160 | 8847360 | 1.90 |
| 8.0 Mpix | 3840 | 2160 | 8294400 | 1.78 |
| 10 Mpix | 3704 | 2778 | 10289712 | 1.33 |
| 10 Mpix | 3704 | 2778 | 10289712 | 1.33 |
| 13 Mpix | 4208 | 3120 | 13128960 | 1.35 |
| 45 Mpix | 8256 | 5504 | 45441024 | 1.50 |
| 31 Mpix | 6464 | 4852 | 31363328 | 1.33 |

**Figure 2. List of Common Cameras**

Some of the pixels on both columns and rows are called dark pixels that are optically black, used internally for black level correction or row noise correction, which cause a reduction in the actual active pixel array or the actual effective pixels used in the array.

Many different pixel transistor designs (3T, 4T, 5T) are available, like the four−transistor (4T) pixel design shown below. The photodiode transforms the photon received to a tiny amount of charge with some switches for selecting different columns and rows. To not upset the photodiode readings, a high impedance amplifier on the photodiode junction is used as a source follower amplifier (TIA/SF Amp) to drive each column bus.

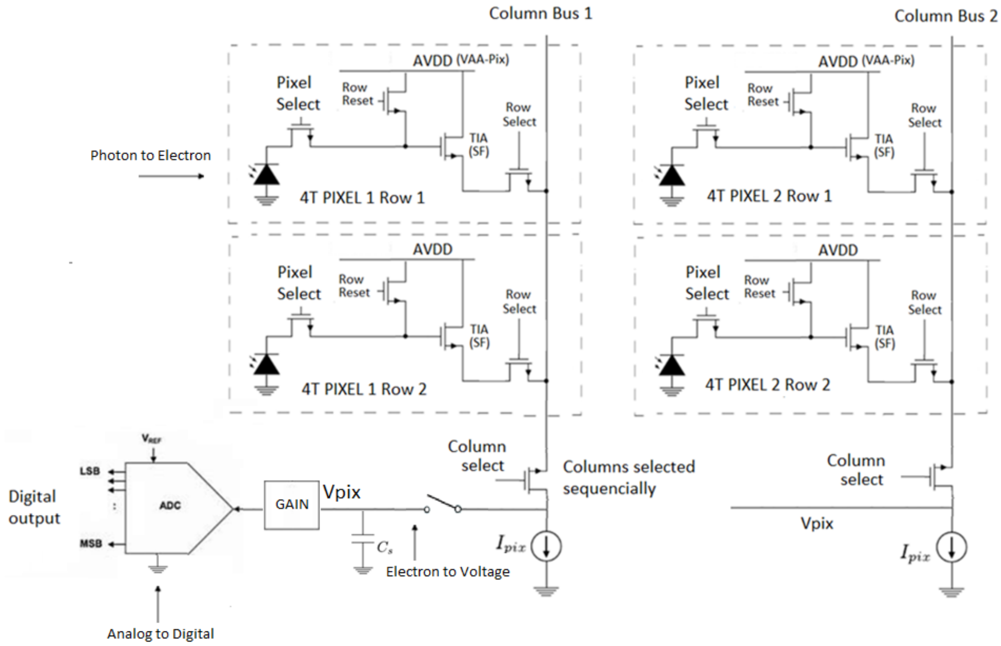


**Figure 3. Example of a 4 Transistor Design**

Each pixel voltage is read out one row at a time and placed into the column capacitors (Cs), followed by a readout using the column decoder and multiplexer.

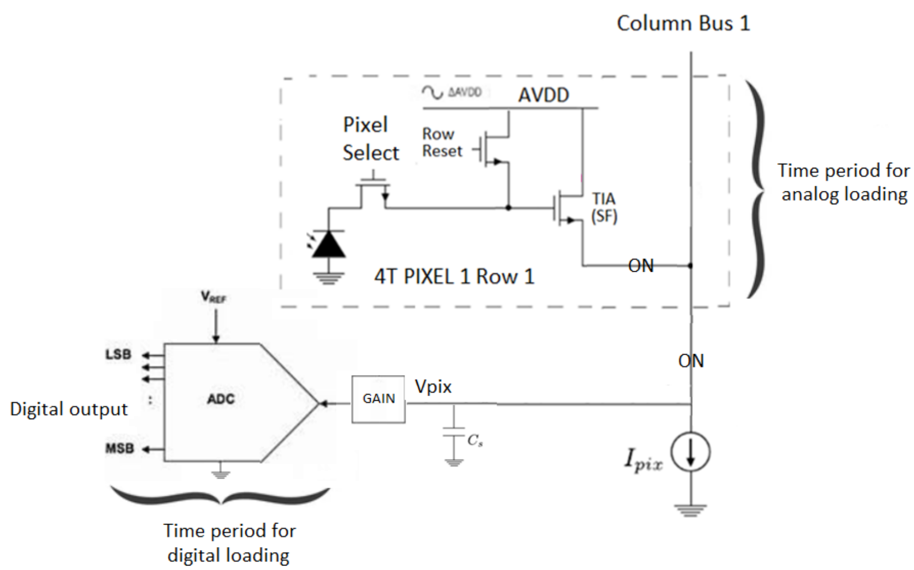


**Figure 4. Example of Selected Row and a Column**

## Frame and Row Transitions

Frame rate measures the speed at which a complete image can be captured and readout of the array for processing, occurring at a typical 30−120 Hz frequency range. The image sensor can be a high frame rate device (>60 fps) for slow−motion playback or a low frame rate device (<60 fps) for motion−blur effects.

The rate can also be limited or affected by the shutter speed, which controls how long the image sensor can collect the light, or the programmable time interval called ‘dark period’ that occurs after the last line is used for horizontal blanking, sync time, or other purposes.

We can calculate the frequency for the highest PSRR needed for a given frame rate (15, 30, or 60)—for example, a 4 MP camera—and design an LDO with the required PSRR for the calculated frequency.

Horizontal row frequency vs needed PSRR frequency

| Camera Mega Pixel (Mpixel) | Horizantal | Vertical | Frames per second | Horizontal Row freq (KHz) |
|---|---|---|---|---|
| 4 | 2560 | 1600 | 15 | 240 |
| Camera Mega Pixel (Mpixel) | Horizantal | Vertical | Frames per second | Horizontal Row freq (KHz) |
| 4 | 2560 | 1600 | 30 | 480 |
| Camera Mega Pixel (Mpixel) | Horizantal | Vertical | Frames per second | Horizontal Row freq (KHz) |
| 4 | 2560 | 1600 | 60 | 960 |

**Figure 5. Effect of Different Frame Rates Versus Horizontal Frequency**

Frame rate is about 75% of the readout rate and another 25% as spare time for other processing like changing the aperture, exposure time calculation, lens AF, image processing, memory write speeds, etc. Frame readout proceeds in a row−sequential fashion for both stills and video, and at the end, the entire frame is gathered in the buffer and presented as a completed image.

## Image Sensor Power Rails

CMOS image sensors typically require three different power rails to power the analog rails (AVDD), interface (DOVDD), and digital rails (DVDD). The standard voltage used for the analog power rail is 2.8 V, the interface power rail is 2.8 V or 1.8 V, and the digital power rail is 1.8 V or 1.2 V.

To improve the noise performance of CMOS image sensors, we can place a large bypass capacitor in front of the voltage supply pins. Decreasing the fluctuation of each power rail can also improve the noise performance of CMOS image sensors. Generally, the analog power rail is the most noise−sensitive rail, followed by the digital rail, which is also sensitive to noise.

## Power Supply Rejection Ratio (PSRR)

The PSRR provides a measure of how well an LDO can reject ripple or how to block noise produced by the supply rail only at the input of the LDO. The higher the PSRR, the more noise or ripple can be blocked from the power supply. These sources of ripples can come either from input supply with 50/60 Hz ripple, switching frequency of a DC−DC, or ripple due to the sharing of an input supply between different circuits.

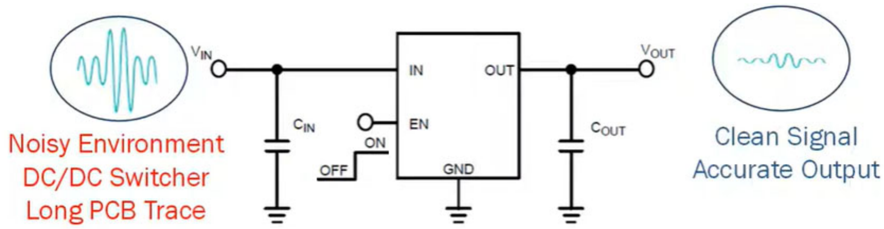


**Figure 6. Example of Noise From Input to Output of an LDO**

The LDO’s feedback loop usually controls the PSRR of the system for frequencies less than 100 kHz, so make sure a proper LDO is selected. For frequencies above 100 kHz, an appropriate selection of passive components and PCB layout/placement controls the PSRR.

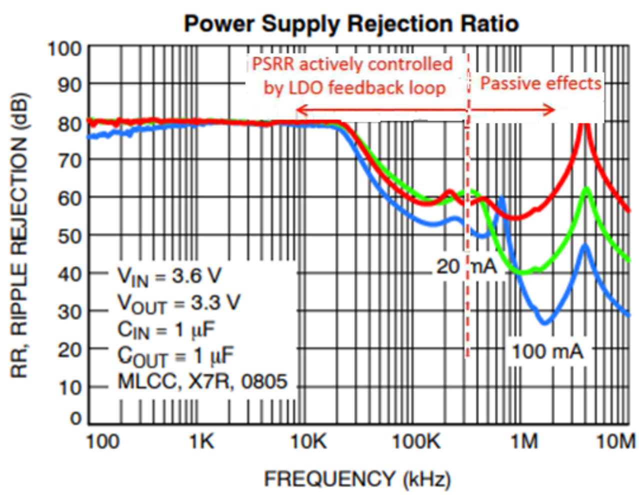


**Figure 7. Typical LDO’s PSRR Behavior Versus Frequency**

Attention should be taken when designing the PCB to allow tight current loops to reduce parasitic inductances and the ripples in between the power rails and the camera rails.

Using a clean bias rail or a higher headroom between Vin and Vo can also increase the PSRR performance capability.

A low PSRR performance or any noise on the analog rail can cause the noise on the power rails to enter the output signal path through the high−gain source follower amplifier circuit, causing an unwanted horizontal ripple to be present in the captured image.

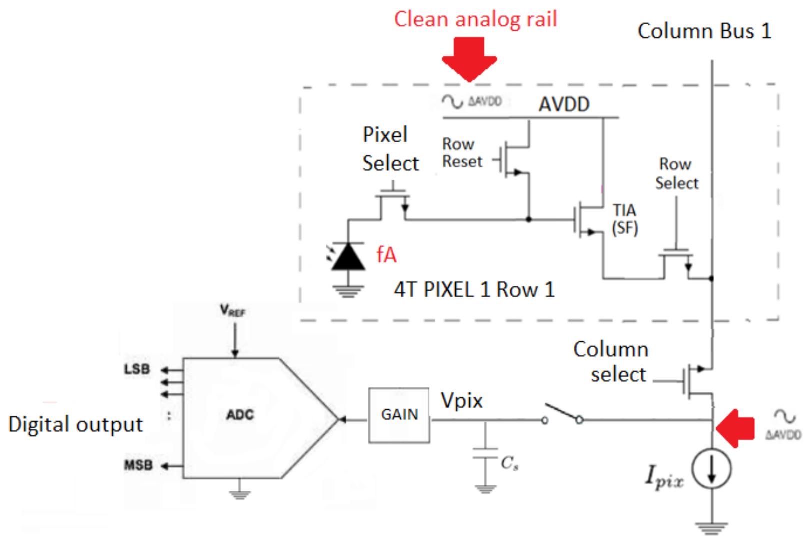


**Figure 8. Example of Any Noise on the Analog Rail**

Normal LDOs have low PSRR at high frequencies, which should be adequate for a standard camera, but with a high resolution and high frame rate image sensor in the range of 50−200 MP, there is a definite need for a specific series of LDOs with high PSRR greater than 90 dB at lower frequency range (up to 10 kHz) and greater than 45 dB at 1−3 MHz frequency range to reduce the ripples during both frame and row rate transitions.

## Sensor Frame and Row Rate Versus Power Supply Loading

It is important to note that both the frame rate (30−120 fps) and the row rate (22−44 kHz) can cause a dynamic load for the image sensor that creates both undershoot and overshoot on the analog rails 2.8 V.

The current draw appears like a step load during each new frame or new row transition. For example, during a frame or row read, or between each frame or row read, the power solution (LDO) needs to handle a few hundreds of mA load changes during each frame and row transition without any substantial fluctuation on its output voltage rails.

For camera decoupling, bulk capacitors with the lowest impedance around row and frame frequencies are desired for optimum system performance.

## LDO Output Noise (μVRMS)

Depending on the image sensor design, each pixel has a charge saturation level or a full well capacity—the amount of charge a pixel can hold before saturating (measured in electrons). For any image sensor, the dynamic range (dB) specifies the brightest and darkest parts of an image that can be captured simultaneously.

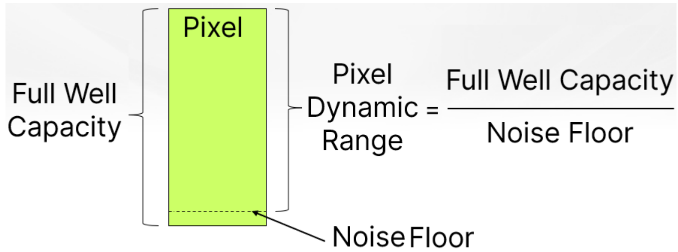


**Figure 9. Pixel Capacity and Noise Floor Example**

At the output of any LDO, the lower the spectral noise density between 10 Hz to 1 MHz plays a significant role in transferring less noise into the CMOS image sensor, allowing a higher dynamic range for a given pixel.

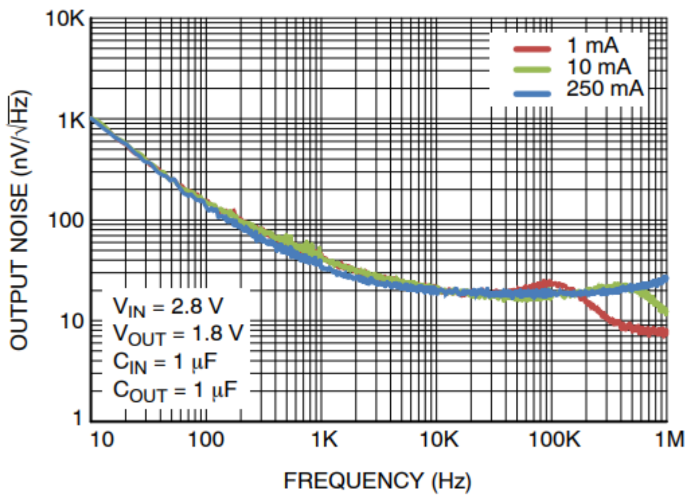


**Figure 10. Typical LDO Output Noise Density**

It is crucial to find the CMOS image sensor's SNR information and design the system so the overall ripple and noise are at least 40 dB lower than the sensor noise threshold.

## Conclusion

There are many issues and differences when designing an LDO power solution for a 4 MP versus 40 MP image sensor, 30 fps versus 120 fps frame rate, or a high dynamic range versus low dynamic range sensor, and more. We can drive the max allowable frame rate for a high−resolution camera from the max ISP Gbps capability and the number of C/D−PHY MIPI lanes used. Considering both the combination of the highest PSRR needed for a calculated highest frame rate frequency plus the RMS noise density required for a given image sensor with a known SNR can help us design an optimized power system to meet the requirements for today's high resolution and high−frame−rate CMOS image sensors.

Using an LDO solution with high PSRR at higher frequencies, low RMS noise, and proper passives with a specific impedance at a given vertical and horizontal frequencies can help to improve the overall noise performance of a CMOS image sensor and reduce the ripple of power supply that can cause an undesired horizontal ripple on the captured images.

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