NCP1680 – CrM Totem Pole PFC IC Tips and Tricks

AND90147/D

INTRODUCTION

The Totem Pole PFC (TPFC) circuit is shown in Figure 1. The topology consists of two half−bridge configurations; one half bridge, commonly referred to as the “Fast Leg” switches at the PWM frequency and the other, commonly referred to as the “Slow Leg” switches at the AC line frequency. The fast leg switches perform the role of the switch and the diode in a classical boost PFC, that is these switches function to regulate the output voltage and shape the input current to provide high power factor and low harmonic distortion. The slow leg switches perform the role of the diode bridge in a classical boost PFC. Active switches with low ON resistance are utilized instead of diodes resulting in improved efficiency. Also, as will be described in the discussion below, the TPFC operates with only one slow leg and one fast leg device in the conduction path whereas the conventional boost PFC operates with two bridge diodes and one active switch or boost diode in the conduction path. Fewer devices in the conduction path and active switches replacing bridge diodes allow the TPFC topology to achieve higher system efficiency and power density than the classical boost PFC.

The fast leg switches are represented as MOSFETs in Figure 1, but the type of switch used for these devices is adaptable and either silicon FETs or Wide Bandgap (WBG) transistors can be used. Silicon FETs specified as fast recovery and/or low reverse recovery charge (Qrr) are suitable for this topology. WBG devices, whether Silicon Carbide (SiC) or Gallium Nitride (GaN), offer excellent $Qg \times R_{DS(on)}$ figure of merit and virtually no Qrr, making them optimal devices for the TPFC fast leg. The NCP1680 is designed for Critical Conduction Mode (CrM) and the PWM drive signals are logic level signals so there is no restriction on using either Si or WBG devices with the selection of an appropriate external half bridge driver.

The TPFC operates with bidirectional current flow in the inductor and the command of the fast and slow leg switches changes depending on the polarity of the AC line cycle. Operation of the TPFC during the positive and negative half line cycles is explained in detail in the NCP1680 datasheet.

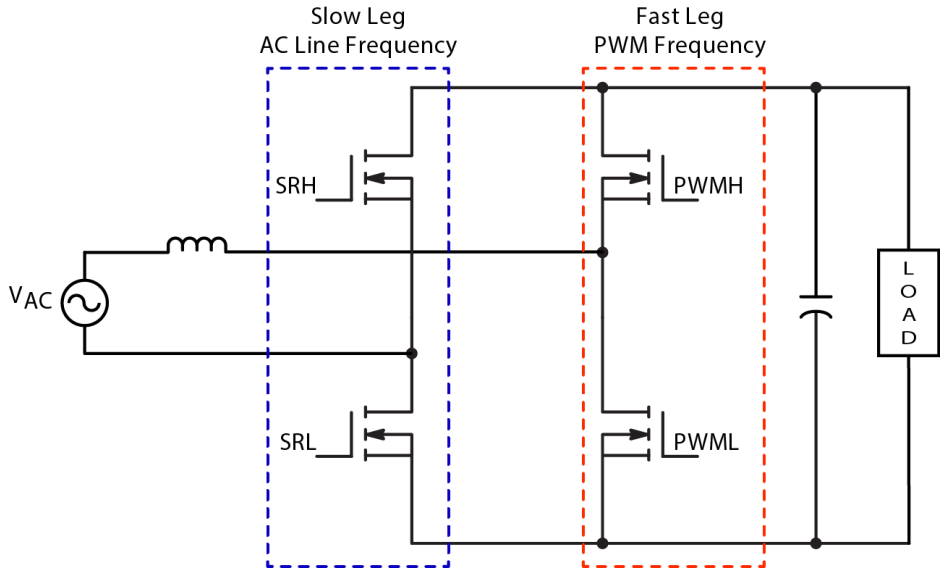

Figure 1. Simplified Totem Pole PFC Topology

Comparison to a Standard Boost PFC Converter

Totem Pole PFC is a derivative of a standard boost PFC converter where the bridge diodes are removed and therefore the boost circuitry directly interfaces with AC input. The key challenges with this approach are detection of line polarity, current sense, and current limit implementation. Further, TPFC is a synchronous boost converter as opposed to standard boost PFC implementation, therefore a zero current detection scheme needs to be implemented while taking care of "D" and "1−D" role reversal that is inherent to TPFC as it sees an unrectified AC line.

All the above−mentioned requirements are implemented in NCP1680. It is also important to note the similarities to a standard boost PFC. Criteria for selecting the boost inductor, output capacitor, and boost FET are exactly same between a TPFC and a standard boost PFC.

Key Specifications

Table 1. KEY SPECIFICATIONS FOR THE DESIGN EXAMPLE UNDER CONSIDERATION

Description	Symbol	Value	Unit
Input Voltage Range	$V_{ac(min)}$−$V_{ac(max)}$	90−265	Vac
Line Frequency Range	$F_{line(min)}$−$F_{line(max)}$	47−63	Hz
Output Voltage	V_{OUT}	395	V
Output Power	P_{OUT}	300	W
Output Ripple	V_{out_ripple}	< 5	%
PF @ Full Load	PF	> 0.95	
THD @ Full Load	THD	< 10	%
Max Switching Frequency	$F_{sw(max)}$	130	kHz
Min Switching Frequency	$F_{sw(min)}$	40	kHz
Full Load Efficiency		97% @ 90 Vac, 99% @ 265 Vac	

POWER STAGE COMPONENTS SELECTION CRITERIA

Boost Inductor

NCP1680 is a CrM Totem Pole PFC controller employing constant on−time control. The inductor selection criterion is same as a classical CrM boost PFC i.e., it is selected for carrying maximum peak current at the peak of the lowest voltage at which the power converter will operate. In a CrM PFC, input RMS current can be estimated as:

$$I_{ac_{max}} = \frac{P_{out}}{V_{ac_{min}} \times \eta} \quad \text{(eq. 1)}$$

Since, NCP1680 is a CrM controller, the inductor current is twice the line current. Therefore, peak inductor current is given by:

$$I_{L_{pk}} = I_{ac\_max} \times \sqrt{2} \times 2 \quad \text{(eq. 2)}$$

For the design specifications selected, peak inductor current is 9.72 A.

Maximum inductance value of boost inductor is given by:

$$L_{ind} = V_{ac\_min} \times \sqrt{2} \times \frac{D_{min\_LL}}{F_{sw\_min} \times I_{L\_pk}} \quad \text{(eq. 3)}$$

Where, D_{min_LL} is duty cycle at low line and is given by:

$$D_{min\_LL} = 1 - \frac{\sqrt{2} \times V_{ac\_min}}{V_{out}} \quad \text{(eq. 4)}$$

For, the specifications given above, calculated maximum boost inductance is 220 μH. A minimum of 40 kHz is assumed as the NCP1680 features a minimum frequency clamp to avoid the power converter enter audible frequency range. This is the highest inductance that will guarantee a pure CrM operation at the low line and at the full load. For instance, a 150 μH inductance will result in a switching frequency of around 59 kHz at the peak of low line while delivering full load.

Output Capacitor

Output capacitor of a front−end boost converter can be selected for the desired output ripple.

Assuming output ripple to be 4% ripple (< 5% spec) of the target output dc voltage, output capacitance is given by:

$$C_{out} = \frac{P_{out}}{V_{out} \times 2 \times \pi \times F_{line_{min}} \times V_{out} \times \text{Ripple \%}} \quad \text{(eq. 5)}$$

For the design specification under consideration, this yields in an output capacitor value of about 160 μF.

2x 100 μF, 450 V electrolytic capacitors are recommended. A ceramic capacitor in the range of 0.1 μF to 10 μF is recommended to filter out any high frequency noise on the bulk.

Slow Leg FET Selection

In a totem pole PFC, the inductor current flows through the slow leg FETs with both the FETs alternately conducting half−wave sinusoid. A simple way to calculate losses is to assume a full−wave sinusoid going through one FET. This is equivalent to calculating for each half−wave sinusoid and adding them together. Boost Inductor RMS current is given by:

$$I_{L\_rms} = \frac{I_{L\_pk}}{\sqrt{6}} \quad \text{(eq. 6)}$$

Above formula results in a combined RMS current of about 4 A. Assuming a 67 mΩ FET, this results in a combined conduction loss of 1 W for both the FETs. Since these FETs switch at a low frequency, switching losses can be ignored.

Alternatively, slow leg FETs can be replaced by diodes to save some cost, but the use of diodes will result in higher losses and it can be easily calculated as follows:

$$I_{L\_avg} = \frac{I_{L\_pk}}{\pi} \quad \text{(eq. 7)}$$

$$P_{br\_loss} = I_{L\_avg} \times V_{br} \quad \text{(eq. 8)}$$

Assuming a forward drop of 0.85 V will result in about 2.63 W in losses in the ‘slow leg’.

Fast Leg Switch Selection

Totem Pole PFC is a synchronous boost topology i.e., compared to a standard boost PFC it features a switch/FET instead of a diode during the “1−D” phase or during the inductor discharge phase. This is necessitated by the phenomenon explained in the introduction section of role reversal of the switches from positive to negative half−line cycle i.e., both the FETs act as the main FET and the synchronous FET.

Therefore, the losses are calculated as follows:

$$P_{sw\_D} = 0.5 \times \left(I_{L_{rms}}\right)^2 \times R_{ds_{fastleg}} \times D_{avg} \quad \text{(eq. 9)}$$

$$P_{sw\_Dprime} = 0.5 \times \left(I_{L_{rms}}\right)^2 \times R_{ds_{fastleg}} \times \left(1 - D_{avg}\right) \quad \text{(eq. 10)}$$

Above two equations are the conduction losses of each FET in both the “D” and “1−D” phase. Average Duty Cycle can be calculated using the following formula:

$$D(t) = \frac{V_{out} - \left(V_{ac\_min} \times \sqrt{2} \times |\sin(\omega \times t|\right)}{V_{out}} \quad \text{(eq. 11)}$$

$$D_{avg} = \sum_{t} \frac{D(t)}{N_{samples}}$$

Our design example, assuming a 50 mΩ GaN HEMT with a worst can $R_{DS(on)}$ of 100 mΩ, this yields in a total loss of 0.787 W for each FET or 1.574 W in combined conduction losses.

A 650 V, FET in an 8 × 8 mm package with an R_{JA} of 50 °C/W will remove the need of heat sinks in this design.

Current Limit

NCP1680 features a novel current limit scheme that utilizes down−slope of the inductor current to limit the current during the on−time. NCP1680 datasheet provides an excellent description. For the scope of this document, it is sufficient to know that selecting the resistor to implement this feature is no different than a standard PFC.

$$R_{zcd} = \frac{V_{cl\_LL}}{1.15 \times I_{L\_pk}} \quad \text{(eq. 12)}$$

To allow for inductance variation, the current limit resistor is selected to deliver 15% more max peak current. For our design example, R_{ZCD} calculation results in 125 mΩ resistor and its corresponding power dissipation is 0.4 W. Two 250 mΩ, 2 W resistors in a low inductance 4527 package not only yields good thermal performance but also its low inductance package reduces any ringing on the current sense waveform.

NCP1680 features an optional scheme where the current limit threshold can be reduced for high line compared to low line. Please refer to the electrical table in the NCP1680 datasheet.

SETTING UP THE NCP1680

Line Sensing (LVSNS1 and LVSNS2 Pins)

Line sensing is achieved by utilizing LVSNS1 and LVSNS2 pins. These two pins are low volage pins that can handle a max of 5.5 V. LVSNS1 is connected to the line side of the inductor and LVSNS2 is connected to the neutral. A differential ADC takes the difference between these two pins and creates a digital haversine inside the IC. This information is used for various features including polarity detection, brownout detection, line frequency monitoring etc. Please refer to the datasheet for details.

The recommended divide down for universal input applications is K_{L_DIV}, is around 100. i.e.,

$$\frac{R_{LOWERX}}{R_{LOWERX} + R_{UPPERX}} = \frac{1}{K_{L\_DIV}} \quad \text{(eq. 13)}$$

Typical values for R_{UPPERX} can be in the range of 5 MΩ to 10 MΩ while R_{LOWERX} can be 50 kΩ to 100 kΩ. Upper portion of the resistor divider should consist of at least two 1206 components connected in series to withstand the voltage drop. A small capacitor in the range of 47 pF to 470 pF is recommended to connect in parallel to the R_{LOWERX} resistors to filter any high frequency noise. This capacitor should be placed close to the LVSNSx pins.

Aux and Valley Sensing

Aux pin is used to monitor the switch node resonance through an auxiliary winding of the boost inductor. This pin enables valley−turn on of the main switch in both the CrM and frequency foldback operation.

Auxiliary winding is setup such that the Aux pin sees ringing on the switch node of the fast leg FETs. NCP1680 features an innovative valley pin detection circuit that turns on the main switching FET (“D” FET) with lowest possible voltage across it for both the positive and negative half line cycle. Ringing at the aux pin is given by $N_{aux} \times (V_{out} - V_{ac} \times \sqrt{2})$. To ensure a good signal to noise ratio N_{aux} of 0.1 is appropriate for this design. It ensures that at the peak of ac line we see 2 V at the aux winding and at the ac zero cross this will yield in about 40 V. Aux pin has a max current rating of −2/+5 mA. Therefore, a series resistor of at least 10 kΩ is recommended to the limit current. Further, as shown in Figure 2, a schottky diode is recommended that can clamp the pin a diode drop when the aux winding swings negative. A capacitor in the order of 100 pF can be installed to adjust the valley sensing circuit to catch the optimal point and further optimize the efficiency.

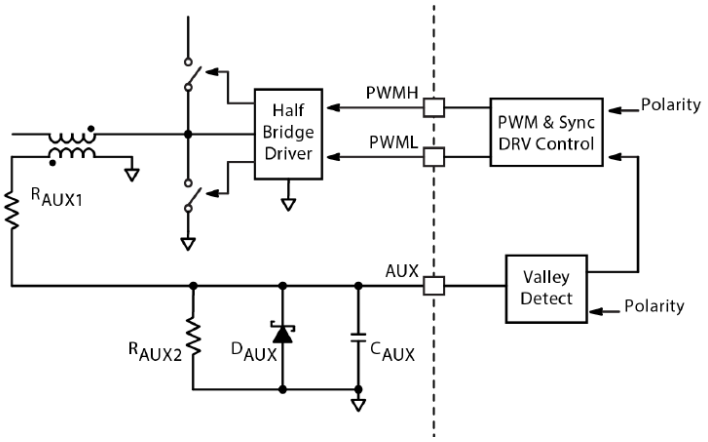

Figure 2. Typical Auxiliary Winding Arrangement

Feedback Resistors

Feedback resistors form a simple resistor divider and can be easily calculated using the following formula:

$$K_{FB} = \frac{V_{REF}}{V_{out}} \qquad \text{(eq. 14)}$$

Where K_{FB} is the feedback scaling factor. Internal reference of NCP1680 is 2.5 V and assuming a target output voltage of 395 V will result in K_{FB} of 0.0063.

The upper feedback resistor divider (R_{FBU}) is selected such that power loss in the feedback network is minimized. This value can impact the standby power of the power supply. For consumer applications, portion of standby power budget allocated to feedback resistor divider will be in the order 20 mW. Therefore, a 7.5 MΩ is a good starting point value for this resistor. Depending on the voltage rating and physical size this will be a network of 2 or 3 resistors. The lower feedback resistor can be calculated using the following formula:

$$R_{FBL} = \frac{R_{FBU} \times K_{FB}}{1 - K_{FB}} \qquad \text{(eq. 15)}$$

In our example, R_{FBL} comes out to 47.5 kΩ. NCP1680 implements a digital control loop and therefore, FB is continuously sampled by an ADC in the controller every 100 μs or 10 kHz. An anti−aliasing filter needs to be designed so that it effectively attenuates any signal above one−half of the sampling frequency. This can simply be a capacitor connected from FB pin to ground.

$$C_{AA} > \frac{1}{\pi \times R_{eff} \times F_{sample}} \qquad \text{(eq. 16)}$$

Where, R_{eff} is the parallel combination of R_{FBL} and R_{FBU}. For our example, anti−aliasing capacitor calculation results in 670 pF of capacitance. A 1 nF capacitor was selected for our design.

Zero Current Detection (ZCD) Pin Filtering

ZCD sensing in the NCP1680 controls the gating of the (1−D) switch and is also used for peak current limiting and overload protection. Therefore, good signal integrity from the ZCD sensing is integral to optimum performance in the NCP1680. As the ZCD sense is a pulsating waveform some R−C filtering directly at the ZCD pin is recommended to prevent switching noise from corrupting the ZCD signal. Recommended time constant for ZCD filtering is anywhere between 47 to 470 ns but the exact filter value is best determined empirically on real hardware.

There exists a tradeoff between an underdamped and an overdamped response of the R−C filter. An underdamped response will not provide sufficient filtering and the ringing on the ZCD signal may cause the overload protection to trigger prematurely. Conversely, an overdamped filter response will cause an excessively slow rise of the ZCD signal leading to delayed turn on of the (1−D) device, degrading overall application efficiency.

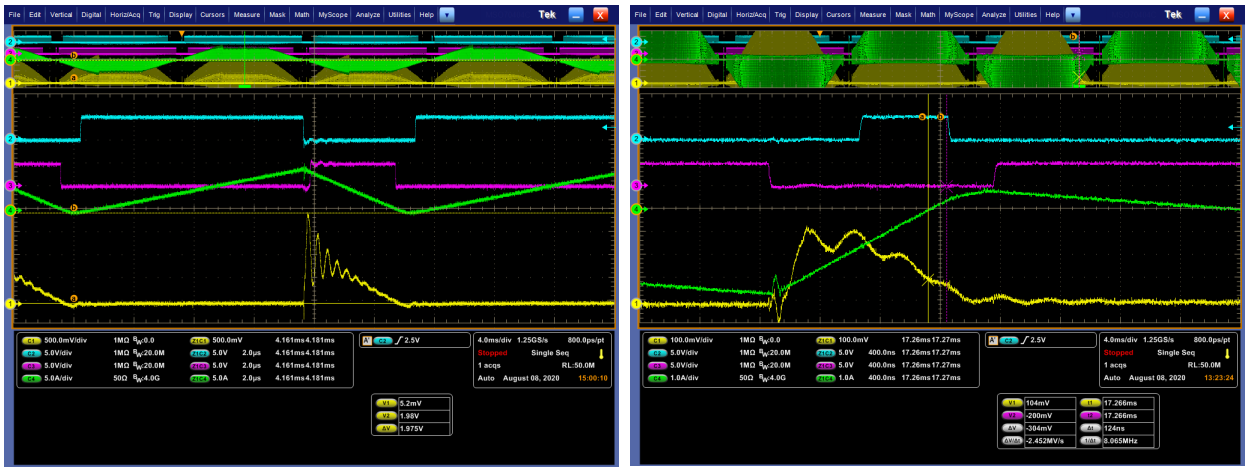

Figure 3. ZCD Underdamped Waveform (Left) ZCD Overdamped Waveform (Right)

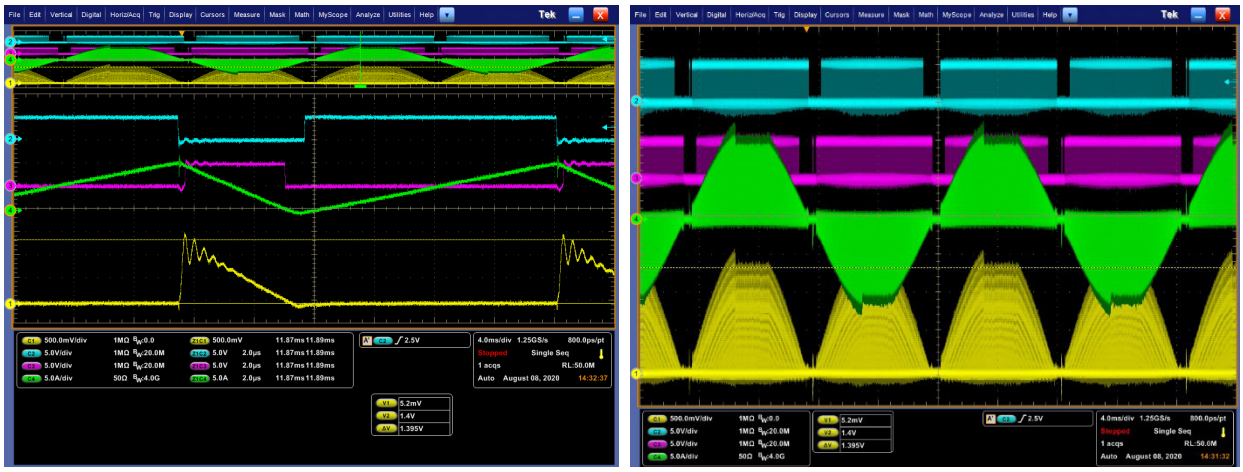

Figure 4. ZCD Optimally Damped Waveform (Left) & Corresponding Overload Waveform (Right)

Driver Input Filtering

Applications using the NCP1680 controller will require external gate driver ICs to efficiently drive the fast and slow leg switches. As the fast leg may employ Gallium Nitride (GaN) switches a fast and robust gate driver IC such as the NCP51820 or the NCP51530 is recommended. It is further recommended that the control signals (PWMx) from the NCP1680 be filtered directly at the input of the gate driver IC to prevent noise from coupling into the signal path and accidently triggering the gate driver circuit. The recommended filtering time constant for the driver inputs is ~50–100 ns, typically achieved with a 1 kΩ resistor and either a 47 or 100 pF capacitor placed directly at the pin of the driver.

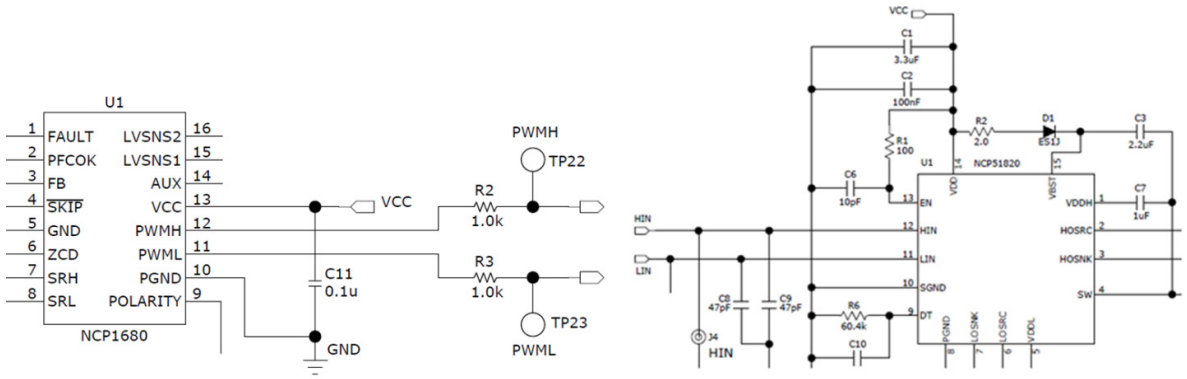

Figure 5. Suggested Half−Bridge Driver Input Filtering

Skip/Standby Mode Control

The NCP1680 features a Skip/Standby mode which enables the application to achieve very good no−load and light−load performance. The device must be externally commanded to enter the Skip mode by pulsing the PFCOK pin or grounding the $\overline{\text{SKIP}}$ pin, and in a typical application this control signal would be provided by a downstream dc−dc converter. An example of skip control circuitry using the PFCOK pin interfacing with the NCP13992 is shown below in Figure 6.

The interface circuitry can use component values similar to what is shown in the NCP1680 EVB. The PFCMODE pin on NCP13992 is nominally equal to the V_{CC} bias voltage of the controller, and pulses to GND when the LLC converter enters skip mode. The coupling capacitor will act as a charge pump and discharge the capacitance to GND at the PFCOK pin. The voltage and timing thresholds of the NCP1680 necessitate that the PFCOK pin be pulled below 400 mV for greater than 50 μs for the NCP1680 controller to enter the skip mode. A sample waveform of the PFCOK pin is shown in Figure 7.

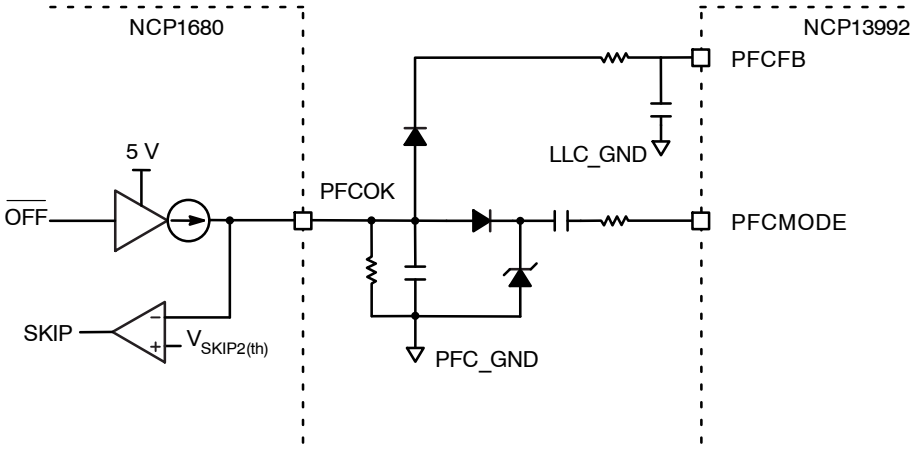

Figure 6. NCP1680 – NCP13992 Skip Interface

Once skip mode has been entered the NCP1680 controller will regulate the bulk voltage with a form of hysteretic control, meaning that the bulk voltage will cycle between its nominal regulation voltage and ~94% of nominal regulation. The frequency at which the bulk voltage cycles will be dependent on the output load. To maintain the EVB in skip/standby mode it is necessary to continue pulsing the PFCOK pin wherein every PFCOK pulse must meet the previously stated voltage and timing threshold requirements. The pulse frequency to maintain skip mode must be faster than the frequency at which the bulk voltage cycles between nominal regulation and 94% of nominal regulation. Hence it is technically possible to operate the EVB in skip mode at any load level and often in applications, skip operation may be necessary up to 5–10% of the rated load. Figure 8 shows skip mode operation with the EVB loaded at 20 W. A lighter load, or no load will result in much longer cycle frequency and better performance.

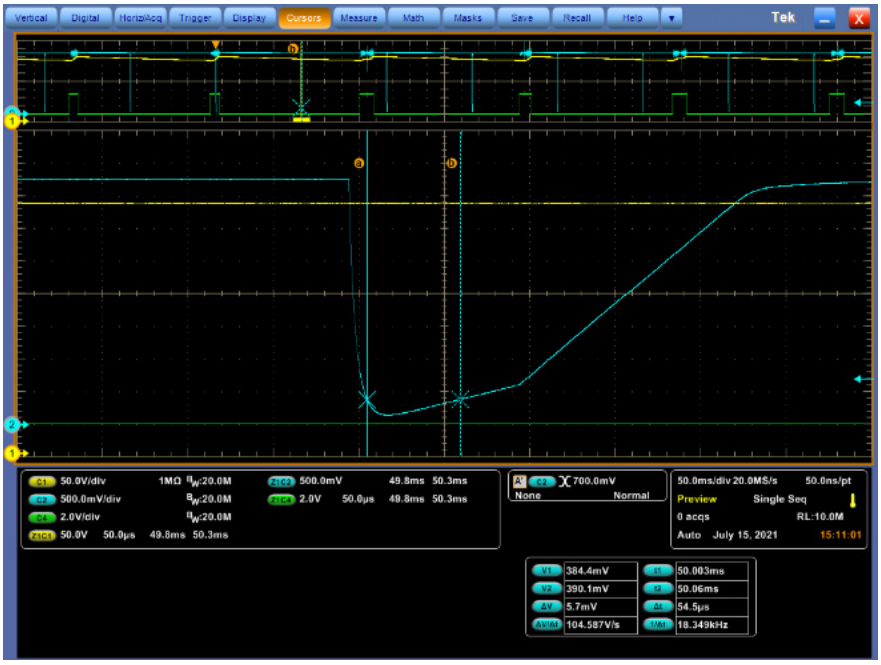

Figure 7. PFCOK Skip−Entry Signal (Ch1 = Bulk Voltage, Ch2 = PFCOK, Ch4 = $\overline{\text{SKIP}}$)

Figure 8. NCP1680 Skip Mode Operation (Ch1 = Bulk Voltage, Ch2 = PFCOK, Ch4 = $\overline{\text{SKIP}}$)

Inrush Current Considerations

Classical boost PFC converters can be subject to high inrush current due to the direct charging path from the AC source to the bulk capacitor. The Totem Pole PFC is no different, with the caveat that the current path is different depending on the conduction angle of the AC source when power is first applied. The figure below illustrates the inrush current paths in both positive and negative half line cycles. Two high voltage diodes connected in a half−bridge fashion as shown below is needed in a TPFC. Peak inrush current can be calculated using the following formula. This should be calculated at the peak of maximum input voltage.

$$I_{inrush} = \frac{V_{ac\_peak}}{\sqrt{\frac{L_{ind}}{C_{out}}} + L_{ind_{DCR}} + C_{out_{ESR}}}$$

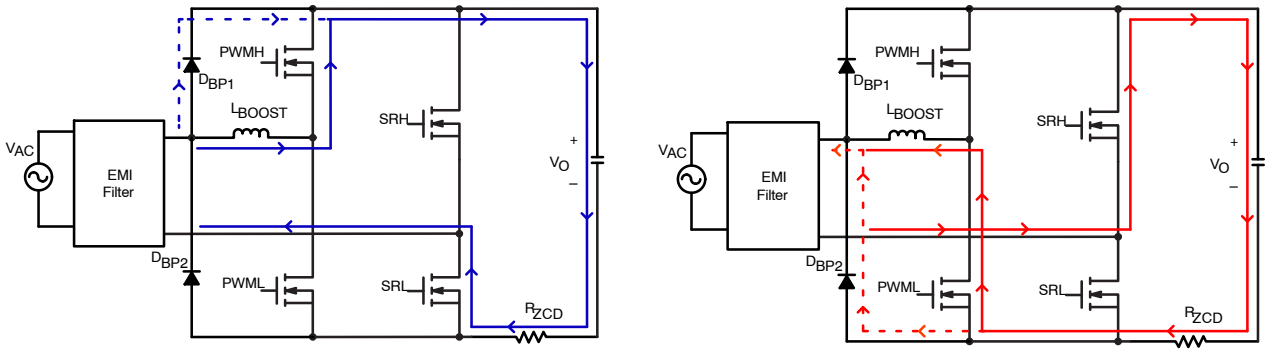

Figure 9. Inrush Current Path for Positive and Negative Half Line Cycles

EMI COMPONENT SELECTION

EMI component selection is a complex topic and depends on many variables such as: layout, magnetic construction technique, component type and placement. Therefore, the following discussion will be limited to common EMI topologies employed in TPFC and one specific issue related to TPFC i.e., noise at the AC zero crossing.

In a TPFC topology the slow leg bridge node is required to swing ~400 V (bulk voltage) at every AC line voltage zero crossing. The transition from 0–400 V (or vice versa) can generate excessive ringing and noise in the PFC which translates typically to observable common mode noise in the conducted emissions spectrum. A capacitor across drain−source of each of the slow leg switches is recommended to mitigate the noise generated during the transition. The capacitor does not need to be safety rated (X or Y ratings), however a film dielectric capacitor is recommended as certain ceramic capacitors suffer from piezoelectric phenomenon and may generate significant acoustic noise.

Figure 10 shows recommended filter configuration that would be needed to pass EMI standards. Typically, a combination of low frequency and high frequency common mode (CM) chokes are need along with y−capacitors that are decoupled to chassis of the power supply to filter out the CM noise. A differential mode (DM) choke along with X rated capacitors are needed to filter out the DM noise. EMI filters naturally will impact efficiency. Often, size of the EMI filter is inversely proportional the DC resistance and presents a tough trade−off for high density power supplies. Depending upon the component selection it is entirely possible to eliminate the HF CM choke or the DM choke. It is important to note that the leakage inductance of the CM choke will offer some DM filtering.

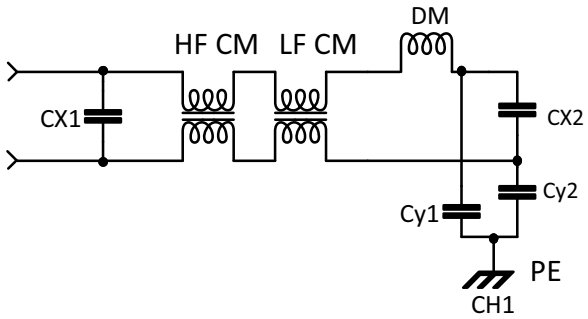

Figure 10. Typical EMI Filter Configuration

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊