ON Semiconductor®

Designing High-Efficiency ATX Solutions

Practical Design Considerations & Results
from a 255 W Reference Design

Agenda

- Regulation and Market Requirements
- Target Specification for the Reference Design
- Architectural Considerations
- Design Approach & Key considerations for each stage
  - PFC Stage
  - Main SMPS Stage
  - Secondary Stage
- Results
- Summary

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Drivers for Efficiency Improvements

- Reducing Energy consumption has become a major goal for governments and consumers across the globe
- Businesses need to adapt to these ever increasing demands for higher efficiency
- “Green” groups are continuing to constantly push the boundaries
- Higher integration into end-products and smaller form factors are also pushing the need for higher efficiency
- Early enablers of increased efficiency are gaining lot of attention and garnering increased rewards
- The Climate Savers Computing Initiative (CSCI) is an influential group that is pushing high efficiency requirements in computing
  - This group has the most aggressive efficiency targets of any major group or regulation agency world-wide
  - Their specifications were quickly adopted by other groups, including 80Plus in the US

CSCI Efficiency Requirements

	Year 1	Year 2	Year 3	Year 4
Time Table	July '07-June '08	July '08 - June '09	July '09 - June '10	July '10 - June '11
Minimum Efficiency Targets (@ 20%, 50%, 100% of rated o/p)	Energy Star 4.0 80%, 80%, 80% PF=0.9	82%, 85%, 82%	85%, 88%, 85%	87%, 90%, 87%
Equivalent to	80 PLUS	80 PLUS BRONZE	80 PLUS SILVER	80 PLUS GOLD
Purchase Commitment				
Most recent EnergyStar Compliant PC	100%	100%	100%	100%
85% PSU		>=20%	>=80%	100%
88% PSU			>=20%	>=80%
90% PSU				>=20%

- With active involvement from Intel, Microsoft, Google, HP, Dell & Lenovo this is a very influential group
- In addition, CSCI members are asked to have minimum purchase commitments listed above every year

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Reference Design

- ATX reference design that meets Climate Savers Year 3 targets (similar to 80 PLUS Silver targets) is presented
- The 255 W design was built to real-world specs
  - Specifications from 3 major OEMs were incorporated
  - Standard ATX dimensions and outputs
  - Standard protection features
  - The finished unit was fully tested in a rigorous manner
- Overall cost of the system was a key consideration during every design step
- LLC-HB Resonant Topology adopted for this design

Reference Design – Target Specifications

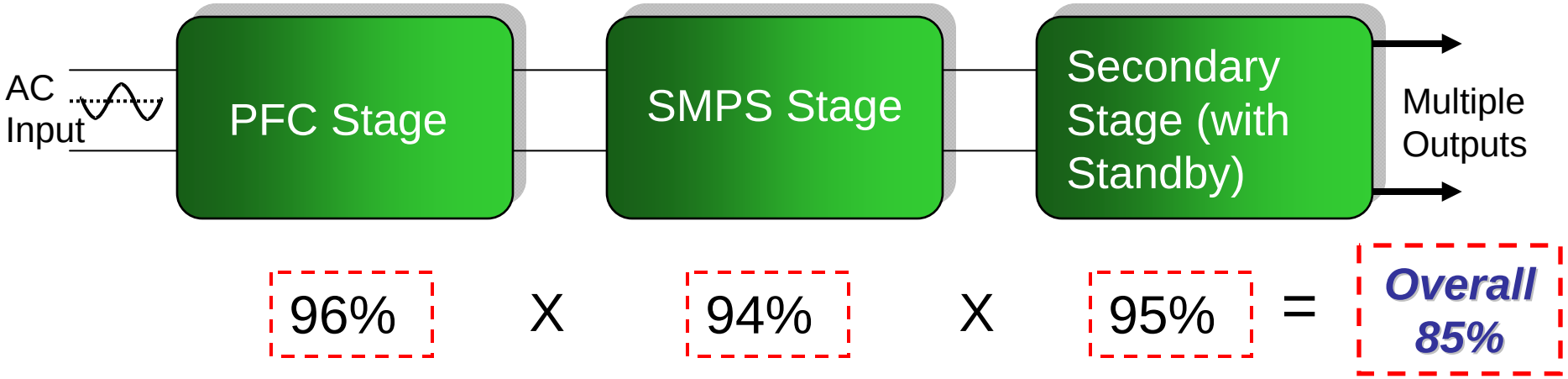
- Input range: 90 Vac to 264 Vac (100 Vac, 115 Vac, 230 Vac, and 240 Vac as the label voltage)
- Output power: 255 W
- Output voltage: 12 V_A, 12 V_B, -12 V, 3.3 V, 5 V, and 5 V_{sb}
- Efficiency requirement:
  - Above 85% at 20 % and full load
  - Above 88% at 50 % load
- Power factor: > 0.9 at 230 Vac, 50 % load
- Standby power requirement (FEMP): < 1 W

Reference Design – Output Loading

Output	Max Current (A)	Full Load (A)	50% Load (A)	20% Load (A)
12 V_A	13.0	9.5	4.75	1.90
12 V_B	7.0	5.12	2.56	1.02
-12 V	0.4	0.32	0.16	0.06
3.3 V	8.0	5.03	2.52	1.01
5 V	15.0	9.44	4.72	1.89
5 V_{sb}	3.0	2.39	1.20	0.48
Total Power (W)	361.2	255	128	51
Efficiency Requirement		**> 85 %**	**> 88 %**	**> 85 %**

Efficiency Targets by Stage

- To meet the overall efficiency target of 85%, each stage has to meet a minimum efficiency



Min. efficiency needed to achieve **85% overall efficiency** (across load/line)

- In order to meet the minimum efficiency targets, the architecture, key components, and overall design has to be carefully considered
- ON Semiconductor's reference design has achieved the objective while still keeping the overall cost down!!

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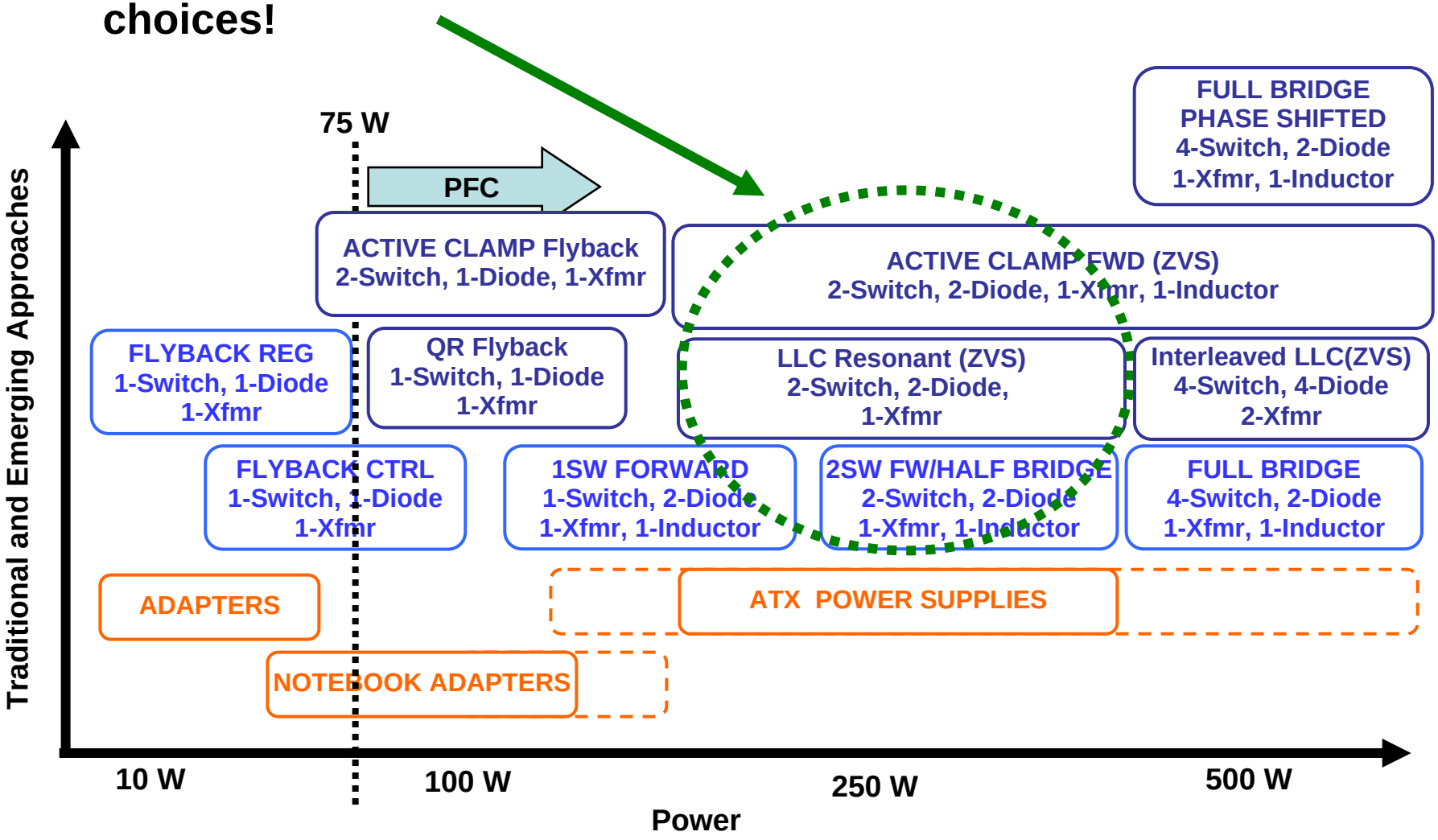
Topology Comparison

	Dual switch Forward	LLC HB Resonant	Active Clamp Forward
Transformer	Easy to design Leakage sensitive 1Q operation Lower creepage	Hardest to design Controlled $L_{leakage}$ 2Q operation Lower creepage	Hardest to design No leakage sensitive 2Q operation Higher creepage
MOSFET	500 V (600 V) 2 pcs high current	500 V (600 V) 2 pcs high current	800 V 1pcs high current 1pcs low current
Output Choke	Conventional design	No needed	Conventional design (smaller by 15%)
Output Capacitor	Conventional design	Needs higher ripple capability (more losses)	Conventional design
Cross regulation	Good with coupled choke	Not Very Good	Good with coupled choke
Switching	Hard Switching	Soft Switching	Soft Switching
Efficiency	Mid	High	High

Topology Options for Main Converter

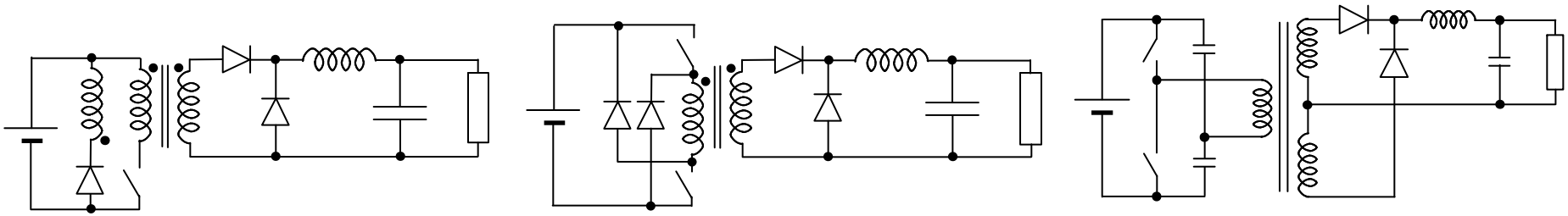
- **Output Power level and Efficiency requirements dictate specific choices!**



Topology Summary

2-SW Forward or other Hard Switching topology:

- Does not facilitate soft switching
- Does not facilitate sync rectification
- Lower Efficiency
- 2-sw forward has 30% worse MOSFET figure of merit (Vds*Irms)
- Higher cost in Magnetic components (Transformer + Output choke)
- 2 high current/voltage diodes required
- Heatsink required for both power MOSFETs



Benefits of LLC Series Resonant Converter

- Type of serial resonant converter that allows operation in relatively wide input voltage and output load range when compared to other resonant topologies
- Limited number of components: resonant tank elements can be integrated to a single transformer – only one magnetic component needed
- Zero Voltage Switching (ZVS) condition for the primary switches under all normal load conditions
- Zero Current Switching (ZCS) for secondary diodes
- Soft-switching and lower EMI are additional benefits

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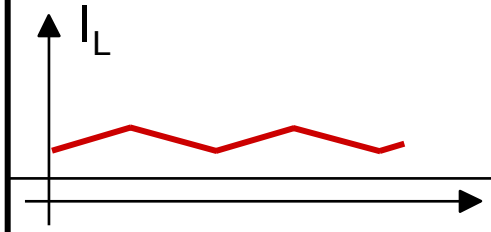
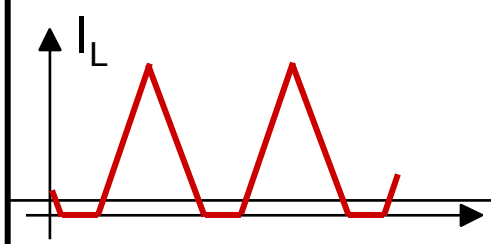
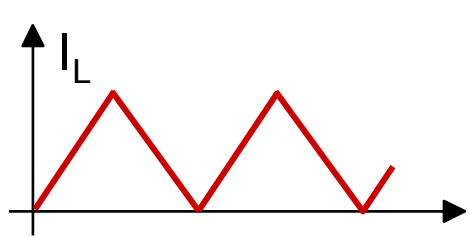
PFC Efficiency Improvements

- First, select the mode of operation (CCM or DCM/CrM)
- ON Semiconductor has >94% efficient solutions for both CrM and CCM applications

	Operating Mode	Main Feature
	Continuous Conduction Mode (CCM)	Always hard-switching Inductor value is largest Minimized rms current
	Discontinuous Conduction Mode (DCM)	Highest rms current Reduced coil inductance Best Stability
	Critical conduction Mode (CrM)	Good performance to cost Large rms current Switching frequency not fixed – EMI becomes harder

Considerations for Different Operation Mode

- For CCM, high efficiency can be achieved by:
  - Optimal switch selection (at light load, switching losses dominate, so it is more advisable to sacrifice Rds-on for faster switching)
  - Soft recovery boost diode
  - Inductor sized for copper loss reduction (Core losses are low)

- For DCM/CrM, high efficiency can be achieved by
  - Optimizing the inductor core for low core loss and low high-frequency winding losses
  - Selecting a lower Rds-on switch
  - Less attention to be paid to boost diode selection

PFC – Output Power Positioning

Part number	75-150 W	150-250 W	250-500 W	>500 W
NCP1601				
NCP1606				
NCP1653				
NCP1654/55				
NCP1650				
Recommended	Better fit exists			

Fixed Freq. Discontinous Conduction & Critical
Critical Conduction Mode
Continuous conduction Mode

- There is a grey area in the mode of operation to be chosen for a 250 W application
- For this reference design, a CCM mode PFC was chosen using ON Semiconductor's NCP1654

PFC – CCM MOSFETs Choice

	20N60C3 Rds(on) = 0.19Ω Coss = 780 pF		15N60C3 Rds(on) = 0.28Ω Coss = 540 pF	
	Switching losses (Coss)	Conduction losses	Switching losses (Coss)	Conduction losses
100 % load 270 W	1.28 W	1.34 W	0.88 W	1.98 W
	Sub-total: 2.62 W		**Sub-total: 2.86 W**	
50 % load 135 W	1.28 W	0.34 W	0.88 W	0.5 W
	Sub-total: 1.61 W		**Sub-total: 1.38 W**	
20 % load 54 W	1.28 W	0.05 W	1.28 W	0.08 W
	Sub-total: 1.33 W		**Sub-total: 0.96 W**	

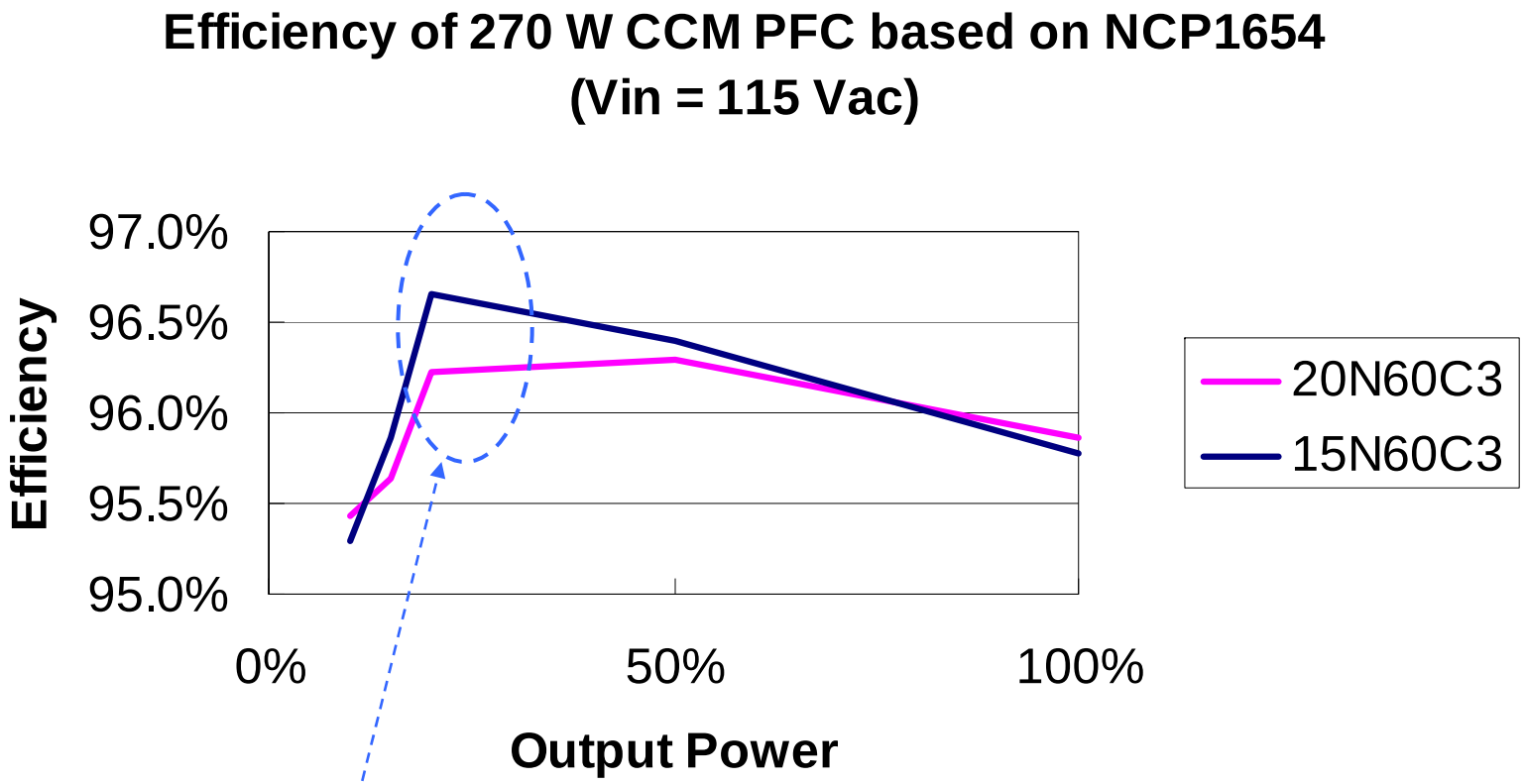
Conduction losses:

$$P_{on,\max} = R_{DS(on)} \cdot \left(\frac{P_{in,\max}}{V_{acLL}} \right)^2 \cdot \left(1 - \frac{8\sqrt{2}V_{acLL}}{3\pi V_{out}} \right)$$

Switching losses caused by Coss:

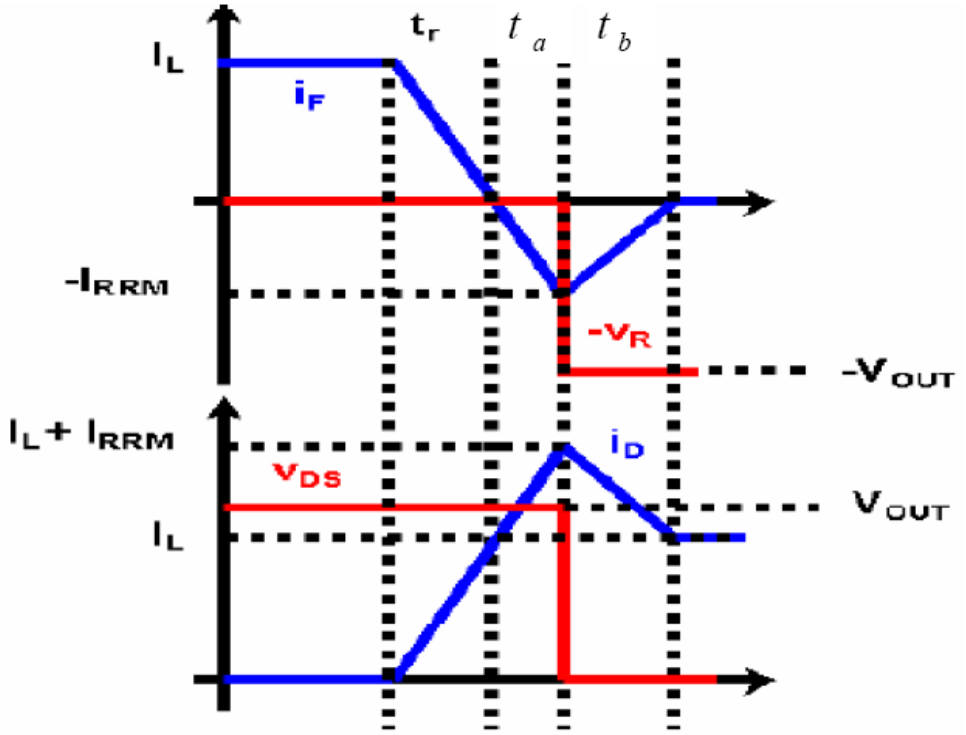
$$\int_0^{V_{end}} CV^2 dv = \frac{2}{3} C_{25} \sqrt{25} \cdot V^{1.5} \cdot f$$

PFC – CCM MOSFETs Choice (cont'd)



- At light load, switching losses dominate. In some conditions, MOSFETs with lower rating provide better efficiency

PFC – CCM Boost Diode Choice

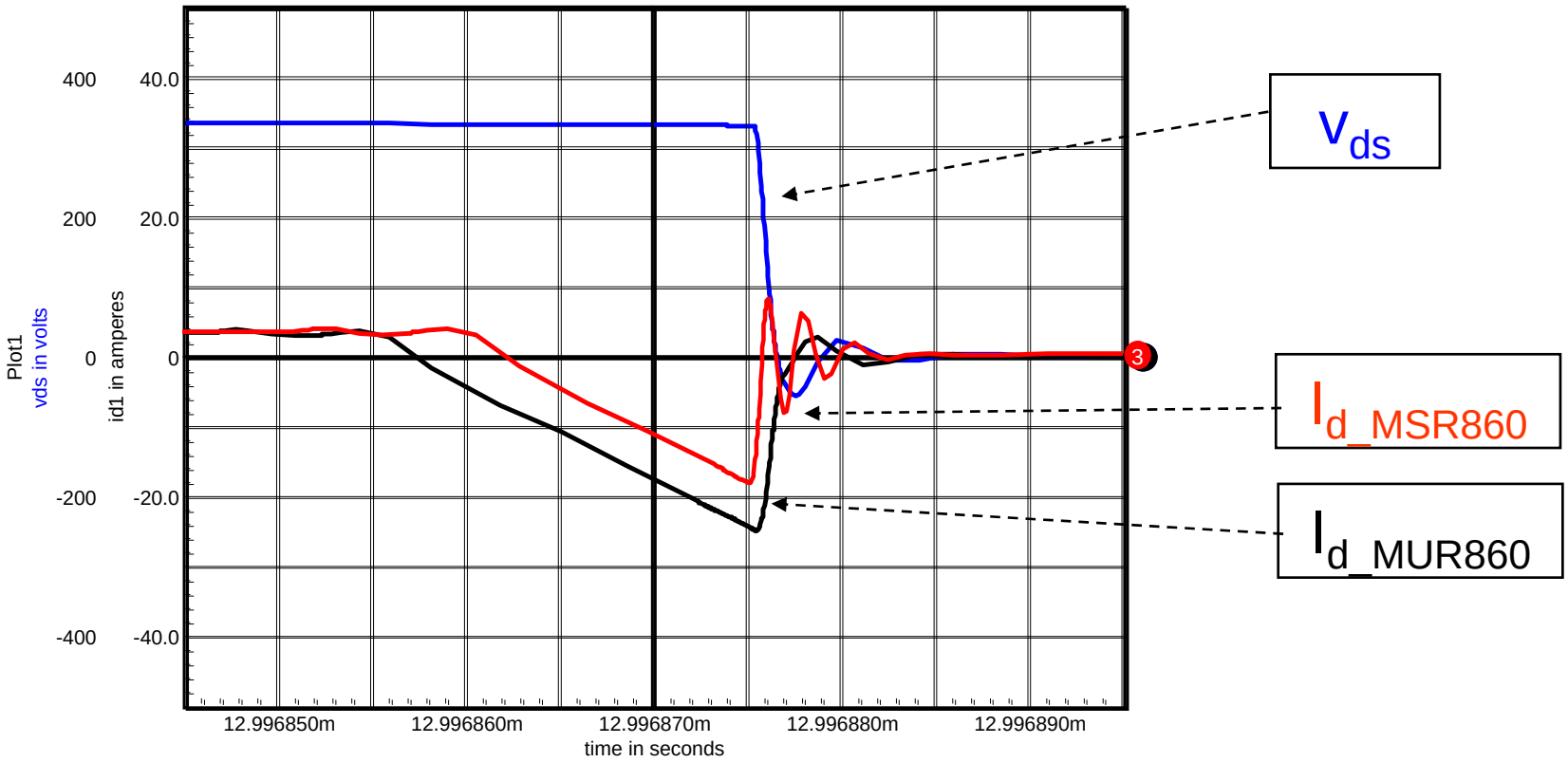


Boost diode

MOSFETs

- In CCM operation, the I_{RRM} (Q_{rr}), and (t_r + t_a + t_b) of boost diode impact the switching losses of MOSFETs and boost diodes significantly

PFC – CCM Boost Diode Choice (cont'd)

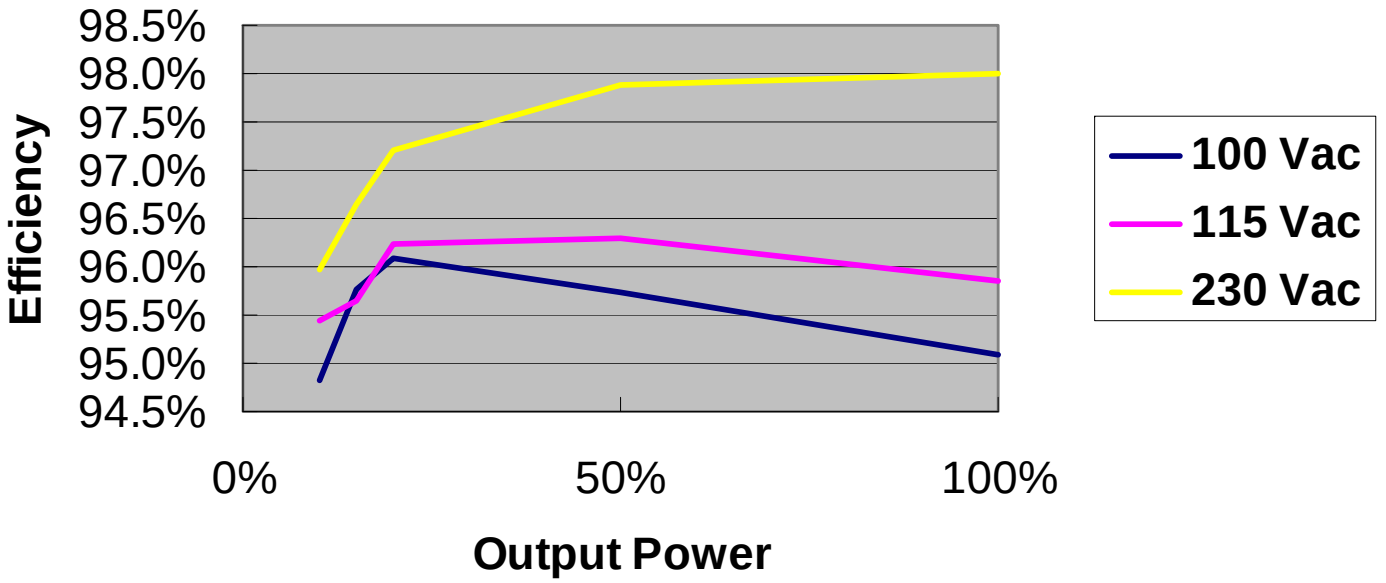


- A soft recovery diode, e.g. MSR860, with s = tb/ta = 3 and Qrr = 700 nC, reduces the switching losses

PFC – CCM Boost Diode Choice (cont'd)

- To further improve the efficiency, here come several choices:
  - Silicon Carbide Schottky Diode – zero recovery diode
    - This provides better performance at added cost
  - Qspeed Q-series PFC rectifier – soft recovery diode with s = tb / ta =1.3 and Qrr = 35 nC

NCP1654 CCM PFC 270 W Application



PFC MOSFET Q1 = 20N60C3

PFC Diode D1 = Qspeed LQA08TC600

PFC choke = 650 μH

Efficiency > 95 % at 100 Vac

- By selecting suitable components, efficiency is optimized
- But some people might think the boost diode costs more, what other solutions can be used?

Summary of PFC Stage Considerations

- Both CCM and CrM/DCM PFC can provide good efficiency at power range around 250 W
- The design considerations for each topology are different
- For CCM, high efficiency can be achieved by:
  - Optimal switch selection
  - Soft recovery boost diode
  - Inductor sized for copper loss reduction (Core losses are low)
- For DCM/CrM, high efficiency can be achieved by
  - Optimizing the inductor core for low core loss and low high-frequency winding losses
  - Selecting a lower Rds-on switch
  - Less attention to be paid to boost diode selection

Key Components used in PFC Stage for Reference Design

- NCP1654, 65 kHz CCM PFC controller in SO-8
- PFC choke
  - PQ3319
  - Inductance is 650 µH
  - 0.1 * 50 Litz wire
- PFC MOSFET
  - SPP15N60C3, 15 A, 650 V, 0.19 Ω $R_{ds(on)}$
- PFC Diode
  - Qspeed LQA08T600, 8 A, 600 V

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Topology Options for Main Convertor (cont'd)

Advantage with Soft Switching solutions:

- Cost effective, highly efficient and lower EMI due to soft switching
- ACF and LLC are being used for 80 PLUS and 85 PLUS solutions
- Self-driven Sync Rectification in ACF
- Facilitates Synchronous Rectification in LLC
- 15% lower output inductor in ACF or No output choke required in LLC
- Better Transformer core utilization (2Q operation)
- Allows operation at higher frequency, thus smaller size

Active clamp was used in 1st 80 PLUS ref design in past. In order to show another example, LLC was chosen in this 85 PLUS efficiency design

Design Tips for Light Load Efficiency

- Reduce switching losses with soft-switching operation by selecting FETs with low capacitance (trade-off with low Rds-on)

	Dual switch Forward	LLC HB Resonant	Active Clamp Forward
Total FET Coss	1560 pF	1560 pF	930 pF
Turn-on voltage	400 V	0 V	200 V
Turn-on losses (100 kHz)	4.8 W	0 W 	1.1 W
Turn-off current	2.5 A	1.6 A	2.0 A
Turn-off losses (25 ns, 100 kHz)	0.8 W	0.4 W 	0.6 W

Design Tips for Light Load Efficiency (cont'd)

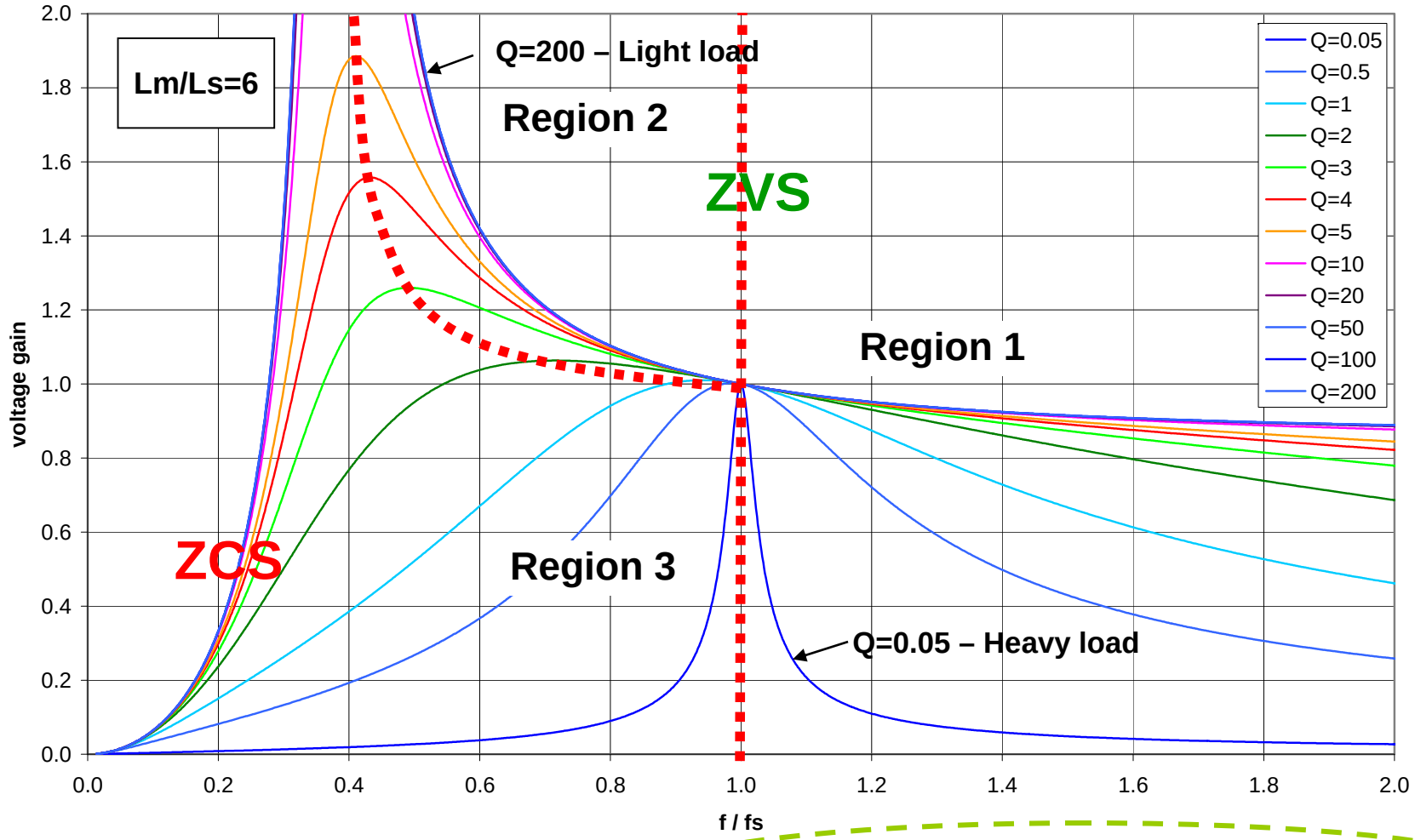
- At light load, every 0.1 W counts!
  - For a 250 W output system, 0.6 W loss reduction leads to 1.2% efficiency improvement at 20% load

- Within the high-volume ATX application space of 240 – 300 W, LLC HB Resonant topology is a good solution to achieve higher efficiency at light load due to ZVS on primary MOSFETs

The Optimized Operating Point

- Gain characteristics shape and needed operating frequency range is given by these parameters:
  - Lm/Ls ratio
  - Characteristic impedance of the resonant tank
  - Load value
  - Transformer turns ratio
- The operating point of fop = fs is the most attractive
  - Sinusoidal primary current
  - MOSFETs and secondary rectifiers optimally used
  - This operating point can be reached only for specific input voltage and load (usually full load and nominal Vbulk)

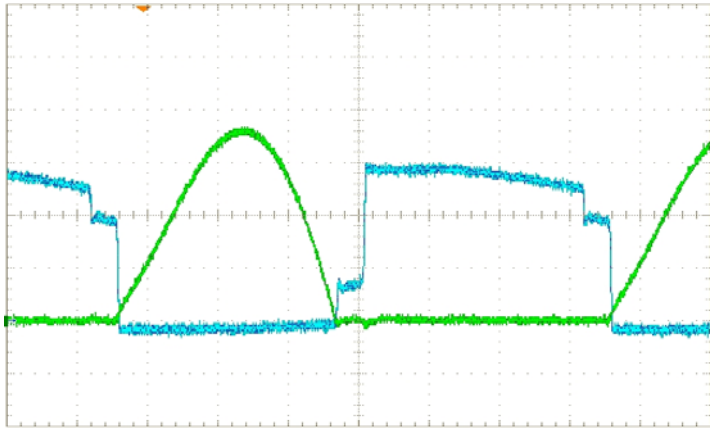
Normalized Gain Characteristic



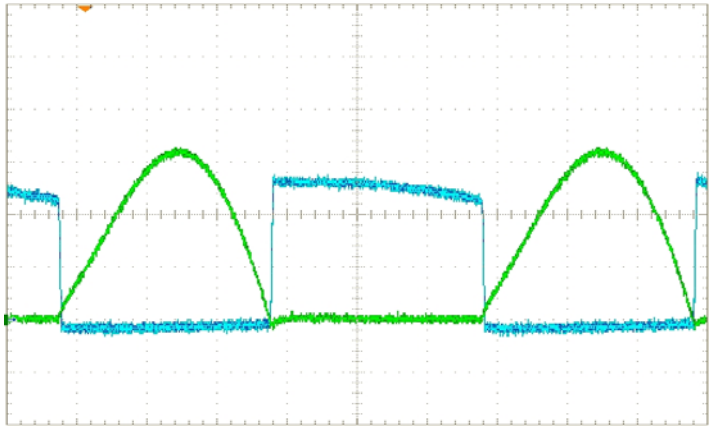
Region3: ZCS region

Region 1 and 2: ZVS operating regions

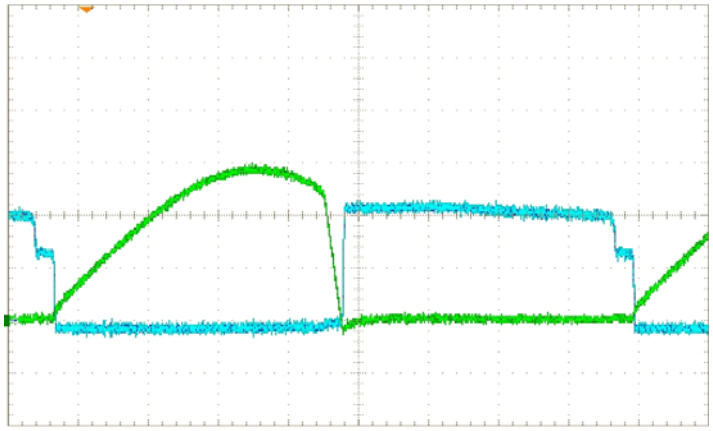
Secondary Waveforms of LLC with Diode



a) $F_{op} < F_s$



b) $F_{op} = F_s$



c)$F_{op} > F_s$

- rectifier current
- rectifier voltage

Assumptions:

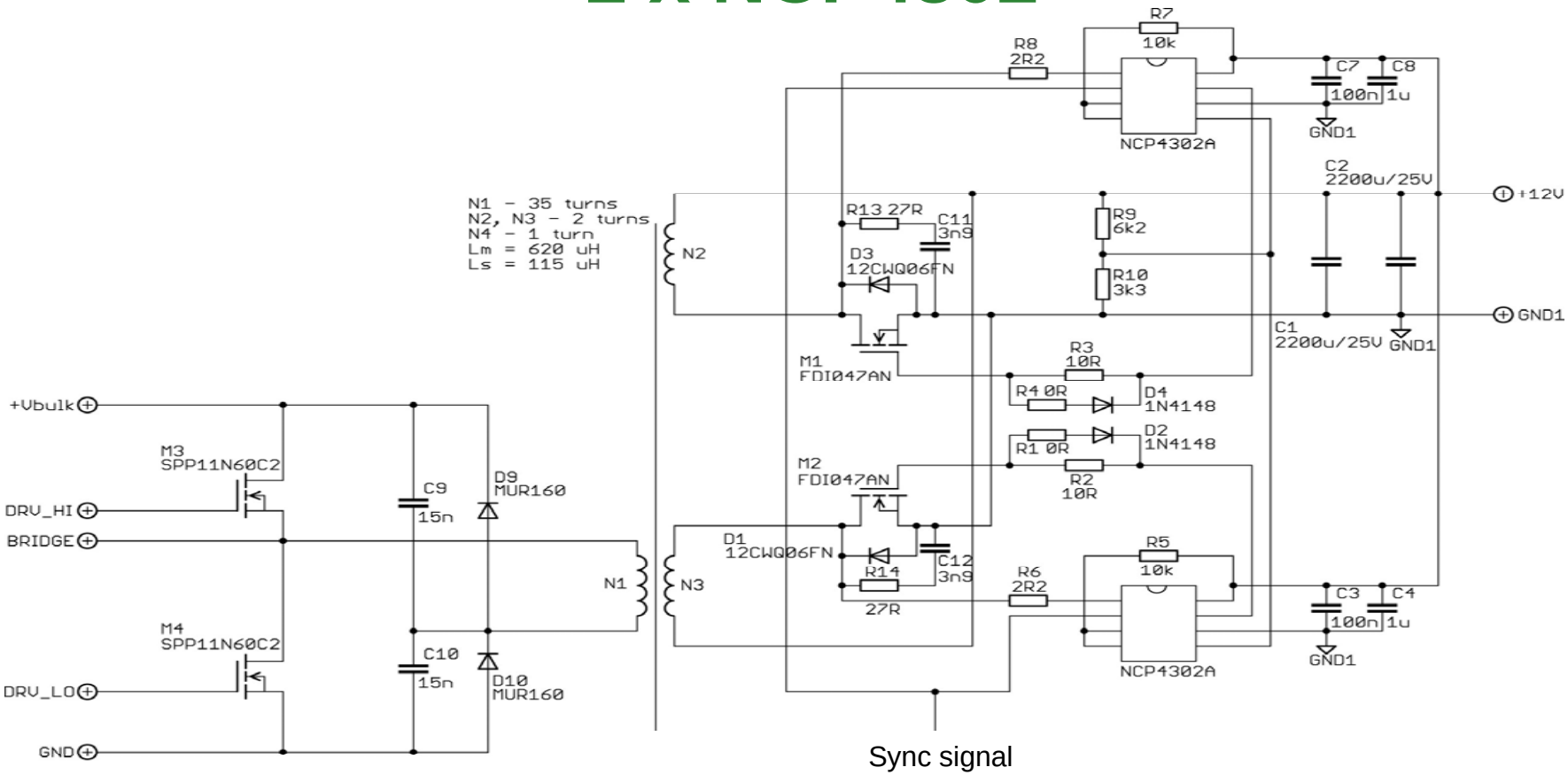
1. Secondary current is sinusoidal
2. Operating state is in resonant frequency F_s.

Secondary Current Calculations

Equations	24 V/10 A output	12 V/20 A output
RMS diode current $I_{D\_RMS} = I_{out} \cdot \frac{\pi}{4}$	$I_{D\_RMS} = 7.85A$	$I_{D\_RMS} = 15.7A$
AVG diode current $I_{D\_AVG} = \frac{I_{out}}{2}$	$I_{D\_AVG} = 5A$	$I_{D\_AVG} = 10A$
Peak diode current $I_{D\_PK} = I_{out} \cdot \frac{\pi}{2}$	$I_{D\_PK} = 15.7A$	$I_{D\_PK} = 31.4A$

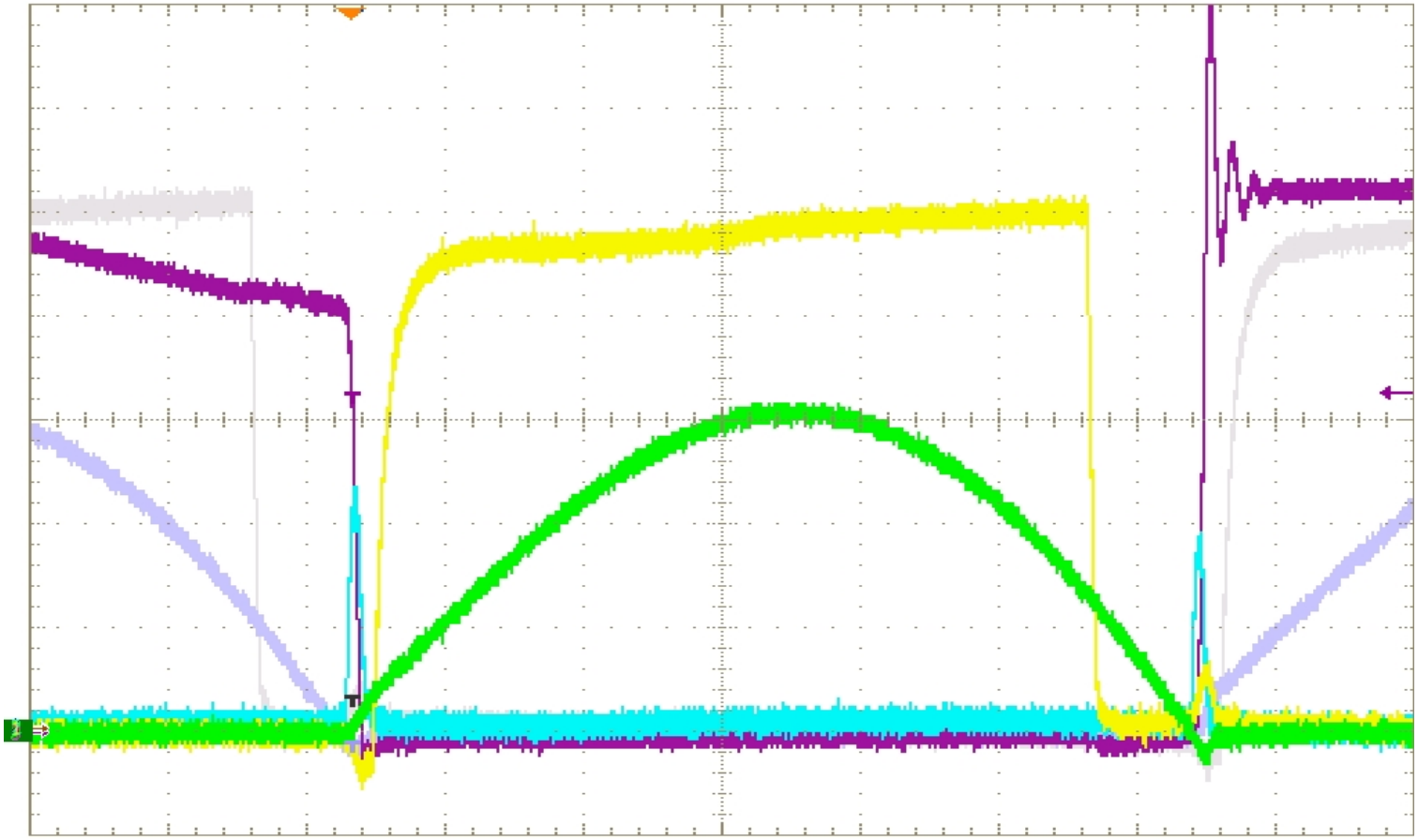
- Even at 12 V, the RMS current is still in the acceptable range for LLC topology

Synchronous Rectification Solution using 2 x NCP4302



Sync signal
(patent pending)

SR Operation for $F_{op}= F_s$



C1 2.0V
C2 2.0V
C3 5.0V
C4 10.0A Ω
R1 2.0V 1.0µs
R2 10.0A 1.0µs

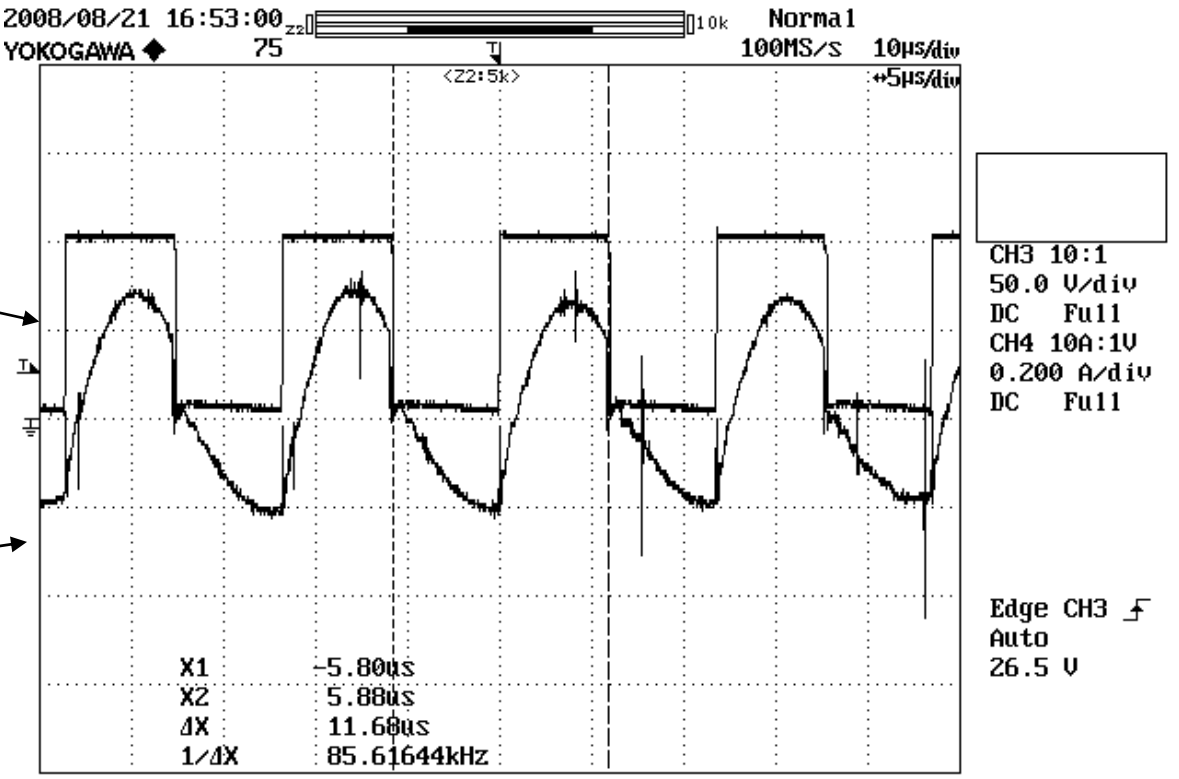
- SR MOSFET gate signal
- Rectifier current
- SR MOSFET drain voltage
- Trigger input

1.0µs/div
5.0GS/s 200ps/pt
A C3 ⌝ 16.3V

The Operation Point of LLC HB

Vds of primary MOSFET

Current in resonant tank



- The resonant frequency, f_s, is 77 kHz
- The operating frequency at full load is 85 kHz
- Primary MOSFETs operate at ZVS

Key Components of Main SMPS Stage in Reference Design – Primary Side

- NCP1396, LLC controller featuring high voltage driver

- Integrated resonant tank solution, i.e. the leakage inductance of transformer acts as resonant inductance.
  - EE35 bobbin
  - Lm = 630 µH
  - Ls = 80 µH
  - Np = 33 Turns, 0.08 * 80 Litz wires
  - Ns = 2 Turns, 0.2 *25 Litz wires

- MOSFETs at primary side
  - STP12NM50, 12 A 500 V, 0.35 Ω $R_{ds(on)}$

Key Components of Main SMPS Stage in Reference Design – Secondary Side

- 2 pcs of NCP4302, the synchronous rectifier controller, to control SR MOSFETs

- MOSFETs as rectifiers
  - STP80NF55, 80 A, 55 V, 5 mΩ $R_{ds(on)}$

- Diodes in parallel the SR MOSFETs to reduce dead time losses
  - MBR20L45CTG, 20 A, 45 V

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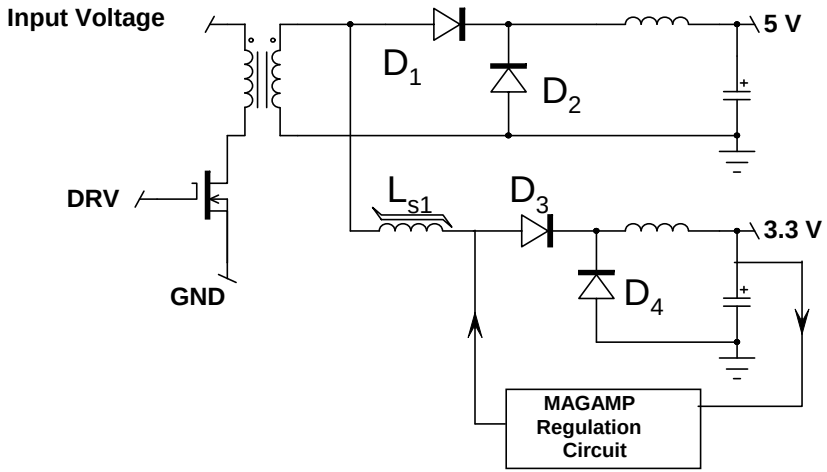
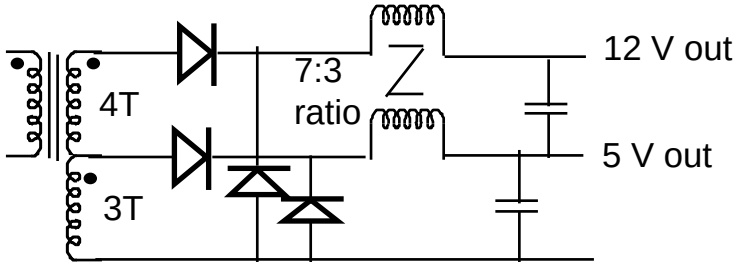
Topology Options for Secondary Convertor

- New stringent requirements for cross regulation require zero load operation on +3.3 V and +5 V outputs

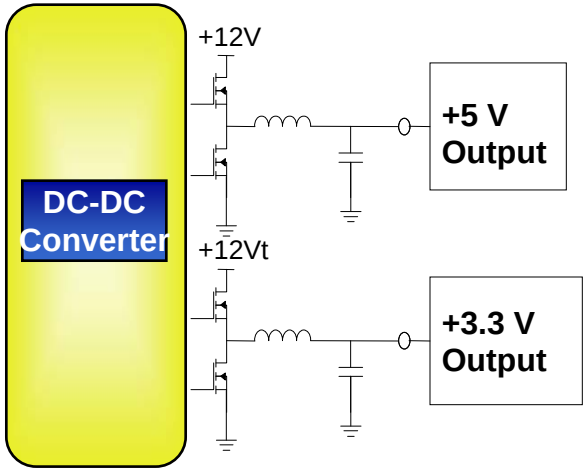
- Stacking transformer windings, coupling the output chokes, Mag-amp approach is hard to meet new requirements



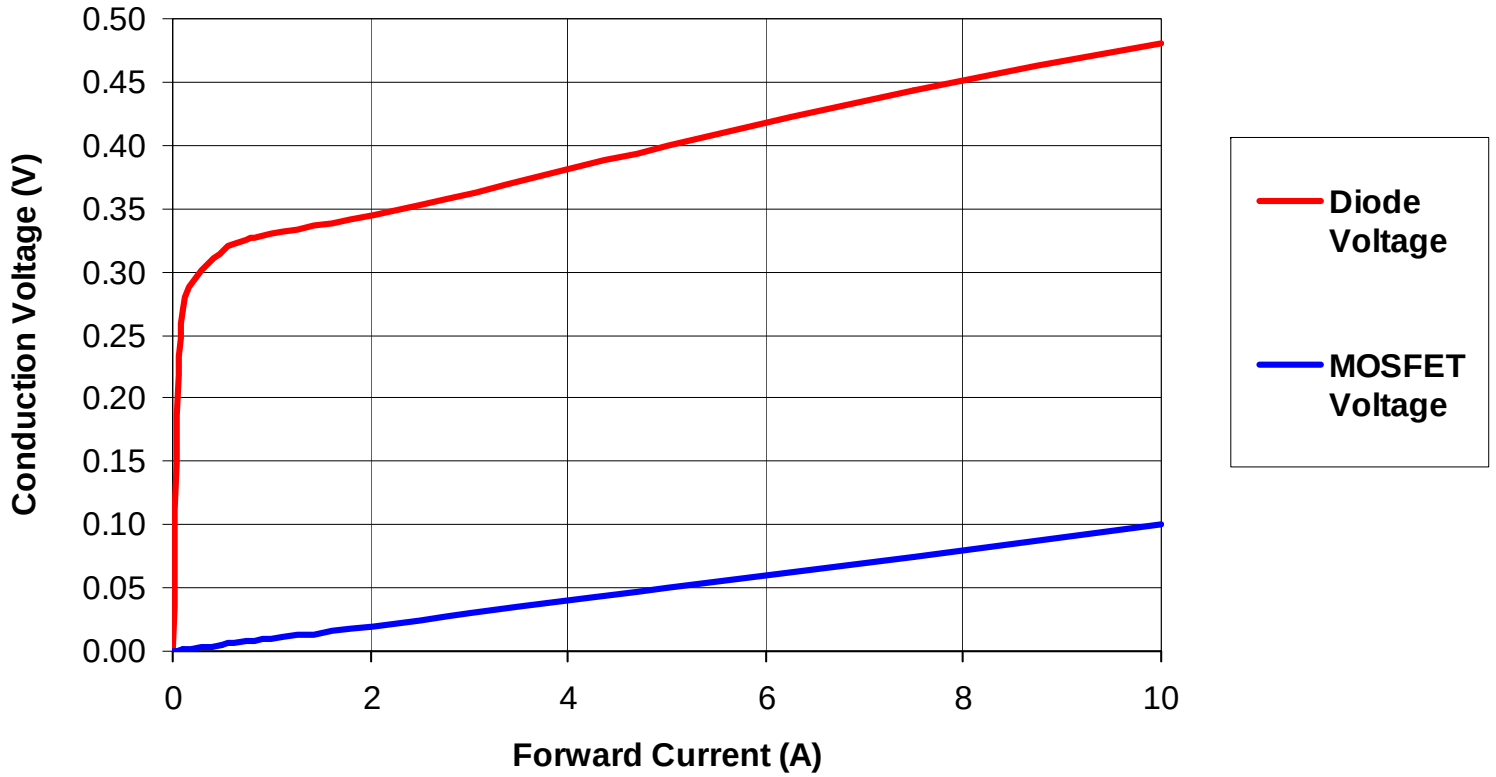


Topology Options for Secondary Converter

- LLC HB does not have an output choke
  - So, it lends itself to moving to a single +12 V output followed by a dc-dc stage to generate the +5 V and +3.3 V outputs
  - This provides better cross-regulation
  - However, the efficiency is a challenge due to additional power processing stages (+12 V → +5 V and +3.3 V)



Why Synchronous Rectification in DC-DC?



- Diode forward drop (0.35 V to 0.45 V) limits efficiency to 3.3/(3.3+0.45)=88%

Design Consideration in SR Buck

What can be done to Reduce Power Loss?

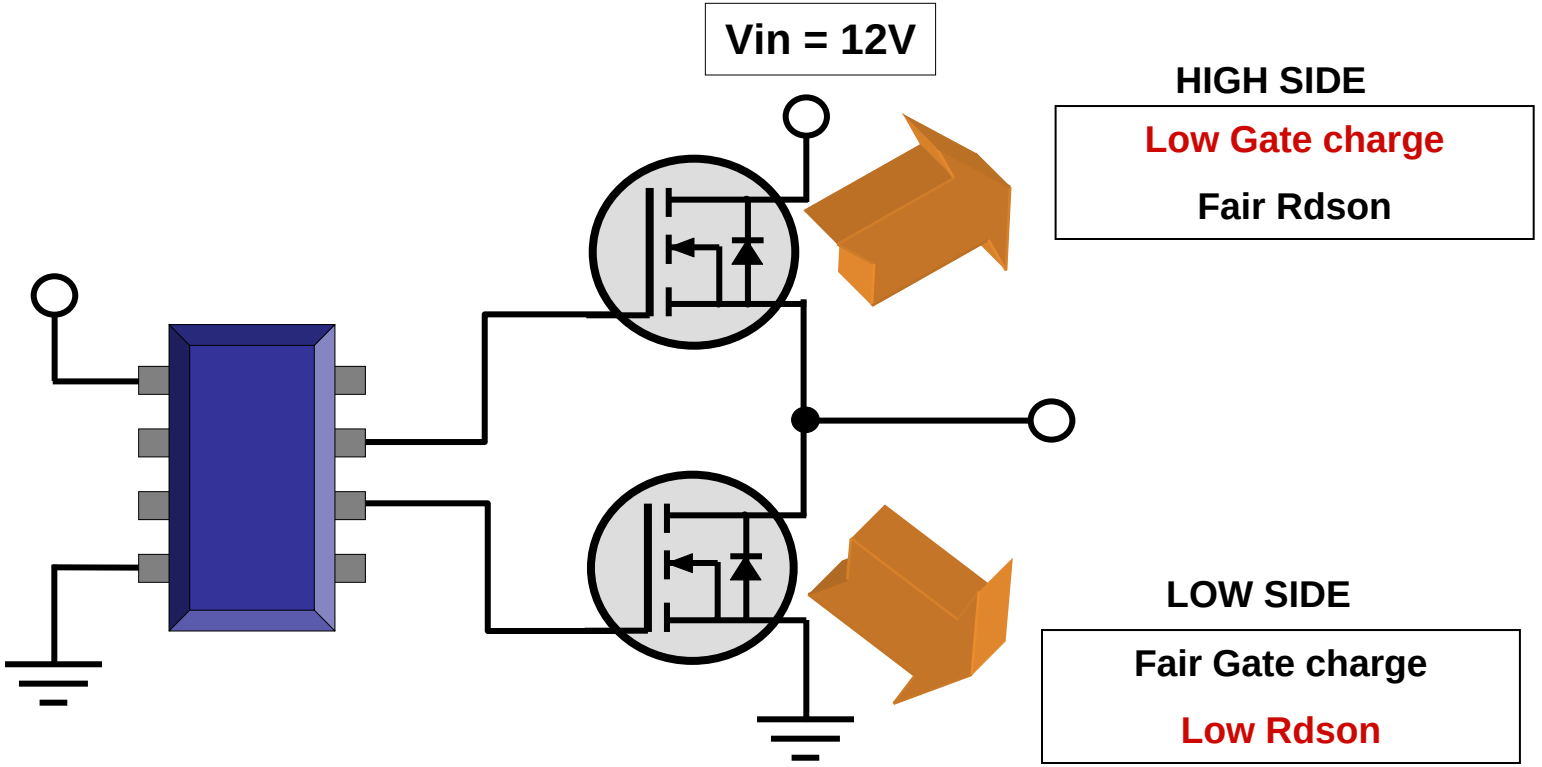
- Upgrade MOSFET, Reduce Rdson and chose low Qg
- Add Schottky diode in parallel low side FET to reduce dead time loss
- Use inductor with Low DCR
- Use reasonably high frequency (200 kHz ~ 400 kHz) due to the switching lost
- Increase PCB layers and copper thickness

Design Consideration in SR buck (cont'd)

Layout Consideration:

- Sensitive signals should be kept away from the high dV/dT trace such as gate drive (minimum 5 mm or 0.2 in)
- In some practical design, noise isolation technique is also an alternative solution for compact PCB board
- The MOSFET gate traces to the IC must be short, straight, and as wide as possible
- Minimize the "Star" or "T" trace length on gate traces
- The VCC bypass capacitor (0.1 F or greater) should be located as close as possible to the IC and connection to GND must be as short as possible

MOSFETs Selection for SR Buck Application



- The losses in the Low side FET is dominated by conduction losses
  - Therefore Rdson is the most important
- High side FET affects the switching speed
  - Therefore, it is important to minimize the switching charge Qsw and gate resistance Rg, while maintaining a reasonable on-resistance Rdson

Key DC to DC Buck Converter Components used in Reference Design

- 2 pcs of NCP1586, the buck converter controller, for 5 V and 3.3 V outputs
  - NCP1586 built in non overlap timing control prevents cross conduction of rectification MOSFETs
- Power chokes
  - 5.7 µH
- MOSFETs
  - NTD4809N, 58 A, 30 V, 14 mΩ $R_{ds(on)}$

Key Components for Standby Converter in Reference Design

- NCP1027, 65 kHz PWM controller featuring 700 V MOSFET
  - The efficiency at full load is optimized because it allows deep CCM operation thanks to the adjustable ramp compensation feature
  - The light load efficiency is optimized thanks to the skip mode operation

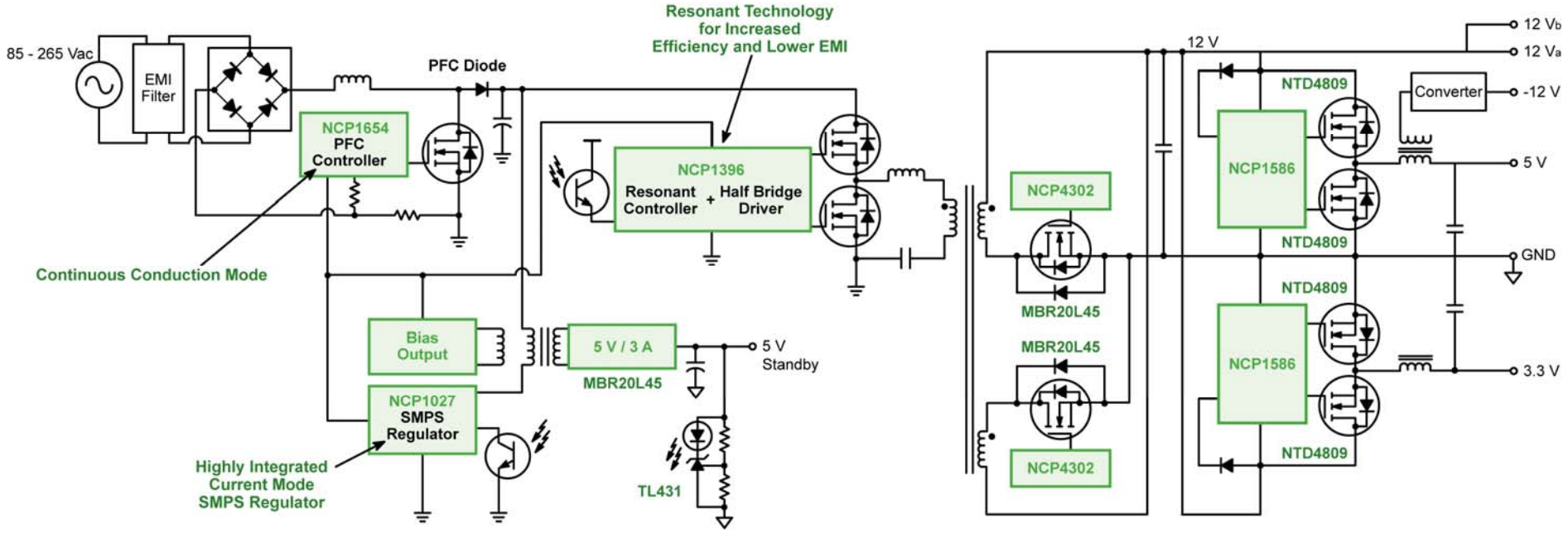
- The Stby transformer
  - EEL19 bobbin
  - Np = 105 T, 1.4 mH
  - Ns = 6 T
  - Naux = 20 T

- Diode
  - MBR20L45CTG, 20 A, 45 V

Agenda

- Regulation and Market Requirements
- Target Specification for the Reference Design
- Architectural Considerations
- Design Approach & Key considerations for each stage
  - PFC Stage
  - Main SMPS Stage
  - Secondary Stage
- Results
- Summary

255 W, 85 PLUS ATX Power Supply Reference Design



Specification	20% load	50% load	100% load
• Multiple-Output • Non-Redundant • PFC 0.9 at 50%	85%	88%	85%

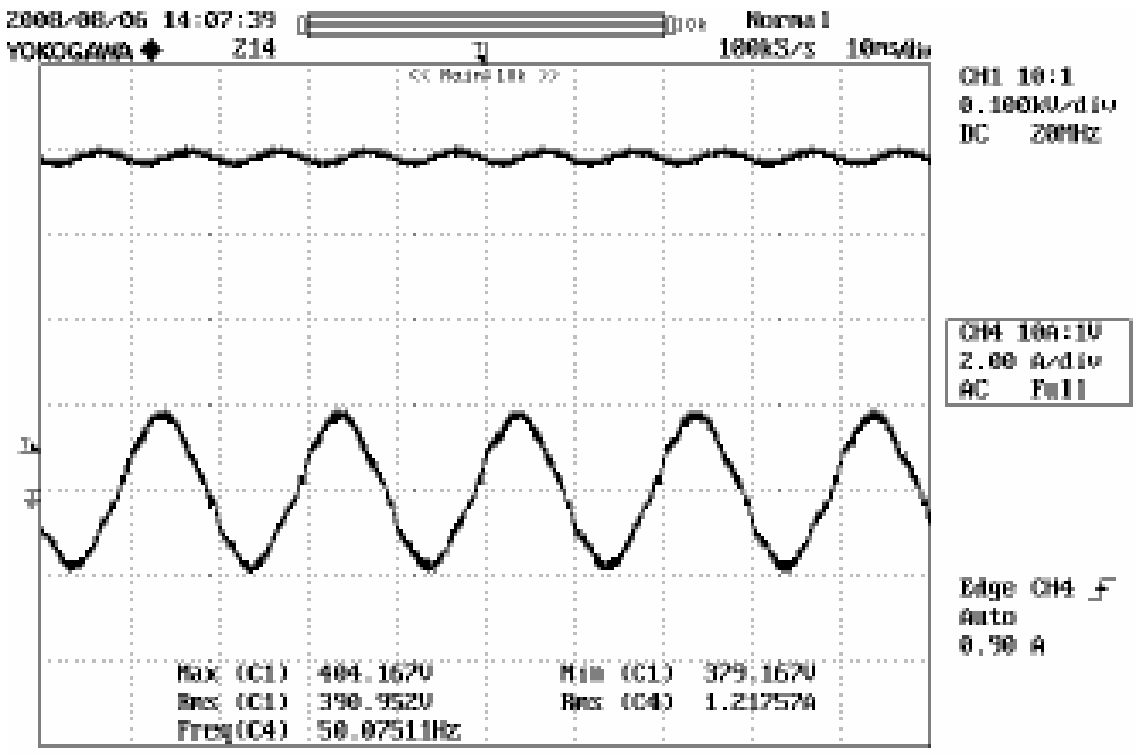
80 PLUS SILVER
Climate Savers 3

GreenPoint™ From ON Semiconductor

The Input Current at 230 Vac, 50 % Load

Vbulk

Input Current



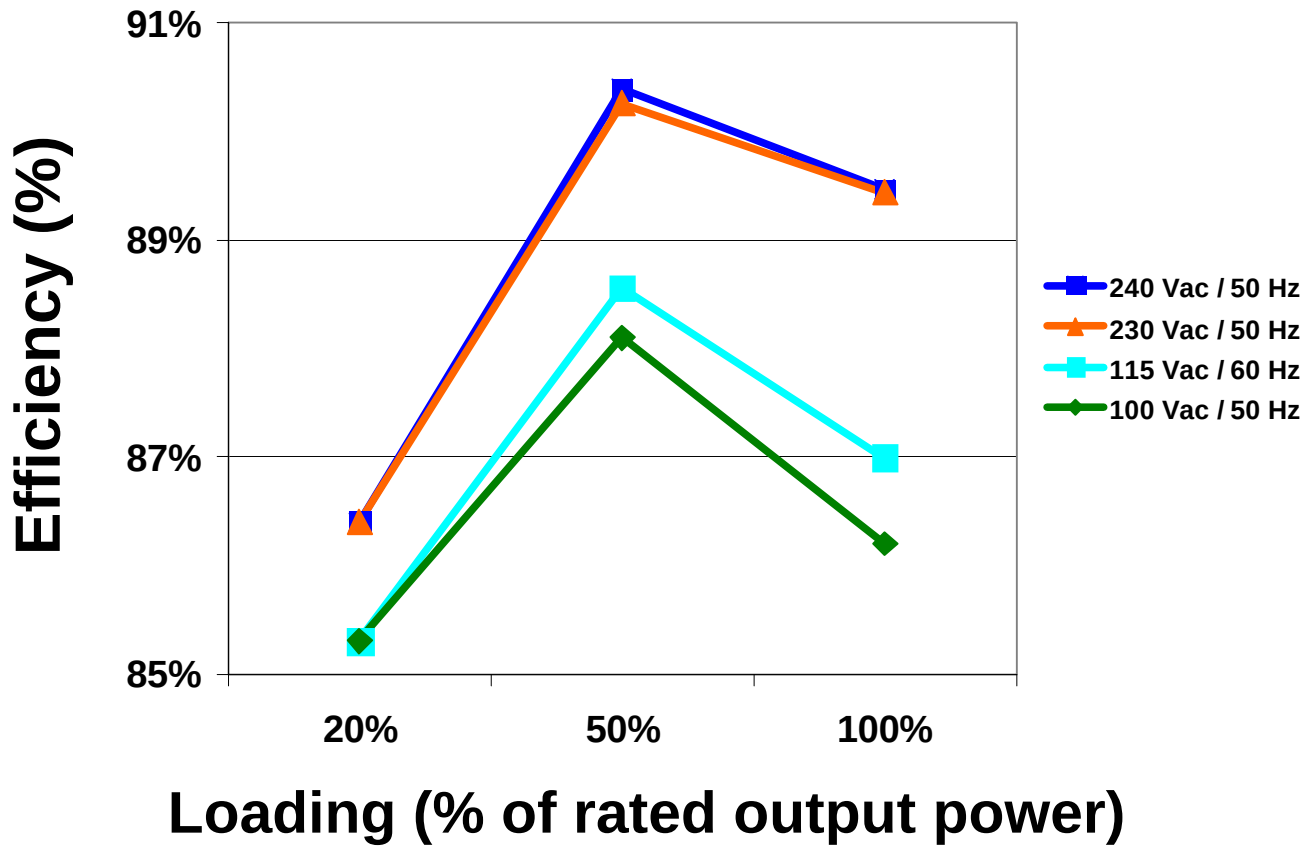
- PF = 0.991 at 230 Vac input, full load
- PF = 0.952 at 230 Vac, input, 50 % load

Efficiency Results

Input	20% Load	50% Load	100% Load
100 Vac	85.35%	88.61%	86.78%
115 Vac	85.57%	89.12%	87.59%
230 Vac	86.25%	90.69%	89.73%
240 Vac	86.69%	90.93%	89.86%
Requirement @ 115 Vac	**85%**	**88%**	**85%**

Efficiency Results

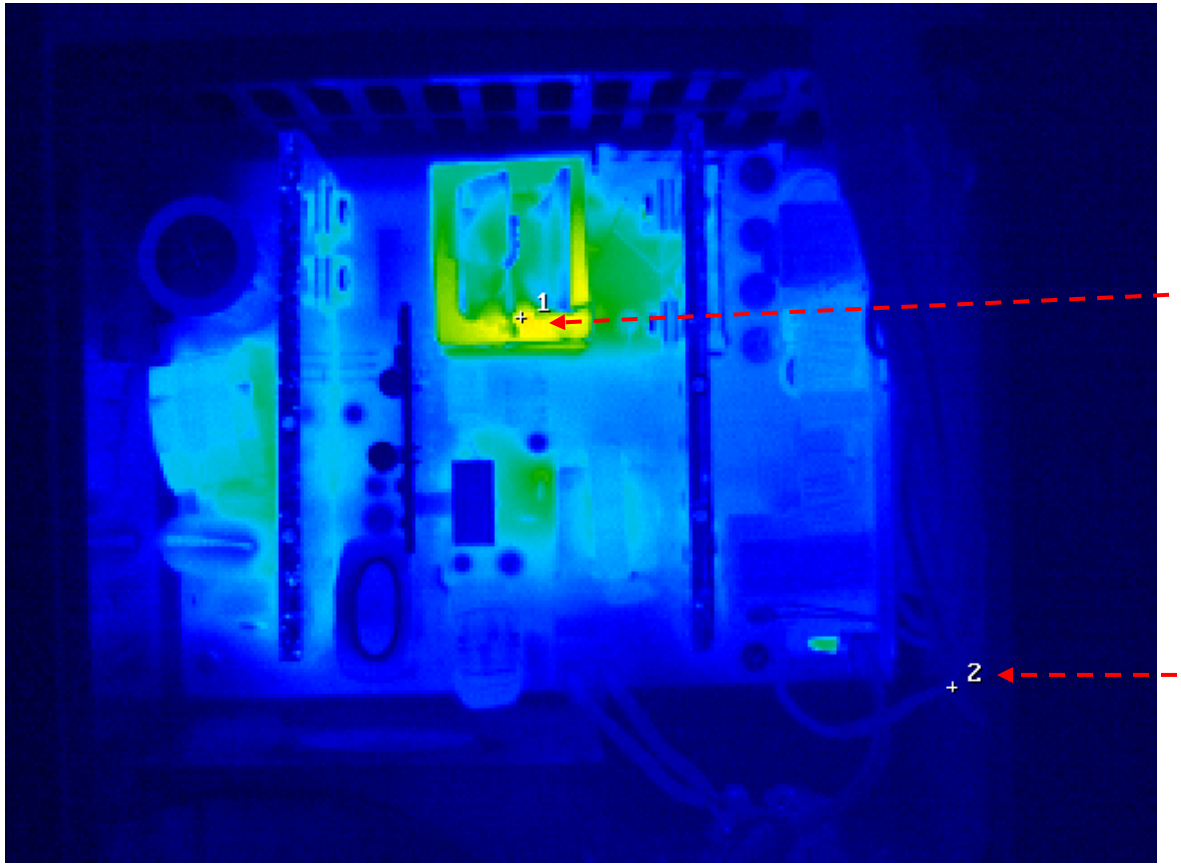
Efficiency > 85% @ 4 line voltages and 3 loads



The Output Voltage Regulation

Load	DC Terminal Voltage (V) & DC Load Current (A)											
	$12V_A$		$12V_B$		5V		3.3V		5Vsb		-12V	
(%)	(V)	(A)	(V)	(A)	(V)	(A)	(V)	(A)	(V)	(A)	(V)	(A)
20	12.01	1.90	12.02	1.03	5.01	1.89	3.25	1.01	4.99	0.48	-12.78	0.06
50	11.97	4.75	11.97	2.56	4.98	4.71	3.22	2.52	4.96	1.20	-12.37	0.16
100	11.86	9.50	11.87	5.12	4.93	9.43	3.18	5.02	4.91	2.39	-11.95	0.32

The Thermal Result @ 100 Vac, Full load



LLC-HB transformer is 85℃

The ambient temperature outside the case is around 33 ℃

- The thermal performance is optimized.

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Summary

- In order to obtain high overall efficiency for the power supply, up-front architectural considerations and component selection for each stage are critical
- A soft-switching topology, coupled with highly efficient PFC stage and output stage are required to meet the new efficiency requirements of the OEMs
- ON Semiconductor's 85% PLUS reference design offers a fully tested, robust and cost-effective solution
  - This solution can be optimized for higher efficiencies and other output power ratings

For More Information

- View the extensive portfolio of power management products from ON Semiconductor at www.onsemi.com
- View reference designs, design notes, and other material supporting the design of highly efficient power supplies at www.onsemi.com/powersupplies