The SN74LS85 is a 4-Bit Magnitude Comparator which compares two 4-bit words (A, B), each word having four Parallel Inputs (A0−A3, B0−B3); A3, B3 being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monotonic code. Three Outputs are provided: “A greater than B” (OA>B), “A less than B” (OA<B), “A equal to B” (OA=B). Three Expander Inputs, IA>B, IA<B, IA=B, allow cascading without external gates. For proper compare operation, the Expander Inputs to the least significant position must be connected as follows: IA<B = IA>B = L, IA=B = H. For serial (ripple) expansion, the OA>B, OA<B and OA=B Outputs are connected respectively to the IA>B, IA<B, and IA=B Inputs of the next most significant comparator, as shown in Figure 1. Refer to Applications section of data sheet for high speed method of comparing large words.

The Truth Table on the following page describes the operation of the SN74LS85 under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a series expansion scheme. The lower five lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

- Easily Expandable
- Binary or BCD Comparison
- OA>B, OA<B, and OA=B Outputs Available

### GUARANTEED OPERATING RANGES

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Supply Voltage</td>
<td>4.75</td>
<td>5.0</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>TA</td>
<td>Operating Ambient Temperature Range</td>
<td>0</td>
<td>25</td>
<td>70</td>
<td>°C</td>
</tr>
<tr>
<td>IOH</td>
<td>Output Current – High</td>
<td></td>
<td></td>
<td>−0.4</td>
<td>mA</td>
</tr>
<tr>
<td>IOL</td>
<td>Output Current – Low</td>
<td></td>
<td></td>
<td>8.0</td>
<td>mA</td>
</tr>
</tbody>
</table>

### ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Shipping</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74LS85N</td>
<td>16 Pin DIP</td>
<td>2000 Units/Box</td>
</tr>
<tr>
<td>SN74LS85D</td>
<td>SOIC−16</td>
<td>38 Units/Rail</td>
</tr>
<tr>
<td>SN74LS85DR2</td>
<td>SOIC−16</td>
<td>2500/Tape &amp; Reel</td>
</tr>
<tr>
<td>SN74LS85M</td>
<td>SOEIAJ−16</td>
<td>See Note 1</td>
</tr>
<tr>
<td>SN74LS85MEL</td>
<td>SOEIAJ−16</td>
<td>See Note 1</td>
</tr>
</tbody>
</table>

1. For ordering information on the EIAJ version of the SOIC package, please contact your local ON Semiconductor representative.
SN74LS85

CONNECTION DIAGRAM DIP (TOP VIEW)

VCC A3 B2 A2 A1 B1 A0 B0
16 15 14 13 12 11 10 9

B3 IA<_B IA>_B IA=B OA>_B OA<_B OA=B GND
1 2 3 4 5 6 7 8

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

<table>
<thead>
<tr>
<th>PIN</th>
<th>FUNCTION</th>
<th>HIGH (U.L.)</th>
<th>LOW (U.L.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IA&gt;_B</td>
<td>A &gt; B Expander Inputs</td>
<td>1.5 U.L.</td>
<td>0.75 U.L.</td>
</tr>
<tr>
<td>IA&lt;_B</td>
<td>A &lt; B, A &gt; B, Expander Inputs</td>
<td>1.5 U.L.</td>
<td>0.75 U.L.</td>
</tr>
<tr>
<td>OA&gt;_B</td>
<td>A Greater than B Output</td>
<td>10 U.L.</td>
<td>5 U.L.</td>
</tr>
<tr>
<td>OA&lt;_B</td>
<td>B Greater than A Output</td>
<td>10 U.L.</td>
<td>5 U.L.</td>
</tr>
<tr>
<td>OA=B</td>
<td>A Equal to B Output</td>
<td>10 U.L.</td>
<td>5 U.L.</td>
</tr>
</tbody>
</table>

LOADING (Note a)

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

LOGIC SYMBOL

VCC = PIN 16
GND = PIN 8

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LOGIC DIAGRAM

TRUTH TABLE

<table>
<thead>
<tr>
<th>COMPARING INPUTS</th>
<th>CASCADING INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>A&gt;B</td>
</tr>
<tr>
<td>A3&gt;B3</td>
<td>X X X</td>
<td>H L L</td>
</tr>
<tr>
<td>A3=B3</td>
<td>X X X</td>
<td>H L L</td>
</tr>
<tr>
<td>A3=B3 A2&gt;B2</td>
<td>X X X</td>
<td>H L L</td>
</tr>
<tr>
<td>A3=B3 A2=B2</td>
<td>X X X</td>
<td>H L L</td>
</tr>
<tr>
<td>A3=B3 A2=B2 A1&gt;B1</td>
<td>X X X</td>
<td>H L L</td>
</tr>
<tr>
<td>A3=B3 A2=B2 A1=B1</td>
<td>X X X</td>
<td>H L L</td>
</tr>
<tr>
<td>A3=B3 A2=B2 A1=B1 A0&gt;B0</td>
<td>X X X</td>
<td>H L L</td>
</tr>
<tr>
<td>A3=B3 A2=B2 A1=B1 A0=B0</td>
<td>H L L</td>
<td>H L L</td>
</tr>
<tr>
<td>A3=B3 A2=B2 A1=B1 A0=B0</td>
<td>H L L</td>
<td>H L L</td>
</tr>
<tr>
<td>A3=B3 A2=B2 A1=B1 A0=B0</td>
<td>H L L</td>
<td>L L H</td>
</tr>
<tr>
<td>A3=B3 A2=B2 A1=B1 A0=B0</td>
<td>H L L</td>
<td>L L H</td>
</tr>
<tr>
<td>A3=B3 A2=B2 A1=B1 A0=B0</td>
<td>H L L</td>
<td>L L H</td>
</tr>
</tbody>
</table>

H = HIGH Level
L = LOW Level
X = IMMATERIAL

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NOTE:
The SN74LS85 can be used as a 5-bit comparator only when the outputs are used to drive the A0−A3 and B0−B3 inputs of another SN74LS85 as shown in Figure 2 in positions #1, 2, 3, and 4.

Figure 1. Comparing Two n-Bit Words

APPLICATIONS

Figure 2 shows a high speed method of comparing two 24-bit words with only two levels of device delay. With the technique shown in Figure 1, six levels of device delay result when comparing two 24-bit words. The parallel technique can be expanded to any number of bits, see Table 1.

Table 1

<table>
<thead>
<tr>
<th>WORD LENGTH</th>
<th>NUMBER OF PKGS.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1−4 Bits</td>
<td>1</td>
</tr>
<tr>
<td>5−24 Bits</td>
<td>2−6</td>
</tr>
<tr>
<td>25−120 Bits</td>
<td>8−31</td>
</tr>
</tbody>
</table>

NOTE:
The SN74LS85 can be used as a 5-bit comparator only when the outputs are used to drive the A0−A3 and B0−B3 inputs of another SN74LS85 as shown in Figure 2 in positions #1, 2, 3, and 4.

Figure 2. Comparison of Two 24-Bit Words

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**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input HIGH Voltage</td>
<td>2.0</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input LOW Voltage</td>
<td></td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IK}$</td>
<td>Input Clamp Diode Voltage</td>
<td>−0.65</td>
<td>−1.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output HIGH Voltage</td>
<td>2.7</td>
<td>3.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output LOW Voltage</td>
<td>0.25</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.35</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Input HIGH Current</td>
<td>20</td>
<td></td>
<td>60</td>
</tr>
<tr>
<td></td>
<td>A &lt; B, A &gt; B, Other Inputs</td>
<td></td>
<td>0.1</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input LOW Current</td>
<td>−0.4</td>
<td></td>
<td>−1.2</td>
</tr>
<tr>
<td></td>
<td>A &lt; B, A &gt; B, Other Inputs</td>
<td></td>
<td>0.1</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Output Short Circuit Current (Note 2)</td>
<td>−20</td>
<td>−100</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Power Supply Current</td>
<td>20</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

2. Not more than one output should be shorted at a time, nor for more than 1 second.

**AC CHARACTERISTICS** ($T_A = 25^\circ \text{C}, V_{CC} = 5.0 \text{ V}$)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>Any A or B to A &lt; B, A &gt; B</td>
<td>24</td>
<td>36</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>Any A or B to A = B</td>
<td>20</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>A &lt; B or A &gt; B to A &gt; B</td>
<td>14</td>
<td>22</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>A = B to A = B</td>
<td>13</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>A &gt; B or A = B to A &lt; B</td>
<td>14</td>
<td>22</td>
<td>ns</td>
</tr>
</tbody>
</table>

Figure 3.

**AC WAVEFORMS**

![AC Waveform Diagram](image-url)
SN74LS85

PACKAGE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R

NOTES:
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

<table>
<thead>
<tr>
<th>DIMENSIONS</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.740 (0.029)</td>
</tr>
<tr>
<td>B</td>
<td>0.250 (0.010)</td>
</tr>
<tr>
<td>C</td>
<td>0.155 (0.006)</td>
</tr>
<tr>
<td>D</td>
<td>0.015 (0.001)</td>
</tr>
<tr>
<td>F</td>
<td>0.040 (0.001)</td>
</tr>
<tr>
<td>G</td>
<td>0.100 BSC</td>
</tr>
<tr>
<td>H</td>
<td>0.000 BSC</td>
</tr>
<tr>
<td>J</td>
<td>0.008 (0.000)</td>
</tr>
<tr>
<td>K</td>
<td>0.110 (0.004)</td>
</tr>
<tr>
<td>L</td>
<td>0.295 (0.012)</td>
</tr>
<tr>
<td>M</td>
<td>0.250 (0.010)</td>
</tr>
<tr>
<td>S</td>
<td>0.200 (0.008)</td>
</tr>
</tbody>
</table>

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

<table>
<thead>
<tr>
<th>DIMENSIONS</th>
<th>INCHES</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>9.80 10.00</td>
</tr>
<tr>
<td>B</td>
<td>3.80 4.00</td>
</tr>
<tr>
<td>C</td>
<td>1.35 1.75</td>
</tr>
<tr>
<td>D</td>
<td>0.35 0.49</td>
</tr>
<tr>
<td>F</td>
<td>0.40 1.25</td>
</tr>
<tr>
<td>G</td>
<td>1.27 BSC</td>
</tr>
<tr>
<td>J</td>
<td>0.10 0.25</td>
</tr>
<tr>
<td>K</td>
<td>0.10 0.25</td>
</tr>
<tr>
<td>M</td>
<td>0.007</td>
</tr>
<tr>
<td>P</td>
<td>0.50 0.55</td>
</tr>
<tr>
<td>R</td>
<td>0.25 0.50</td>
</tr>
</tbody>
</table>

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PACKAGE DIMENSIONS

M SUFFIX
SOEIAJ PACKAGE
CASE 966–01
ISSUE O

MILLIMETERS INCHES

<table>
<thead>
<tr>
<th>DIM</th>
<th>MIN</th>
<th>MAX</th>
<th>MIN</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>2.05</td>
<td>0.081</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>0.06</td>
<td>0.021</td>
<td>0.007</td>
<td>0.033</td>
</tr>
<tr>
<td>C</td>
<td>0.50</td>
<td>0.020</td>
<td>0.033</td>
<td>0.035</td>
</tr>
<tr>
<td>D</td>
<td>0.18</td>
<td>0.008</td>
<td>0.014</td>
<td>0.020</td>
</tr>
<tr>
<td>E</td>
<td>0.35</td>
<td>0.014</td>
<td>0.020</td>
<td>0.020</td>
</tr>
<tr>
<td>J</td>
<td>0.70</td>
<td>0.028</td>
<td>0.035</td>
<td>0.035</td>
</tr>
</tbody>
</table>

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.05 (0.002) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.06 (0.024).

**M SUFFIX**

SOEIAJ PACKAGE
CASE 966–01

**NOTES:**
2. CONTROLLING DIMENSION: MILLIMETER.
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**REFERENCES:**

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- DRAWING

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- DRAWING

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3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.05 (0.002) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.06 (0.024).

**REFERENCES:**

- PACKAGE DIMENSIONS
- DRAWING

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