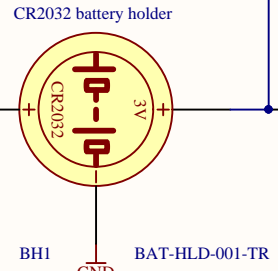
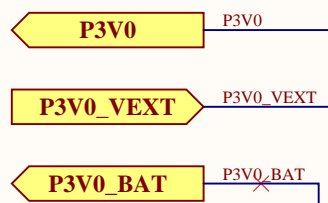
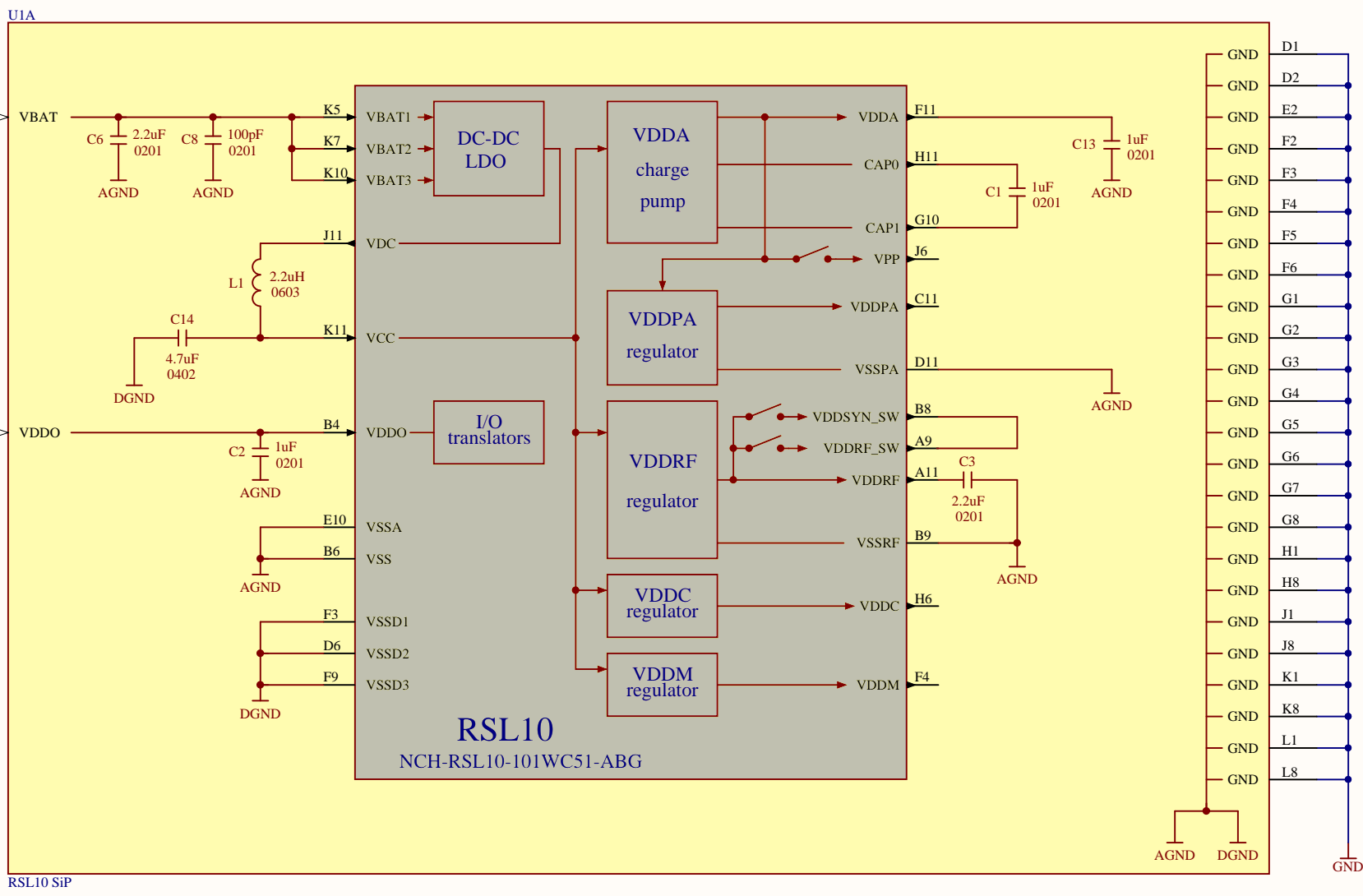


RSL10-SENSE-GEVB		Assembly variant:	State:
<i>Top level block diagram</i>		<i>standard_board</i>	<i>released</i>
Revision: 1.1	Repository revision: TBD		ON Semiconductor Solution Engineering Center Piešťany
Engineer: Tomas Duris	7.Dec 2018 20:10		
File: RSL10_SENSE_GEVB.SchDoc	1/4		



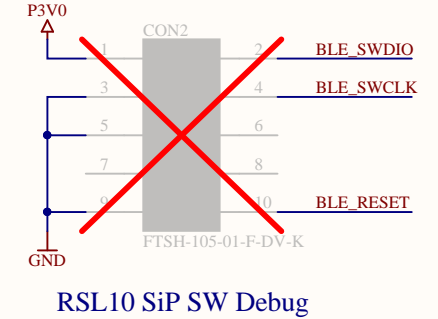
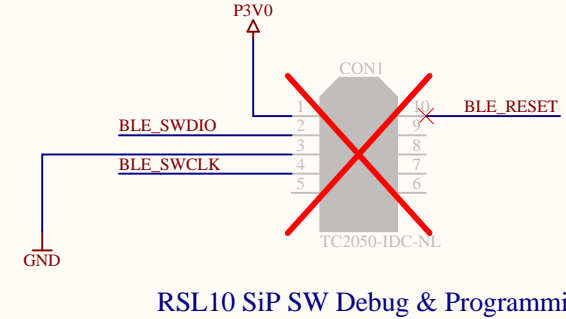
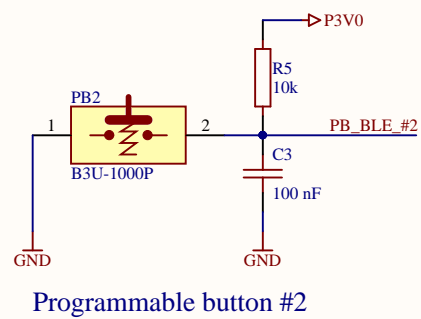
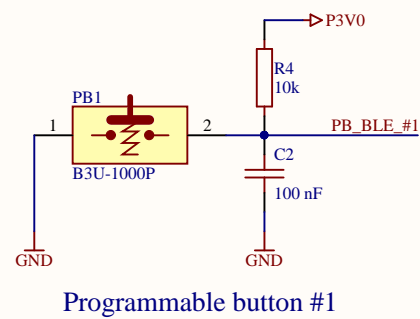
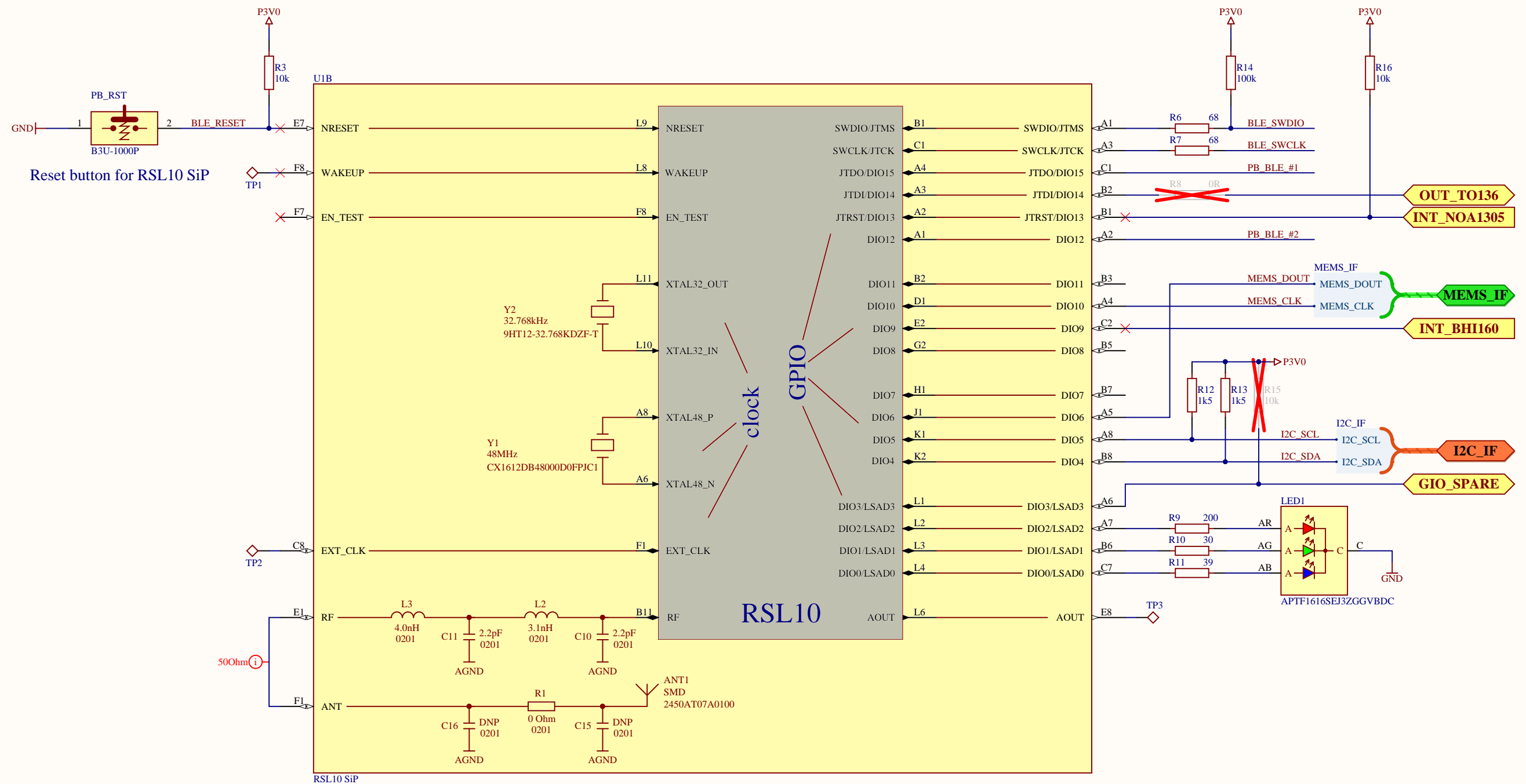


Coin cell battery 3V 220mAh

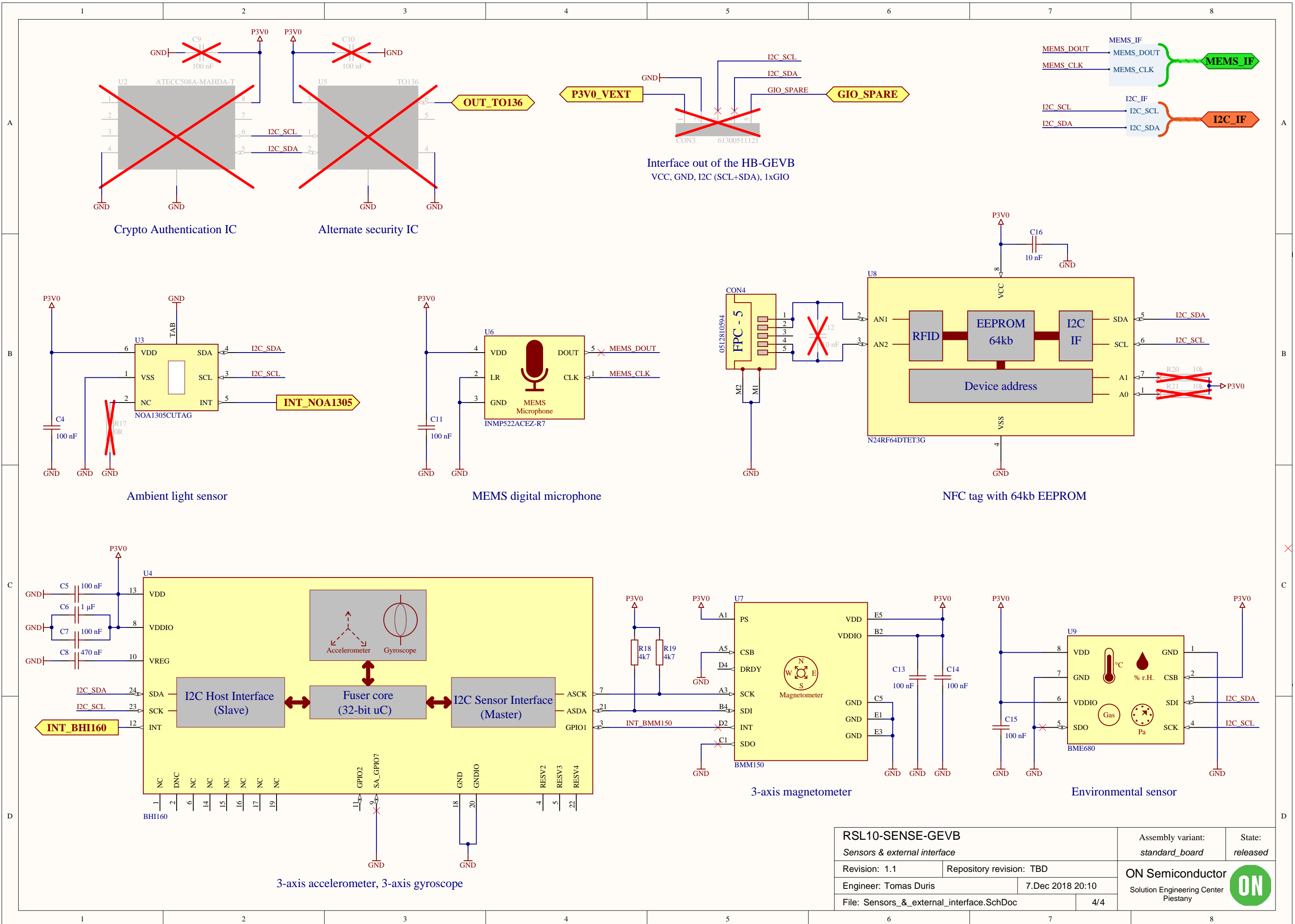


RSL10-SENSE-GEVB		Assembly variant:	State:
<i>RSL10 SiP power management</i>		<i>standard_board</i>	<i>released</i>
Revision: 1.1	Repository revision: TBD		ON Semiconductor Solution Engineering Center Piešťany
Engineer: Tomas Duris	7.Dec 2018 20:10		
File: RSL10_SiP_power.SchDoc	2/4		





RSL10-SENSE-GEVB		Assembly variant:	State:
RSL 10 SiP signals		standard_board	released
Revision: 1.1	Repository revision: TBD		ON Semiconductor Solution Engineering Center Piestany
Engineer: Tomas Duris	7.Dec 2018 20:10		
File: RSL10_SiP_signals.SchDoc	3/4		



RSL10-SENSE-GEVB		Assembly variant:	State:
Sensors & external interface		standard_board	released
Revision: 1.1	Repository revision: TBD	ON Semiconductor Solution Engineering Center Piešťany	
Engineer: Tomas Duris	7.Dec 2018 20:10		
File: Sensors_&_external_interface.SchDoc	4/4		