I3T80

Process Technology

I3T80: 0.35 μm Process Technology

ON Semiconductor®

www.onsemi.com

Overview

Providing the density of a 0.35 μm digital process, analog/mixed−signal capability and high voltage, the ON Semiconductor Intelligent Interface Technology I3T80 process is the answer to the need for increased digital content in a mixed−signal and/or high voltage environment. Featuring high voltage devices up to 80 V as well as digital and analog operation at 3.3 V, the I3T80 process family features a wide range of capabilities in a single IC.

Features

- 3 to 5 Metal Layers
- Metal to Metal (MIM) Linear Capacitors
- High, Medium, and Low Resistivity Polysilicon Resistors
- Floating High−Voltage NDMOS and PDMOS Transistors
- Floating Medium−Voltage NDMOS Transistors
- Floating High− and Low−Voltage Diodes
- Medium−Voltage NPN Bipolar Transistors
- Medium−Voltage PNP Bipolar Transistors (Collector Grounded, High and Low Gain)
- Zener Zap Diode for OTP
- Buried Zener Diode for Clamping
- Polysilicon Clamping Diode
- High− and Medium−Voltage Floating Metal Capacitors
- Deep N+ Doped Guard Rings

PROCESS CHARACTERISTICS

Operating Voltage	3.3 V
Substrate Material	N−epitaxy on P−sub, Retrograde Wells
Drawn Transistor Length	0.35 μm
Gate Oxide Thickness	7.0 nm
Contact/Via Size	0.4 μm
Contacted Gate Pitch	1.3 μm
Top Metal Thickness	1020 nm
Metal Pitch	
Metal 1	1.0 μm
Metal 2	1.1 μm
Top Metal	1.4 μm
Contacted Metal Pitch	
Metal 1/ CNT	1.1 μm
Metal 1/ Via 1	1.2 μm
Metal 2 to Top 1 / Via	1.2 μm
Metal Composition	Al/Cu
Isolation	LOCOS
ILD Planarization	USG/BPTEOS+CMP
IMD Planarization	HDP/PETEOS+CMP

SAMPLE PROCESS OPTIONS

	Mask Layers
3 Metal, 80 V, MIMC, HIPO, OTP	23
4 Metal, 80 V, MIMC, HIPO, OTP	25
5 Metal, 80 V, MIMC, HIPO, OTP, Flash EEPROM	28

DEVICE CHARACTERISTICS

All Values Typical at 25°C

LOW−VOLTAGE TRANSISTORS

NMOS Transistor	Typical Value	Units
Vt (10/0.35, linear extrapolated)	0.59	V
Vmax = Vbd	3.6	V
IDS (10/0.35, Vds = Vgs = 3.3 V)	530	μA/μm
PMOS Transistor	**Typical Value**	**Units**
Vt (10/0.35, linear extrapolated)	−0.57	V
Vmax = Vbd	−3.6	V
IDS (10/0.35, Vds = Vgs = 3.3 V)	−250	μA/μm

HIGH−VOLTAGE TRANSISTORS

Floating NMOS @ 80 V	Typical Value	Units
Vt (10/0.35, linear extrapolated)	0.59	V
Vmax = Vfloat to P−substrate	80	V
Vmax = Vbd	3.6	V
IDS (10/0.35, Vds = Vgs = 3.3 V)	530	μA/μm
Floating PMOS @ 80 V	**Typical Value**	**Units**
Vt (10/0.35, linear extrapolated)	−0.57	V
Vmax = Vfloat to P−substrate	80	V
Vmax = Vbd	−3.6	V
IDS (10/0.35, Vds = Vgs = 3.3 V)	−250	μA/μm
Floating NDMOS for Switching Application: VFNDM80	**Typical Value**	**Units**
Vt	0.54	V
Vmax = Vbd (higher if self protected)	70	V
Vgsmax (full lifetime)	3.6	V
Ids (Vds = 40, Vgs = 1.5 V)	100	μA/μm
Ron*Area (block of 16 fingers) Without isolation With isolation	 180 260	mΩ*mm^2
Floating NDMOS for Analog Application: VFNDM80A	**Typical Value**	**Units**
Vt	0.56	V
Vmax = Vbd (higher if self protected)	70	V
Vgsmax (full lifetime)	3.6	V
Ids (Vds = 40, Vgs = 1.5 V)	70	μA/μm
Ron*Area (block of 16 fingers) Without isolation With isolation	 250 325	mΩ*mm^2

Floating Medium Voltage NDMOS	Typical Value	Units
Vt	0.58	V
Vmax = Vbd	14	V
Vgsmax (full lifetime)	3.6	V
Ids (Vds = 10 V, Vgs = 3.3 V)	300	μA/μm
Ron*Area	31	mΩ*mm^2
Floating HV PMOS: LFPDM80	**Typical Value**	**Units**
Vt (W = 40 mm)	−0.56	V
Vmax = Vbd	−70	V
Vgsmax (full lifetime)	−3.6	V
Ids (Vds = 40 V, Vgs = 1.5 V)	18.5	μA/μm
Ron*Area	280	mΩ*mm^2
Floating PDMOS: LFPDMS	**Typical Value**	**Units**
Vt	−0.56	V
Vmax = Vbd	−5.5	V
Vgsmax	−3.6	V
Ids (Vds = 5 V, Vgs = 3.3 V)	96	μA/μm

DIODES

Zener Diode: PBZD (a = 2 μm)	Typical Value	Units
Vz @ 100 μA	4.6	V
Rzener	45	Ω
Ileak @ Vz = 0.5 V	200	nA
Zapping Zener Diode for OTP: UZZD	**Typical Value**	**Units**
Vz @ 1 A	1.5	V
Vbd @ 10 mA	4.5	V
Ileak_max @ Vz = 1 V	1.4	mA
Floating High Voltage Diode: FID80	**Typical Value**	**Units**
Vak_reverse, Ia = 100 nA	> 80	V
Vak_forw, Ik = 100 μA	0.79	V
Isub/IA, Va = 0.7 V	0.5	%
Poly Diode for Gate Clamping: POLYD	**Typical Value**	**Units**
Vreverse @ Ia = 10 μA	6.8	V
Ileak/W @ Vrev = 3.6 V	< 20	nA/μm

BIPOLAR TRANSISTORS

Vertical Medium−Voltage PNP: VPB (Parameter, E_area = 0.64 μm²)	Typical Value	Units
Hfe @ Ic = 10 μA	8	−
Bvceo @ Ic = 1 μA	−63	V
Bvces @ Ic = 1 μA	−67	V
Icmax	250	μA
Vertical Medium−Voltage "High−Gain" PNP Transistor: VPHB (Parameter, E_area = 0.64 μm²)	**Typical Value**	**Units**
Hfe @ Ic = 100 nA	115	−
|Bvceo| @ Ic = 1 μA	> 80	V
|Bvces| @ Ic = 1 μA	> 100	V
Icmax	250	μA
Medium−Voltage NPN (Parameter, E_area = 16 μm²)	**Typical Value**	**Units**
Hfe max	120	−
Bvceo @ Ic = 1 μA	23	V
Bvces @ Ic = 1 μA	> 80	V
|Vearly|	> 70	V

CAPACITORS (PARAMETER @ 25°C)

Type (Maximum Voltage)	Typical Value	Units
Metal2 / Metal2.5 Plate: MIMC (3.6 V)	1.5	fF/μm²
Metal1 / Metal3 Plate (80 V)	0.1	fF/μm²
Poly / Metal3 Plate (80 V)	0.14	fF/μm²
Metal1 / Metal3 Bar (80 V)	0.26	aF/μm/ finger
Poly / Metal3 Bar (80 V)	0.33	aF/μm/ finger

RESISTORS (PARAMETER @ 25°C)

Resistor Type	Typical Value	Units
High−Resistance Poly: HIPO	975	Ω/square
Salicided P+ Poly: LOPOR	2.4	Ω/square
Unsalicided P+ Poly: PPOLR	240	Ω/square
Unsalicided P+ in Mwell	64	Ω/square
Unsalicided N+ Poly: NPOLR	292	Ω/square
Unsalicided N+ in Pwell	47.5	Ω/square
Nwell under FOX (field oxide)	958	Ω/square
Nwell in AA (active area)	800	Ω/square
Pwell in AA (active area)	1755	Ω/square

LIBRARIES

Standard Cell	
Ultra High Density Core Shell	pn sum: 2.0
	Area of 2−input nand (na21): 38.88 μm²
	Gate density (na21 @ 100% utilization): 25.72 k gates/mm²
	Scan Flop density (scan flops @ 100% utilization): 3.215 k ff/mm²
	Average power (@ 3.3 V): 0.2929 μW/MHz/gate
Standard I/O	
Fat Pad I/O Library (for core limited designs)	190.80 μm min in−line pad pitch
	203.40 μm pad height
Tall Pad I/O Library (for pad limited designs)	97.20 μm min in−line pad pitch
	374.40 μm pad height

MEMORY OPTIONS

RAM	
Synchronous High Speed / High Temp Single Port SRAM	Minimum: 16 words x 2 bits
	Maximum: 128 k bits (i.e: 16 k words x 8 bits, 8 k words x 16 bits, …)
Synchronous High Speed / High Temp Dual Port SRAM	Minimum: 16 words x 2 bits
	Maximum: 128 k bits (i.e: 16 k words x 8 bits, 8 k words x 16 bits, …)
Low Power Synchronous SRAM	Minimum: 64 words x 4 bits
	Maximum: 128 k bits (i.e: 16 k words x 8 bits, 8 k words x 16 bits, …)
ROM	
Synchronous High Speed / High Temp Diffusion ROM	Minimum: 256 words x 4 bits
	Maximum: 512 k bits (i.e: 64 k words x 8 bits, 32 k words x 16 bits, …)
Low Power Synchronous Via Programmable ROM	Minimum: 256 words x 4 bits
	Maximum: 512 k bits (i.e: 64 k words x 8 bits, 32 k words x 16 bits, …)
Non−Volatile Memory	
OTP − One Time Programmable	Fuse: Zener Diode optimized for low power zapping
	Both Serial and Parallel Output Capability
	In field programming available
	Vector: Up to 320 bits

CAD TOOL COMPATIBILITY

Digital Design	Synopsys Design Compiler
	Cadence Verilog
Analog Design	Cadence DFII (4.4.6)
	Spectre
Place and Route	Synopsys Apollo
	Cadence Silicon Ensemble
Physical Verification	Mentor Graphics Calibre

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative