FDBL86062-F085

N-Channel POWERTRENCH® MOSFET

100 V, 300 A, 2.0 mΩ

Features
• Typical $R_{DS(on)} = 1.5 \, \text{mΩ}$ at $V_{GS} = 10 \, \text{V}$, $I_D = 80 \, \text{A}$
• Typical $Q_{g(tot)} = 95 \, \text{nC}$ at $V_{GS} = 10 \, \text{V}$, $I_D = 80 \, \text{A}$
• UIS Capability
• Qualified to AEC Q101
• This Device is Pb–Free and is RoHS Compliant

Applications
• Automotive Engine Control
• PowerTrain Management
• Solenoid and Motor Drivers
• Integrated Starter/Alternator
• Primary Switch for 12 V Systems
# MOSFET Maximum Ratings

- **Symbol**: \( V_{DSS} \)
  - **Parameter**: Drain-to-Source Voltage
  - **Rating**: 100 V
  - **Units**: V

- **Symbol**: \( V_{GS} \)
  - **Parameter**: Gate-to-Source Voltage
  - **Rating**: \( \pm 20 \) V

- **Symbol**: \( I_D \)
  - **Parameter**: Drain Current - Continuous (\( V_{GS} = 10 \)) (Note 1) \( T_C = 25^\circ \)C
  - **Rating**: 300 A
  - **Parameter**: Pulsed Drain Current \( T_C = 25^\circ \)C
  - **Rating**: See Figure 4

- **Symbol**: \( E_{AS} \)
  - **Parameter**: Single Pulse Avalanche Energy (Note 2)
  - **Rating**: 352 mJ

- **Symbol**: \( P_D \)
  - **Parameter**: Power Dissipation
  - **Rating**: 429 W
  - **Parameter**: Derate Above 25°C
  - **Rating**: 2.9 W/°C

- **Symbol**: \( T_J, T_{STG} \)
  - **Parameter**: Operating and Storage Temperature
  - **Rating**: –55 to +175 °C

- **Symbol**: \( R_{JC} \)
  - **Parameter**: Thermal Resistance, Junction to Case
  - **Rating**: 0.35 °C/W

- **Symbol**: \( R_{JA} \)
  - **Parameter**: Maximum Thermal Resistance, Junction to Ambient (Note 3)
  - **Rating**: 43 °C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by silicon.
2. Starting \( T_J = 25^\circ \)C, \( L = 0.1 \) mH, \( I_{AS} = 84 \) A, \( V_{DD} = 100 \) V during inductor charging and \( V_{DD} = 0 \) V during time in avalanche.
3. \( R_{JA} \) is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. \( R_{JC} \) is guaranteed by design, while \( R_{JA} \) is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

## Package Marking and Ordering Information

<table>
<thead>
<tr>
<th>Device Marking</th>
<th>Device</th>
<th>Package</th>
<th>Reel Size</th>
<th>Tape Width</th>
<th>Quantity</th>
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<tr>
<td>FDBL86062</td>
<td>FDBL86062--F085</td>
<td>MO--299A</td>
<td>13&quot;</td>
<td>24 mm</td>
<td>2000 Units</td>
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</table>

## Electrical Characteristics

- **Symbol**: \( V_{GS(th)} \)
  - **Parameter**: Gate to Source Threshold Voltage
  - **Test Conditions**: \( V_{DS} = V_{GS} = 0 \) V
  - **Rating**: 2.0 – 3.1 – 4.5 V

- **Symbol**: \( R_{DS(on)} \)
  - **Parameter**: Drain to Source On Resistance
  - **Test Conditions**: \( I_D = 80 \) A, \( V_{GS} = 10 \) V
  - **Rating**: \( T_J = 25^\circ \)C – 1.5 – 2.0 mΩ

- **Symbol**: \( Q_{g(Tot)} \)
  - **Parameter**: Total Gate Charge at 10 V
  - **Test Conditions**: \( V_{GS} = 0 \) to 10 V
  - **Rating**: \( V_{DD} = 80 \) V

- **Symbol**: \( Q_{gs} \)
  - **Parameter**: Gate-to-Source Gate Charge
  - **Test Conditions**: \( V_{GS} = 0 \) to 2 V

- **Symbol**: \( Q_{gd} \)
  - **Parameter**: Gate-to-Drain “Miller” Charge
  - **Test Conditions**: \( V_{GS} = 0 \) to 2 V

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### ELECTRICAL CHARACTERISTICS (continued) $T_J = 25^\circ C$, unless otherwise noted

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
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<tr>
<td>$t_{on}$</td>
<td>Turn–On Time</td>
<td>$V_{DD} = 50,V$, $I_D = 80,A$, $V_{GS} = 10,V$, $R_{GEN} = 6,\Omega$</td>
<td>–</td>
<td>–</td>
<td>73</td>
<td>ns</td>
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<td>$t_{d(on)}$</td>
<td>Turn–On Delay</td>
<td>–</td>
<td>31</td>
<td>–</td>
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<tr>
<td>$t_r$</td>
<td>Rise Time</td>
<td>–</td>
<td>25</td>
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<tr>
<td>$t_{d(off)}$</td>
<td>Turn–Off Delay</td>
<td>–</td>
<td>36</td>
<td>–</td>
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<tr>
<td>$t_f$</td>
<td>Fall Time</td>
<td>–</td>
<td>9</td>
<td>–</td>
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<tr>
<td>$t_{off}$</td>
<td>Turn–Off Time</td>
<td>–</td>
<td>59</td>
<td>–</td>
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### DRAIN–SOURCE DIODE CHARACTERISTICS

| $V_{SD}$ | Source–to–Drain Diode Voltage | $I_{SD} = 80\,A$, $V_{GS} = 0\,V$ | – | – | 1.25 | V |
| $I_{SD} = 40\,A$, $V_{GS} = 0\,V$ | – | – | 1.2 |

| $I_{r}$ | Reverse–Recovery Time | $I_R = 80\,A$, $dI_{SD}/dt = 100\,A/\mu s$, $V_{DD} = 80\,V$ | – | 115 | 150 | ns |
| $Q_{rr}$ | Reverse–Recovery Charge | – | 172 | 224 | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at $T_J = 175^\circ C$. Product is not tested to this condition in production.
TYPICAL CHARACTERISTICS

Figure 1. Normalized Power Dissipation vs. Case Temperature

Figure 2. Maximum Continuous Drain Current vs. Case Temperature

Figure 3. Normalized Maximum Transient Thermal Impedance

Figure 4. Peak Current Capability
TYPICAL CHARACTERISTICS (continued)

Figure 5. Forward Bias Safe Operating Area

Figure 6. Unclamped Inductive Switching Capability

Figure 7. Transfer Characteristics

Figure 8. Forward Diode Characteristics

Figure 9. Saturation Characteristics

Figure 10. Saturation Characteristics
TYPICAL CHARACTERISTICS (continued)

Figure 11. $R_{DSON}$ vs. Gate Voltage

Figure 12. Normalized $R_{DSON}$ vs. Junction Temperature

Figure 13. Normalized Gate Threshold Voltage vs. Temperature

Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

Figure 15. Capacitance vs. Drain to Source Voltage

Figure 16. Gate Charge vs. Gate to Source Voltage

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NOTES: UNLESS OTHERWISE SPECIFIED
A) PACKAGE STANDARD REFERENCE:
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS
   OR MOLD FLASH. MOLD FLASH OR
   BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER
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<th>REVISION</th>
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