**MOSFET** – N-Channel, 
**POWERTRENCH®**

150 V, 79 A, 16 mΩ

**FDB2532-F085**

**Features**
- \( R_{DS(ON)} = 14 \text{ m}\Omega \) (Typ.), \( V_{GS} = 10 \text{ V}, I_D = 33 \text{ A} \)
- \( Q_g \) (tot) = 82 nC (Typ.), \( V_{GS} = 10 \text{ V} \)
- Low Miller Charge
- Low \( Q_{RR} \) Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

**Applications**
- DC/DC converters and Off-Line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 24 V and 48 V Systems
- High Voltage Synchronous Rectifier
- Direct Injection / Diesel Injection Systems
- 42 V Automotive Load Control
- Electronic Valve Train Systems
- Synchronous Rectification

See detailed ordering and shipping information on page 2 of this data sheet.
**MOSFET MAXIMUM RATINGS** (\(T_C = 25^\circ C\), Unless otherwise noted)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{DSS})</td>
<td>Drain to Source Voltage</td>
<td>150</td>
<td>V</td>
</tr>
<tr>
<td>(V_{GS})</td>
<td>Gate to Source Voltage</td>
<td>(\pm 20)</td>
<td>V</td>
</tr>
<tr>
<td>(I_D)</td>
<td>Drain Current</td>
<td>(79)</td>
<td>A</td>
</tr>
<tr>
<td>(E_{AS})</td>
<td>Single Pulse Avalanche Energy (Note 1)</td>
<td>400</td>
<td>mJ</td>
</tr>
<tr>
<td>(P_D)</td>
<td>Power Dissipation</td>
<td>(310)</td>
<td>W</td>
</tr>
<tr>
<td>(T_J, T_{STG})</td>
<td>Operating and Storage Temperature</td>
<td>(-55) to (+175)</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Starting \(T_J = 25^\circ C\), \(L = 0.5\) mH, \(I_{AS} = 40\) A

**THERMAL CHARACTERISTICS**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{JUC})</td>
<td>Thermal Resistance Junction to Case</td>
<td>0.48</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JUA})</td>
<td>Thermal Resistance Junction to Ambient, 1in² Copper Pad Area</td>
<td>43</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

**PACKAGE MARKING AND ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>Device Marking</th>
<th>Device</th>
<th>Package</th>
<th>Reel Size</th>
<th>Tape Width</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>FDB2532</td>
<td>FDB2532–F085</td>
<td>TO–263 (D²–PAK–3)</td>
<td>330 mm</td>
<td>24 mm</td>
<td>800 Units</td>
</tr>
</tbody>
</table>
## ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>OFF CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B_{VDS}</td>
<td>Drain to Source Breakdown Voltage</td>
<td>I_D = 250 μA, V_GS = 0 V</td>
<td>150</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>I_DSS</td>
<td>Zero Gate Voltage Drain Current</td>
<td>V_DS = 120 V, V_GS = 0 V</td>
<td>1</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DS = 120 V, V_GS = 0 V, T_C = 150°C</td>
<td></td>
<td></td>
<td>250</td>
<td></td>
</tr>
<tr>
<td>I_GSS</td>
<td>Gate to Source Leakage Current</td>
<td>V_GS = ±20 V</td>
<td>±100</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td><strong>ON CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{GS(TH)}</td>
<td>Gate to Source Threshold Voltage</td>
<td>V_GS = V_DS, I_D = 250 μA</td>
<td>2.0</td>
<td>4.0</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>R_{DS(ON)}</td>
<td>Drain to Source On Resistance</td>
<td>I_D = 33 A, V_GS = 10 V</td>
<td>0.014</td>
<td>0.016</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I_D = 16 A, V_GS = 6 V</td>
<td>0.016</td>
<td>0.024</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>I_D = 33 A, V_GS = 10 V, T_C = 175°C</td>
<td>0.040</td>
<td>0.048</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>DYNAMIC CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C_{iss}</td>
<td>Input Capacitance</td>
<td>V_DS = 25 V, V_GS = 0 V, f = 1 MHz</td>
<td>5870</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>C_{oss}</td>
<td>Output Capacitance</td>
<td></td>
<td>615</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>C_{rss}</td>
<td>Reverse Transfer Capacitance</td>
<td></td>
<td>135</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Q_{g(to)}</td>
<td>Total Gate Charge at 10 V</td>
<td>V_GS = 0 V to 10 V, V_DD = 75 V, I_D = 33 A, I_G = 1.0 mA</td>
<td>82</td>
<td>107</td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>Q_{g(th)}</td>
<td>Threshold Gate Charge</td>
<td>V_GS = 0 V to 2 V, V_DD = 75 V, I_D = 33 A, I_G = 1.0 mA</td>
<td>11</td>
<td>14</td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>Q_{gs}</td>
<td>Gate to Source Gate Charge</td>
<td>V_DD = 75 V, I_D = 33 A, I_G = 1.0 mA</td>
<td>23</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>Q_{g2}</td>
<td>Gate Charge Threshold to Plateau</td>
<td></td>
<td>13</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>Q_{gd}</td>
<td>Gate to Drain “Miller” Charge</td>
<td></td>
<td>19</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td><strong>RESISTIVE SWITCHING CHARACTERISTICS (V_GS = 10 V)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{ON}</td>
<td>Turn-On Time</td>
<td>V_DD = 75 V, I_D = 33 A, V_GS = 10 V, R_GS = 3.6 Ω</td>
<td>69</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{ON(OFF)}</td>
<td>Turn-On Delay Time</td>
<td></td>
<td>16</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_r</td>
<td>Rise Time</td>
<td></td>
<td>30</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{OFF}</td>
<td>Turn-Off Delay Time</td>
<td></td>
<td>39</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_f</td>
<td>Fall Time</td>
<td></td>
<td>17</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{OFF}</td>
<td>Turn-Off Time</td>
<td></td>
<td>84</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><strong>DRAIN–SOURCE DIODE CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{SD}</td>
<td>Source to Drain Diode Voltage</td>
<td>I_SD = 33 A</td>
<td>1.25</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I_SD = 16 A</td>
<td>1</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>t_r</td>
<td>Reverse Recovery Time</td>
<td>I_SD = 33 A, dI_SD/dt = 100 A/μs</td>
<td>105</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Q_{RRR}</td>
<td>Reverse Recovery Charge</td>
<td>I_SD = 33 A, dI_SD/dt = 100 A/μs</td>
<td>327</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Width = 100 s
TYPICAL CHARACTERISTICS

$T_C = 25^\circ C$ unless otherwise noted

Figure 1. Normalized Power Dissipation vs. Ambient Temperature

Figure 2. Maximum Continuous Drain Current vs Case Temperature

Figure 3. Normalized Maximum Transient Thermal Impedance

Figure 4. Peak Current Capability
TYPICAL CHARACTERISTICS (Continued)

$T_C = 25^\circ C$ unless otherwise noted

**Figure 5. Forward Bias Safe Operating Area**

**Figure 6. Unclamped Inductive Switching Capability**

**Figure 7. Transfer Characteristics**

**Figure 8. Saturation Characteristics**

**Figure 9. Drain to Source On Resistance vs Drain Current**

**Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature**

**NOTE:** Refer to ON Semiconductor Application Notes AN−7515 and AN−7517
TYPICAL CHARACTERISTICS (Continued)

$T_C = 25^\circ C$ unless otherwise noted

Figure 11. Normalized Gate Threshold Voltage vs. Junction Temperature

Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

Figure 13. Capacitance vs. Drain to Source Voltage

Figure 14. Gate Charge Waveforms for Constant Gate Currents
Figure 15. Unclamped Energy Test Circuit

Figure 16. Unclamped Energy Waveforms

Figure 17. Gate Charge Test Circuit

Figure 18. Gate Charge Waveforms

Figure 19. Switching Time Test Circuit

Figure 20. Switching Time Waveforms
Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, $T_{JM}$, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, $P_{DM}$, in an application. Therefore the application’s ambient temperature, $T_A$ ($^\circ$C), and thermal resistance $R_{thJA}$ ($^\circ$C/W) must be reviewed to ensure that $T_{JM}$ is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{thJA}}$$  \hspace{1cm} (eq. 1)

In using surface mount devices such as the TO–263 (D2–PAK–3) package, the environment in which it is applied will have a significant influence on the part’s current and maximum power dissipation ratings. Precise determination of $P_{DM}$ is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

ON Semiconductor provides thermal information to assist the designer’s preliminary application evaluation. Figure 21 defines the $R_{thJA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR–4 board with 1 oz copper after 1 000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the ON Semiconductor device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeter square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{thJA} = 26.51 + \frac{19.84}{(0.262 + \text{Area})}$$  \hspace{1cm} (eq. 2)  

Area in Inches Squared.

$$R_{thJA} = 26.51 + \frac{128}{(1.69 + \text{Area})}$$  \hspace{1cm} (eq. 3)  

Area in Centimeters Squared.

![Figure 21. Thermal Resistance vs. Mounting Pad Area](image-url)
PSPICE Electrical Model

.SUBCKT FDB2532 2 1 3 ; rev April 2002
CA 12 8 1.4e−9
CB 15 14 1.6e−9
CIN 6 8 5.61e−9

Dboby 7 5 DbobyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD
Ebreak 11 7 17 18 159
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1
It 8 17 1

Lgate 1 9 9.56e−9
Ldrain 2 5 1.0e−9
Lsource 3 7 7.71e−9

RLgate 1 9 95.6
RLdrain 2 5 10
RLsource 3 7 77.1

Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 9.6e−3
Rgate 9 20 1.01

RSLC1 5 51 RSLCMOD 1.0e−6
RSLC2 5 50 1.0e3
Rsource 8 7 RsoureMOD 3.0e−3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE=\(\left\{(V(5,51)/\text{ABS}(V(5,51)))\right\}^2(PWR(V(5,51)/(1e-6*190),3))\}

.MODELD bodyMOD D (IS=6.0E−11 N=1.09 RS=2.3e−3 TRS1=3.0e−3 TRS2=1.0e−6
+ CJO=3.9e−9 M=0.65 TT=4.8e−8 XTI=4.2)

.MODELD breakMOD D (RS=0.17 TRS1=3.0e−3 TRS2=−8.9e−6)

.MODELD plcapMOD D (CJO=1.0e−9 IS=1.0e−30 N=10 M=0.6)

.MODELD mmedMOD NMOS (VTO=3.55 KP=10 IS=1e−30 N=10 TOX=1 L=1u W=1u RG=1.01)

.MODELD mstroMOD NMOS (VTO=4.2 KP=145 IS=1e−30 N=10 TOX=1 L=1u W=1u)

.MODELD mweakMOD NMOS (VTO=2.9 KP=0.05 IS=1e−30 N=10 TOX=1 L=1u W=1u RG=10.1 RS=0.1)

.MODELD bbreakMOD RES (TC1=1.1e−3 TC2=−9.0e−7)

.MODELD rdrainMOD RES (TC1=9.0e−3 TC2=3.5e−5)

.MODELD rslcMOD RES (TC1=3.4e−3 TC2=1.5e−6)
.MODEL RsourceMOD RES (TC1=4.0e−3 TC2=1.0e−6)
.MODEL RvthresMOD RES (TC1=−4.1e−3 TC2=−1.4e−5)
.MODEL RvtempMOD RES (TC1=−4.0e−3 TC2=3.5e−6)

.MODEL S1AMOD VSWITCH (RON=1e−5 ROFF=0.1 VON=−6.0 VOFF=−4.0)
.MODEL S1BMOD VSWITCH (RON=1e−5 ROFF=0.1 VON=−4.0 VOFF=−6.0)
.MODEL S2AMOD VSWITCH (RON=1e−5 ROFF=0.1 VON=−1.4 VOFF=1.0)
.MODEL S2BMOD VSWITCH (RON=1e−5 ROFF=0.1 VON=1.0 VOFF=−1.4)


Figure 22. PSPICE Electrical Model
SABER Electrical Model
REV April 2002

template FDB2532 n2,n1,n3
electrical n2,n1,n3
{
    var i iscl
dp..model dbodymod = (isl=6.0e−11,nl=1.09,rs=2.3e−3,trs1=3.0e−3,trs2=1.0e−6,cjo=3.9e−9,m=0.65,tt=4.8e−8,xti=4.2)
dp..model dbreakmod = (rs=0.17,trs1=3.0e−3,trs2=−8.9e−6)
dp..model dplcapmod = (cjo=1.0e−9,isl=10.0e−30,nl=10,m=0.6)
m..model mmedmod = (type=_n,vto=3.55,kp=10,is=1e−30, tox=1)
m..model mstrongmod = (type=_n,vto=4.2,kp=145,is=1e−30, tox=1)
m..model mweakmod = (type=_n,vto=2.9,kp=0.05,is=1e−30, tox=1,rs=0.1)
sw_vcsp..model s1amod = (ron=1e−5,roff=0.1,von=−6.0,voff=−4.0)
sw_vcsp..model s1bmod = (ron=1e−5,roff=0.1,von=−4.0,voff=−6.0)
sw_vcsp..model s2amod = (ron=1e−5,roff=0.1,von=−1.4,voff=1.0)
sw_vcsp..model s2bmod = (ron=1e−5,roff=0.1,von=1.0,voff=−1.4)
c.ca n12 n8 = 1.4e−9
c.cb n15 n14 = 1.6e−9
c.cin n6 n8 = 5.61e−9
dp..dbody n7 n5 = model=dbodymod
dp..dbreak n5 n11 = model=dbreakmod
dp..dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 159
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 9.56e−9
l.ldrain n2 n5 = 1.0e−9
l.isource n3 n7 = 7.71e−9

res.rlgate n1 n9 = 95.6
res.rldrain n2 n5 = 10
res.rsource n8 n7 = 77.1

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbbreak n17 n18 = 1, tc1=1.1e−3,tc2=−9.0e−7
res.rdren n50 n16 = 9.6e−3, tc1=9.0e−3,tc2=3.5e−5
res.rgate n9 n20 = 1.01
res.rslc1 n5 n51 = 1.0e−6, tc1=3.4e−3,tc2=1.5e−6
res.rslc2 n5 n50 = 1.0e3
res.rsource n8 n7 = 3.0e−3, tc1=4.0e−3,tc2=1.0e−6
res.rvthres n22 n8 = 1, tc1=−4.1e−3,tc2=−1.4e−5
res.rvtemp n18 n19 = 1, tc1=−4.0e−3,tc2=3.5e−6
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod
v.vbat n22 n19 = dc=1

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e−9+abs(v(n5,n51))))*(abs(v(n5,n51)*1e6/190))** 3))
}

Figure 23. SABER Electrical Model
SPICE Thermal Model
REV 26 February 2002

FDB2532

CTHERM1 TH 6 7.5e−3
CTHERM2 6 5 8.0e−3
CTHERM3 5 4 9.0e−3
CTHERM4 4 3 2.4e−2
CTHERM5 3 2 3.4e−2
CTHERM6 2 TL 6.5e−2

RThERM1 TH 6 3.1e−4
RThERM2 6 5 2.5e−3
RThERM3 5 4 2.0e−2
RThERM4 4 3 8.0e−2
RThERM5 3 2 1.2e−1
RThERM6 2 TL 1.3e−1

SABER Thermal Model
SABER thermal model FDB2532
template thermal_model th tl
thermal_c th, tl
{
  ctherm.ctherm1 th 6 =7.5e−3
ctherm.ctherm2 6 5 =8.0e−3
ctherm.ctherm3 5 4 =9.0e−3
ctherm.ctherm4 4 3 =2.4e−2
ctherm.ctherm5 3 2 =3.4e−2
ctherm.ctherm6 2 tl =6.5e−2
  rtherm.rtherm1 th 6 =3.1e−4
  rtherm.rtherm2 6 5 =2.5e−3
  rtherm.rtherm3 5 4 =2.0e−2
  rtherm.rtherm4 4 3 =8.0e−2
  rtherm.rtherm5 3 2 =1.2e−1
  rtherm.rtherm6 2 tl =1.3e−1
}

Figure 24. Thermal Model

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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

D2PAK–3 (TO–263, 3–LEAD)
CASE 418AJ
ISSUE E

NOTES:
1. DIMENSIONING AND TOLERANCING PER
2. CONTROLLING DIMENSION INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH.
   MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE.
   THESE DIMENSIONS ARE MEASURED AT THE OUTMOST
   EXTREMITIES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN
   DIMENSIONS E, L1, DI, AND EI.
6. OPTIONAL MOLD FEATURE.
7. O, O, 3, OPTICAL CONSTRUCTION FEATURE CALL OUTS.

RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please consult
the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERING/MT.

IC Standard Rectifier SSG

XXXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb–Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking.
Pb–Free indicator, "G" or microdot "x", may or may not be present. Some products
may not follow the Generic Marking.

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