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## High Voltage Inverting Buck Reduces Complexity and Board Space

### APPLICATION NOTE

#### INTRODUCTION

Applications in the electronics industry ranging from sensor-based designs to power amplifiers are periodically faced with the requirement to generate a negative voltage rail. Although many transformer-based designs, charge pumps and other methods have been used to meet such a requirement, the inverting buck-boost topology stands out as simple to design and can save on power and board space too.

With power budgets in many applications already stretched, and PCB real estate limited due to the high levels of functionality incorporated in many new products, power devices that use an inverting buck-boost topology can prove extremely valuable to systems designers.

A Buck regulator can be reconfigured to generate a negative output voltage from a positive input voltage using the inverting buck-boost topology. Unlike a buck regulator, the Inverting buck-boost transfers energy to the output through the output diode during the 'Off' time. For this reason, users must keep in mind that the average output current is always less than the average inductor current.

In addition, the designer must be mindful that the device is no longer referenced to Gnd but to the negative output voltage, which makes the effective input voltage across the device  $V_{IN} + |V_{OUT}|$ .

Telecom vendors tend to adopt a two-stage design to generate a negative voltage rail for the GaN PA driver. The first stage steps down the input voltage (48–65 V typically) to 12 V, followed by a second stage that generates –6.5 V. Using a device such as ON Semiconductor's NCP4060, designers can consolidate this into one stage that takes the high input voltage and converts it down to a negative output voltage while sustaining good efficiency and offering a solution for space-constrained applications.

There are a number of important factors and challenges to consider when adopting buck-boost topologies. ON Semiconductor's NCP4060 is an 80 V synchronous buck regulator with integrated power FETs that can accommodate up to 6 A DC loads. It is an example of a device that provides the flexibility to down convert from high input voltages to negative output voltages just by exchanging  $V_{out}$  with Gnd on a buck.

Table 1. POSITIVE INPUT TO NEGATIVE OUTPUT VOLTAGE CONVERSION USING THE NCP4060

Device	Application	$V_{IN}$	$V_{OUT}$	Topology	I/O Isolation
NCP4060	Power Supplies	Positive	Negative	Buck	N/A

#### Application Specs:

Table 2. APPLICATION SPECS.

$V_{IN}$	65 V
$V_{OUT}$	–6.5 V
$I_{OUT}$	5 A
$f_{SW}$	300 Khz
Efficiency %	Up to 85%

# AND9785/D

## Application Schematic:

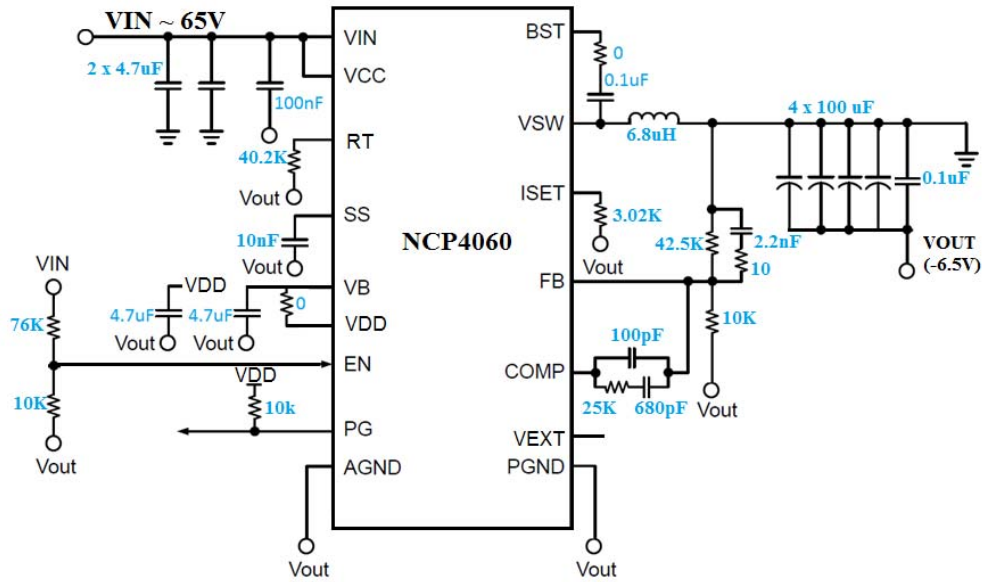


Figure 1. Implementing the NCP4060 in Buck-Boost Configuration

The inverting buck-boost topology is implemented with the NCP4060 with minor modifications to the buck circuit. The inductor is connected to GND and the NCP4060 is referenced to Vout. This reconfiguration in the design allows the output voltage to be inverted and always-below GND. During the 'ON'-Time the control switch is closed, the inductor sees the input voltage across it and current flows to charge it while the output capacitor supplies the load current. During the 'OFF'-Time, the control switch goes open circuit and the inductor discharges to the load and the output capacitor via the Sync switch. The figures below show the voltage and current signals during the 'ON' and 'OFF' times.

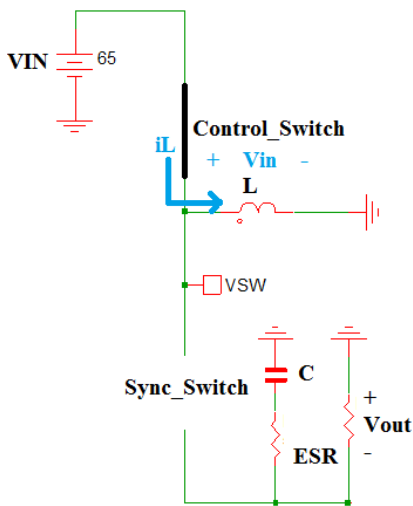


Figure 2. ON-Time

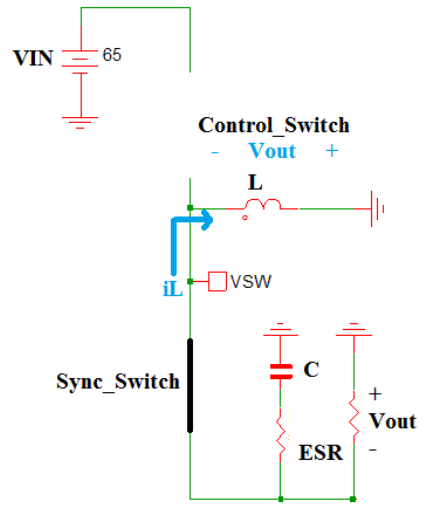


Figure 3. OFF-Time

During the 'ON' time with a fixed DC voltage across the inductor, current ramps up linearly at a rate of

$$\frac{di}{dt} = \frac{V_{in}}{L} \quad (\text{eq. 1})$$

During the 'OFF'-time the flux is continuous, the inductor current cannot change instantaneously hence the voltage across it reverses polarity to keep the current flowing continuously at a rate of

$$\frac{di}{dt} = \frac{-V_{out}}{L} \quad (\text{eq. 2})$$

The average inductor current in a buck-boost circuit is

$$I_L = \frac{I_{out}}{1 - D} \quad (\text{eq. 3})$$

and the peak to peak inductor current is

$$I_{Lpp} = \frac{V_{in} \cdot D}{f_{sw} \cdot L} \quad (\text{eq. 4})$$

and the duty cycle is approximately

$$D = \frac{V_{out}}{V_{out} + V_{in}} \quad (\text{eq. 5})$$

### Output Voltage Setting

An external resistive divider between GND and the Vout reference sets the output voltage. The resistor values can be calculated by using the following equations:

$$R_{Top} = R_{Bottom} \cdot \left( \frac{V_{out} - 1.25}{1.25} \right) \quad (\text{eq. 6})$$

where 1.25 is the internal reference voltage.

### Vin and Vout Range

The maximum input voltage that can be applied to a buck-boost converter IC is lower than what the maximum input voltage can be when the NCP4060 is configured in a buck type application. It is important that the designer is aware that the input voltage across the IC is Vin - VOut that is equal to Vin + |VOut|. In this case 65 + 6.5 ~ 71.5 V.

The output voltage in the inverting buck-boost is inverted with GND as the positive rail and Vout the negative rail.

### Inductor Selection

Sizing the inductor is determined by the switching frequency, ripple current and input voltage. Small inductor values lead to fast transient response and large ripple currents (E = 1/2 IL2pk). Large inductor values lead to small ripple currents and slow transient response. As a rule of thumb, the peak-to-peak ripple current is set to 40% of the maximum average inductor current. The inductor current can be calculated using the following equation:

$$L = \frac{V_{in} \cdot D}{0.4 \cdot I_{avg} \cdot f_{sw}} \quad (\text{eq. 7})$$

where Iavg is Iout / 1-D.

### Input Capacitor Selection

The input capacitors in a buck-boost configuration experience discontinuous currents since the control switch is connected to the input voltage. Fast di/dt from zero to IL and back to zero in CCM requires adequate filtering to attenuate high frequency noise on the input rail. Low ESR MLCCs are recommended along with good component placement around the IC in order to minimize the effect of parasitic inductance. The following equation provides a minimum value for the input capacitor to sustain the input voltage within the tolerance window of 5%.

$$C_{in} = \frac{I_{outmax} \cdot D}{f_{sw} \cdot (0.05 \cdot V_{inmin} - I_{pk} \cdot C_{inESR})} \quad (\text{eq. 8})$$

The Rms Current through the input capacitor is calculated by using the following equation:

$$I_{rmsCin} = \sqrt{D \cdot \left( \frac{1 - D + \Delta I_L^2}{12} \right) \cdot \frac{I_{outmax}}{1 - D}} \quad (\text{eq. 9})$$

An additional bypass capacitor between Vin and Vout is recommended for stability and it could help in lowering the output voltage ripple. There are significant differences that come into play when designing an inverting buck-boost when transitioning from DCM to CCM during which the feedback loop contains a RHPZ.

### Output Capacitor Selection

The output voltage in a buck-boost circuit is noisy due to the switching phenomenon during the 'OFF' time period. The discontinuity in output current forces a larger output capacitor than what it could have been in a buck regulator.

The equation below estimates the minimum capacitance required to sustain the output voltage within the tolerance window:

$$C_{out} = \frac{I_{outmax} \cdot D}{f_{sw} \cdot (\Delta I_L - I_{pk} \cdot C_{outESR})} \quad (\text{eq. 10})$$

The rms current rating of the selected capacitor should be higher than the calculated value below:

$$I_{rmsCout} = I_{outmax} \cdot \sqrt{\frac{D + \frac{\Delta I_L^2}{12}}{1 - D}} \quad (\text{eq. 11})$$

### Typical Waveforms and Simulation Results

In order to demonstrate some of the topics discussed in this paper, a test circuit was constructed and some signals were captured on an oscilloscope to reinforce the aforementioned content. The output voltage and switch node signals are show in figure 3. It is obvious that the switch node voltage varies between Vin and VOut as described in previous sections in the article. The output voltage regulates at -6.5 V and the peak-to-peak ripple voltage measured around 50 mV.

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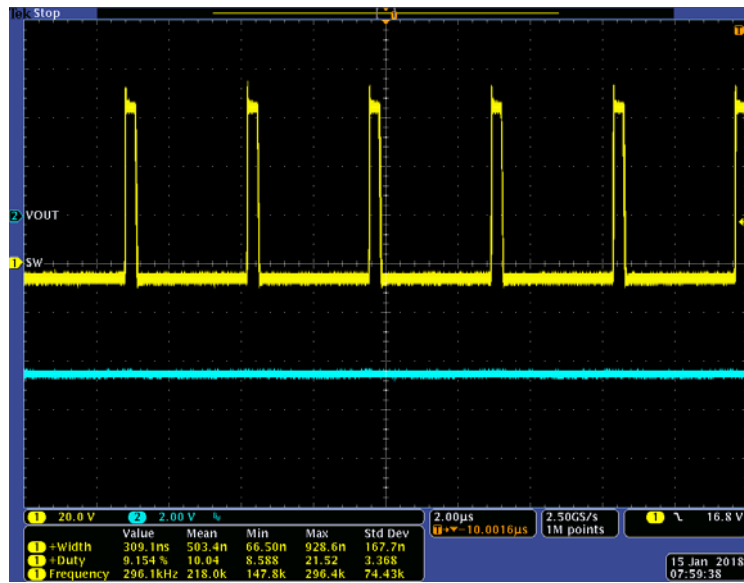


Figure 4.

In addition, a Simplis model was designed for the circuit to show the frequency response at light loads as shown in

figure 5. The Cross-over frequency is around 13 KHz with a 45 degree phase margin along with -18 dB gain margin.

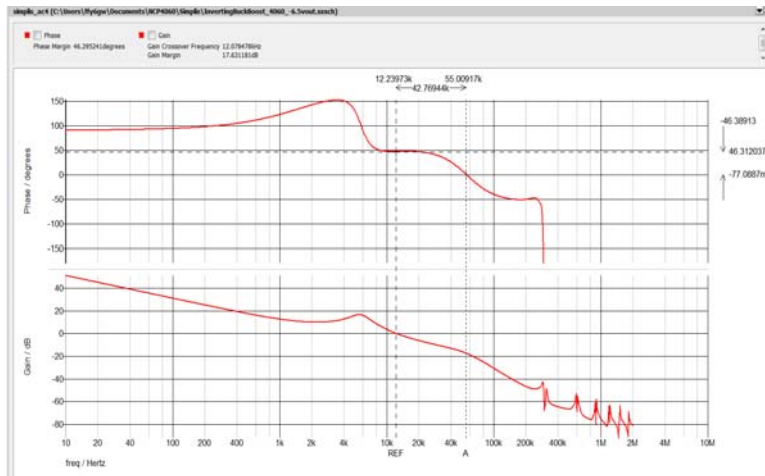


Figure 5.

### Conclusion:

A buck IC can be reconfigured to an inverting buck-boost circuit to generate a negative output voltage from a positive input voltage. The implementation steps are straight forward

however a few design tips were explained to stress the fundamental differences between a Buck regulator and the Inverting Buck-Boost.

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