

NS3L500

3.3V, 8-Channel, 2:1 Gigabit Ethernet LAN Switch with LED Switch

The NS3L500 is a 8-channel 2:1 LAN switch with 3 additional built-in SPDT switches for LED routing. This switch is ideal for Gigabit LAN applications due to its low ON-state resistance and capacitance giving the switch a typical bandwidth of 800 MHz. The switch also has excellent ON-state resistance match, low bit-to-bit skew, and low crosstalk among channels. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs.

This part can be used to replace mechanical relays in low-voltage LAN applications that interface a physical layer over CAT 5 or CAT 6 unshielded twisted pair cable through an isolation transformer. The NS3L500 is available in a 56-pin WQFN package and operates over the extended -40°C to $+85^{\circ}\text{C}$ temperature range.

Features

- V_{CC} Operating Range: +3.0 V to +3.6 V
- Low ON-State Resistance ($R_{ON} = 4 \Omega$ Typical)
- Low ON-State Capacitance ($C_{ON} = 7 \text{ pF}$ Typical)
- Flat ON-State Resistance ($R_{ON}(\text{flat}) = 0.5 \Omega$ Typical)
- Wide Bandwidth (800 MHz Typical)
- Low Crosstalk ($X_{TALK} = -37 \text{ dB}$ Typical)
- Near-Zero Propagation Delay: 250 ps
- Low Bit-to-Bit Skew ($t_{sk(o)} = 100 \text{ ps Max}$)
- Three SPDT Channels for LED Signal Switching
- Packaging: 56-Pin WQFN
- Pin-to-Pin Compatible with PI3L500-A, TS3L500AE and MAX4927
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

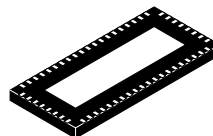
- 10/100/1000 Base-T Ethernet Signal Switching
- Notebooks and Docking Stations
- Hub and Router Signal Switching
- Differential (LVDS, LVPECL) Signal Switching



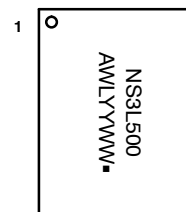
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MARKING DIAGRAMS



WQFN56
MT SUFFIX
CASE 510AK

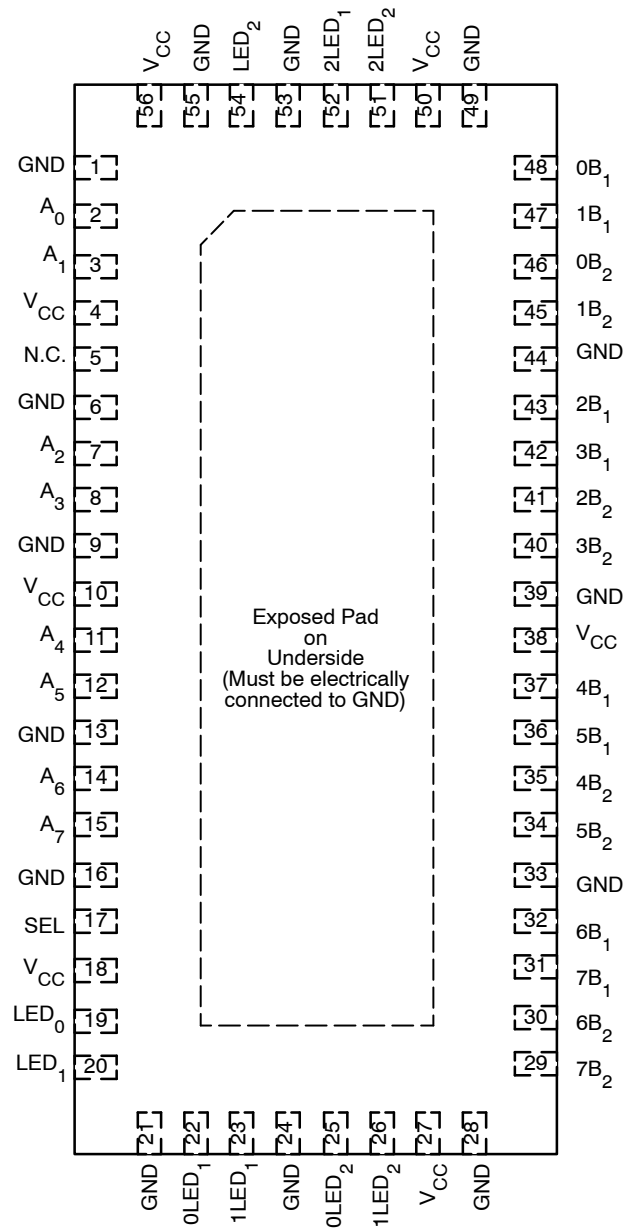


- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

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**Figure 1. Pinout
(Top View)**

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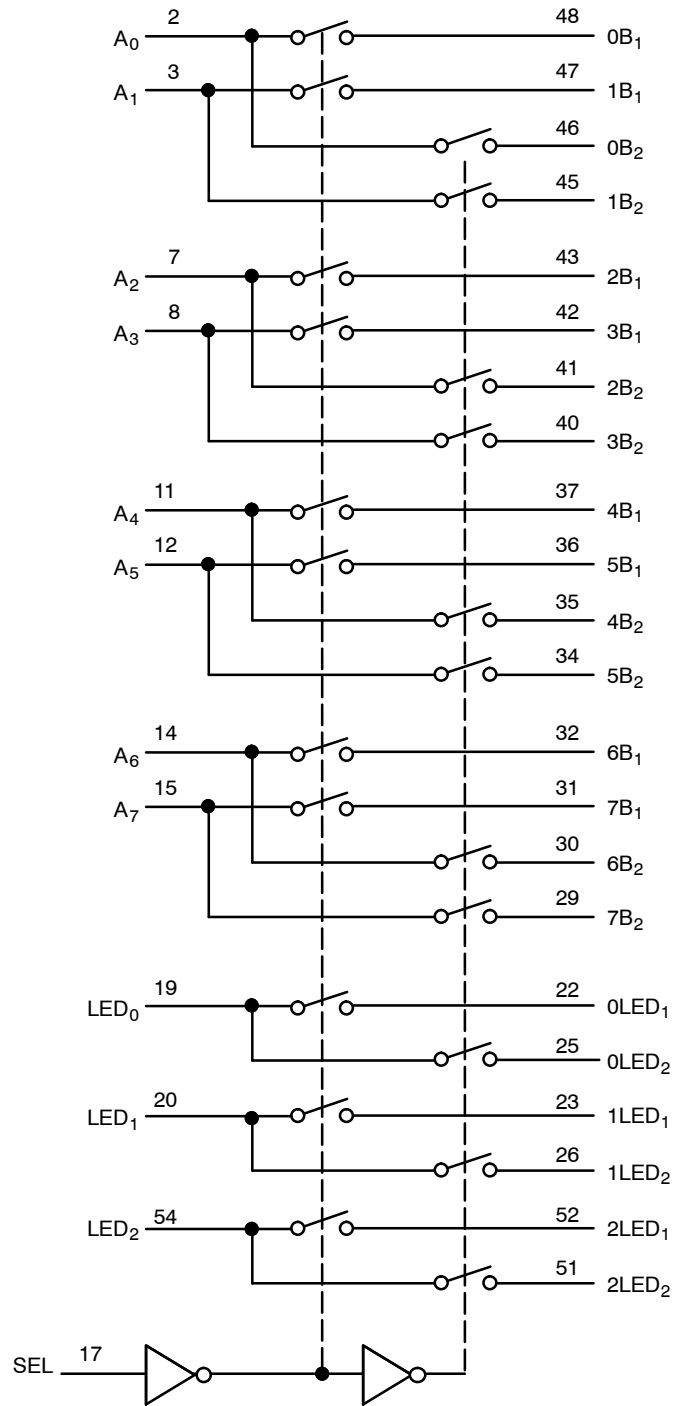


Figure 2. Block Diagram

PIN DESCRIPTION

Pin Name	Description
A _x	Data I/Os
xB _y	Data I/Os
SEL	Select Input
LED _x	LED I/O Port
xLED _y	LED I/O Port

TRUTH TABLE

SEL	Function
L	A _x to xB ₁ : LED _x to xLED ₁
H	A _x to xB ₂ : LED _x to xLED ₂

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MAXIMUM RATINGS

Symbol	Pins	Parameter	Value	Unit
V _{CC}	V _{CC}	Positive DC Supply Voltage	-0.5 to +5.5	V
V _{IN}	SEL	Control Input Voltage	-0.5 to +5.5	V
V _{I/O}	A _X , xB _Y , LED _X , xLED _Y	Switch I/O Voltage Range	-0.5 to V _{CC} +0.5	V
I _{CC}	V _{CC}	DC Output Current	± 120	mA
I _{IK}	SEL	Control Input Clamp Current	-50	mA
I _{I/O}	A _X , xB _Y , LED _X , xLED _Y	ON-State Switch Current	± 120	mA
R _{θJA}		Thermal Resistance, Junction-to-Air	125	°C/W
T _S		Storage Temperature	-65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Pins	Parameter	Value	Unit
V _{CC}	V _{CC}	Positive DC Supply Voltage	+3.0 to +3.6	V
V _{IN}	SEL	Control Input Voltage	0 to +5.5	V
V _{I/O}	A _X , xB _Y , LED _X , xLED _Y	Switch I/O Voltage Range	0 to V _{CC}	V
T _A		Operating Temperature	-40 to +85	°C

Minimum and maximum values are guaranteed through test or design across the Recommended Operating Conditions, where applicable. Typical values are listed for guidance only and are based on the particular conditions listed for section, where applicable. These conditions are valid for all values found in the characteristics tables unless otherwise specified in the test conditions.

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DC ELECTRICAL CHARACTERISTICS (Typical: T = 25°C, V_{CC} = 3.3 V)

Symbol	Pins	Parameters	Conditions	-40°C to +85°C			Unit
				Min	Typ	Max	
1000 BASE-T ETHERNET SWITCHING							
V _{IH}	SEL	Control Input HIGH Voltage		2		5.5	V
V _{IL}	SEL	Control Input LOW Voltage		-0.5		0.8	V
V _{IK}	SEL	Clamp Diode Voltage	V _{CC} = Max, I _{IN} = -18 mA		-0.7	-1.2	V
I _{IH}	SEL	Input HIGH Current	V _{CC} = Max, V _{IN} = V _{CC}	-1		+1	μA
I _{IL}	SEL	Input LOW Current	V _{CC} = Max, V _{IN} = GND	-1		+1	μA
I _{OFF}	SEL	Off-Leakage Current	V _{CC} = 0 V, V _{IN} = 0 V to 3.6 V			±1.5	μA
I _{CC}	V _{CC}	Quiescent Supply Current	V _{CC} = 3.6 V, V _{IN} = V _{CC} or GND, I _O = 0 mA		250	600	μA
I _{LA(OFF)}	A _X , xB _Y	Off-Leakage Current	V _{CC} = 3.6 V, V _{A_X} = 0.3 V, 3.3 V; V _{x_B1} or V _{x_B2} = 3.3 V, 0.3 V	-1		+1	μA
I _{LA(ON)}	A _X , xB _Y	On-Leakage Current	V _{CC} = 3.6 V, V _{A_X} = 0.3 V, 3.3 V; V _{x_B1} or V _{x_B2} = 0.3 V, 3.3 V, or floating	-1		+1	μA
R _{ON}	A _X , xB _Y	On-Resistance	V _{CC} = 3 V, 1.5 V ≤ V _{IN} ≤ V _{CC} , I _O = -40 mA		4	7	Ω
R _{ON(FLAT)}	A _X , xB _Y	On-Resistance Flatness	V _{CC} = 3 V, V _{IN} = 1.5 V and V _{CC} , I _O = -40 mA		0.5		Ω
ΔR _{ON}	A _X , xB _Y	On-Resistance Match Between Switch Pairs	V _{CC} = 3 V, 1.5 V ≤ V _{IN} ≤ V _{CC} , I _O = -40 mA		0.4	1	Ω

10/100 BASE-T ETHERNET SWITCHING

V _{IH}	SEL	Control Input HIGH Voltage		2		5.5	V
V _{IL}	SEL	Control Input LOW Voltage		-0.5		0.8	V
V _{IK}	SEL	Clamp Diode Voltage	V _{CC} = Max, I _{IN} = -18 mA		-0.7	-1.2	V
I _{IH}	SEL	Input HIGH Current	V _{CC} = Max, V _{IN} = V _{CC}	-1		+1	μA
I _{IL}	SEL	Input LOW Current	V _{CC} = Max, V _{IN} = GND	-1		+1	μA
I _{OFF}	SEL	Off-Leakage Current	V _{CC} = 0 V, V _{IN} = 0 V to 3.6 V			±1.5	μA
I _{CC}	V _{CC}	Quiescent Supply Current	V _{CC} = 3.6 V, V _{IN} = V _{CC} or GND, I _O = 0 mA		250	600	μA
I _{LA(OFF)}	A _X , xB _Y	Off-Leakage Current	V _{CC} = 3.6 V, V _{A_X} = 0.3 V, 3.3 V; V _{x_B1} or V _{x_B2} = 3.3 V, 0.3 V	-1		+1	μA
I _{LA(ON)}	A _X , xB _Y	On-Leakage Current	V _{CC} = 3.6 V, V _{A_X} = 0.3 V, 3.3 V; V _{x_B1} or V _{x_B2} = 0.3 V, 3.3 V, or floating	-1		+1	μA
R _{ON}	A _X , xB _Y	On-Resistance	V _{CC} = 3 V, 1.25 V ≤ V _{IN} ≤ V _{CC} , I _O = -10 mA to -30 mA		4	6	Ω
R _{ON(FLAT)}	A _X , xB _Y	On-Resistance Flatness	V _{CC} = 3 V, V _{IN} = 1.25 V and V _{CC} , I _O = -10 mA to -30 mA		0.5		Ω
ΔR _{ON}	A _X , xB _Y	On-Resistance Match Between Switch Pairs	V _{CC} = 3 V, 1.25 V ≤ V _{IN} ≤ V _{CC} , I _O = -10 mA to -30 mA		0.4	1	Ω

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DC ELECTRICAL CHARACTERISTICS (Typical: T = 25°C, V_{CC} = 3.3 V)

Symbol	Pins	Parameters	Conditions	-40°C to +85°C			Unit
				Min	Typ	Max	
LED SWITCHING							
R _{ON}	LED _X , xLED _Y	On-Resistance	V _{CC} = 3 V, 1.25 V ≤ V _{IN} ≤ V _{CC} , I _O = -40 mA		15	25	Ω
R _{ON(FLAT)}	LED _X , xLED _Y	On-Resistance Flatness	V _{CC} = 3 V, V _{IN} = 1.25 V and V _{CC} , I _O = -40 mA		8		Ω
ΔR _{ON}	LED _X , xLED _Y	On-Resistance Match Between Switch Pairs	V _{CC} = 3 V, 1.25 V ≤ V _{IN} ≤ V _{CC} , I _O = -40 mA		1	2	Ω

AC ELECTRICAL CHARACTERISTICS (Typicals: T = 25°C, V_{CC} = 3.3 V)*

Symbol	Pins	Parameters	Conditions	-40°C to +85°C			Unit
				Min	Typ	Max	
SWITCHING CHARACTERISTICS							
t _{PLH} , t _{PHL}	A _X , xB _Y	Propagation Delay	V _{CC} = 3.0 V to 3.6 V (Figure 3)		0.25		ns
t _{ON}	SEL, xLED _Y	Line Enable Time – SEL to xLED _Y	Output: Closed to Open V _{CC} = 3.0 V to 3.6 V (Figure 4)	0.5		15	ns
	SEL, xB _Y	Lines Enable Time – SEL to xB _Y		0.5		3	μs
t _{OFF}	SEL, xLED _Y	Line Enable Time – SEL to xLED _Y	Output: Open to Closed V _{CC} = 3.0 V to 3.6 V (Figure 4)	0.5		9	ns
	SEL, xB _Y	Lines Enable Time – SEL to xB _Y		0.5		35	ns
t _{SK(O)}	A _X , xB _Y	Output Skew between center port to any other port	V _{CC} = 3.0 V to 3.6 V (Calculated, Figure 3)		50	100	ps
t _{SK(P)}	A _X , xB _Y	Skew between opposite transition of the same output (t _{PHL} – t _{PLH})	V _{CC} = 3.0 V to 3.6 V (Calculated, Figure 3)		50	100	ps

DYNAMIC ELECTRICAL CHARACTERISTICS

BW	xB _Y , xLED _Y	-3 dB Bandwidth	R _L = 100 Ω (Figure 5)		800		MHz
O _{IRR}	A _X , LED _X	Off – Isolation	R _L = 100 Ω, f = 250 MHz (Figure 6)		-37		dB
X _{TALK}	A _X to xB _Y A _(X+2) to (X+2)B _Y	Crosstalk	R _L = 100 Ω, f = 250 MHz (Figure 7)		-37		dB

CAPACITANCE

C _{IN}	SEL	Control Pin Input Capacitance	V _{IN} = 0 V, f = 1 MHz		2	3	pF
C _{ON}	A _X , xB _Y	ON Capacitance	V _{IN} = 0 V, f = 1 MHz, Outputs Open, Switch ON		7	10	pF
C _{OFF}	xB _Y	B Port Switch Capacitance	V _{IN} = 0 V, f = 1 MHz, Outputs Open, Switch OFF		5	6	pF

*Guaranteed by design and/or characterization.

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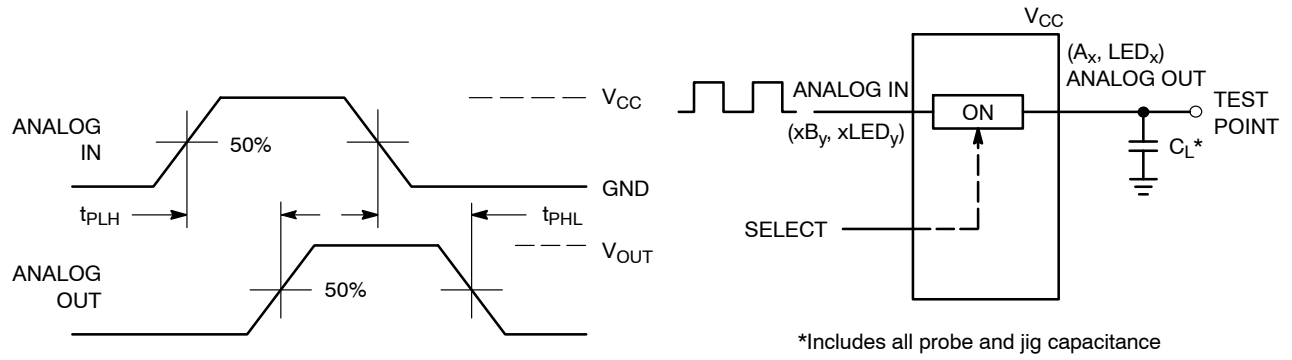


Figure 3. Propagation Delay

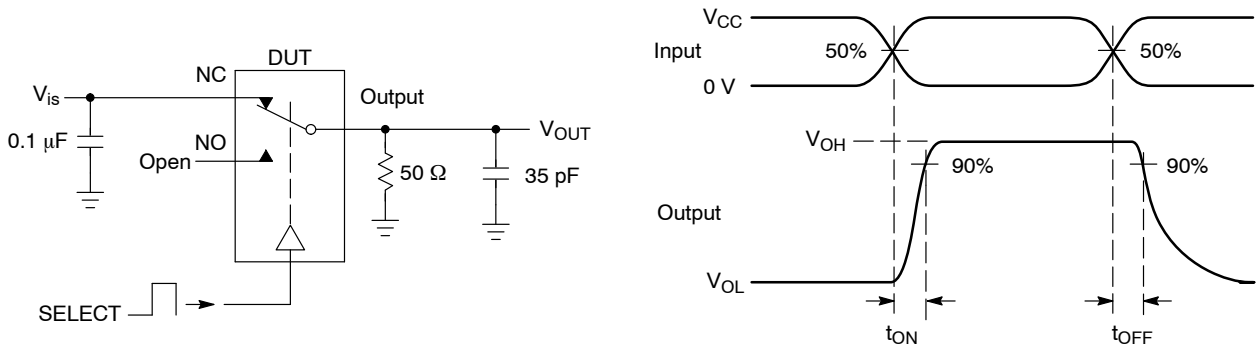


Figure 4. t_{ON}/t_{OFF}

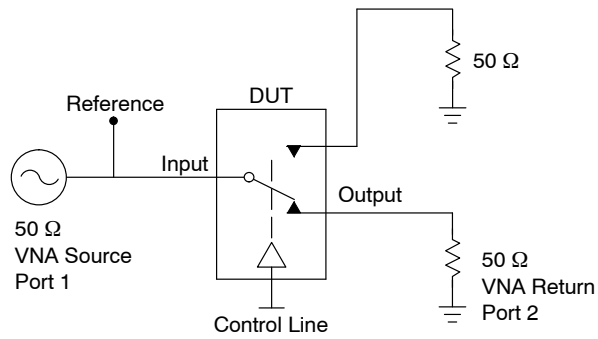


Figure 5. Bandwidth

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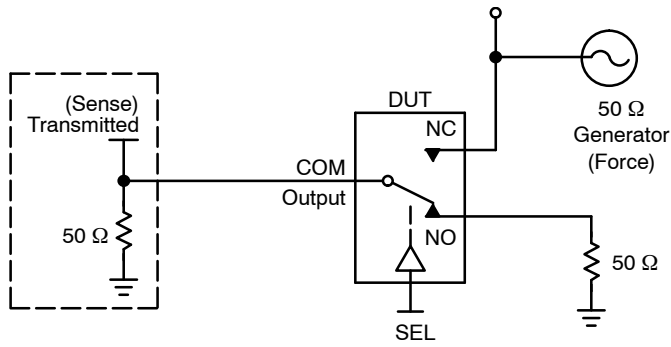
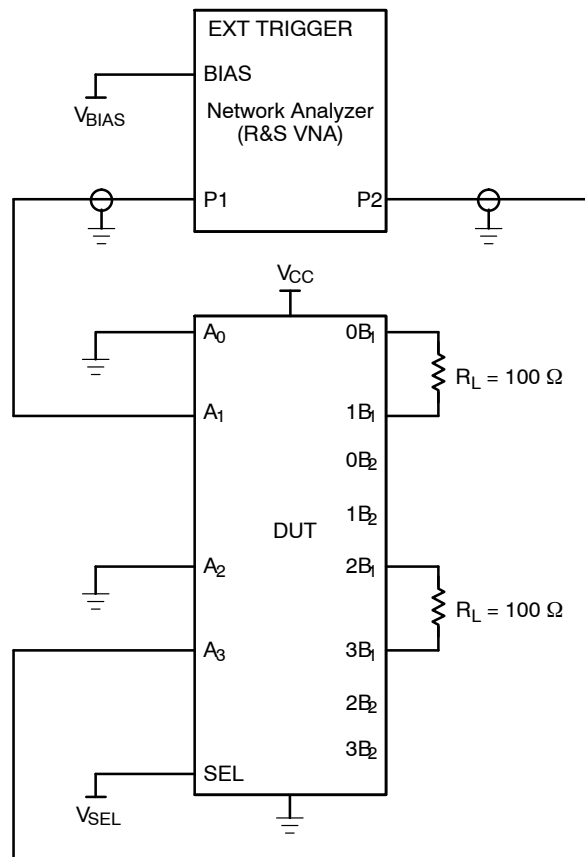


Figure 6. Off-Isolation



1. C_L includes probe and jig capacitance.
2. A $50\ \Omega$ termination resistor is needed to match the loading of the network analyzer.

Figure 7. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when $V_{SEL} = 0$ and A_0 is the input, the output is measured at $1B_1$. All unused analog input (A) ports are connected to GND, and output (B) ports are connected to GND through $50\ \Omega$ pull-down resistors.

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APPLICATION INFORMATION

Logic Inputs

The logic control inputs can be driven up to +3.6 V regardless of the supply voltage. For example, given a +3.3 V supply, the output enables or select pins may be driven low to 0 V and high to 3.6 V. Driving IN Rail-to-Rail® minimizes power consumption.

Power-Supply Sequencing

Proper power-supply sequencing is advised for all CMOS devices. It is recommended to always apply V_{CC} before applying signals to the input/output or control pins.

ORDERING INFORMATION

Device	Package	Shipping†
NS3L500MTTWG	WQFN56 (Pb-free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

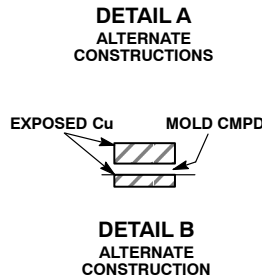
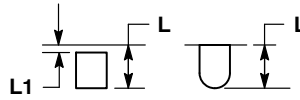
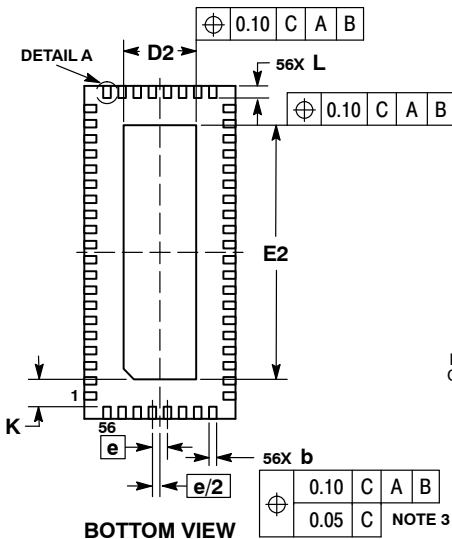
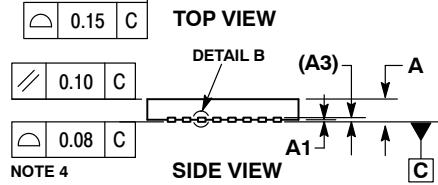
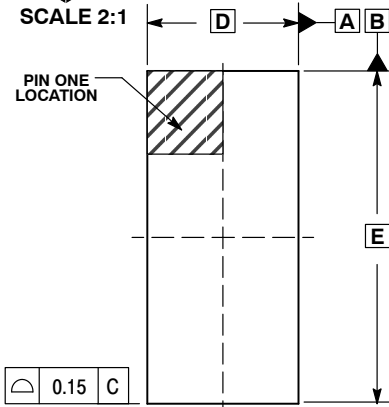
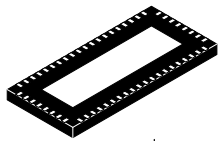
PACKAGE DIMENSIONS

ON Semiconductor®

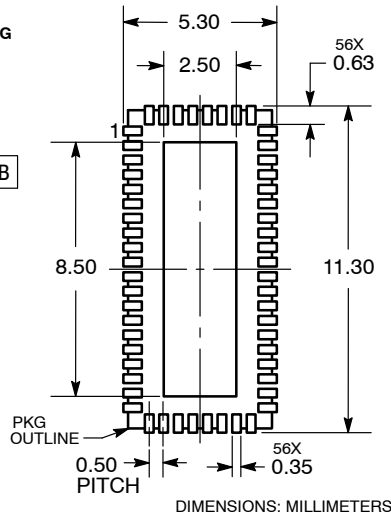


WQFN56 5x11, 0.5P
CASE 510AK-01
ISSUE A

DATE 02 MAR 2010



RECOMMENDED SOLDERING FOOTPRINT

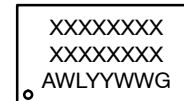


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.70	0.80
A1	---	0.05
A3	0.20	REF
b	0.20	0.30
D	5.00	BSC
D2	2.30	2.50
E	11.00	BSC
E2	8.30	8.50
e	0.50	BSC
K	0.20	MIN
L	0.30	0.50
L1	---	0.15

GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

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