

# 3.3 V Zero Delay Clock Buffer

## NB2309A

The NB2309A is a versatile, 3.3 V zero delay buffer designed to distribute high-speed clocks. It accepts one reference input and drives out nine low-skew clocks. It is available in a 16 pin package.

The -1H version of the NB2309A operates at up to 133 MHz, and has higher drive than the -1 devices. All parts have on-chip PLL's that lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad.

The NB2309A has two banks of four outputs each, which can be controlled by the Select inputs as shown in the Select Input Decoding Table. If all the output clocks are not required, Bank B can be three-stated. The select inputs also allow the input clock to be directly applied to the outputs for chip and system testing purposes.

Multiple NB2309A devices can accept the same input clock and distribute it. In this case the skew between the outputs of the two devices is guaranteed to be less than 700 ps.

All outputs have less than 200 ps of cycle-to-cycle jitter. The input and output propagation delay is guaranteed to be less than 350 ps, and the output to output skew is guaranteed to be less than 250 ps.

The NB2309A is available in two different configurations, as shown in the ordering information table. The NB2309A1 is the base part. The NB2309A11H is the high drive version of the -1 and its rise and fall times are much faster than -1 part.

### Features

- 15 MHz to 133 MHz Operating Range, Compatible with CPU and PCI Bus Frequencies
- Zero Input - Output Propagation Delay
- Multiple Low-Skew Outputs
- Output-Output Skew Less than 250 ps
- Device-Device Skew Less than 700 ps
- One Input Drives 9 Outputs, Grouped as 4 + 4 + 1
- Less than 200 ps Cycle-to-Cycle Jitter is Compatible with Pentium® Based Systems
- Test Mode to Bypass PLL
- Accepts Spread Spectrum Clock at the Input
- Available in 16 Pin, 150 mil SOIC and 4.4 mm TSSOP
- 3.3 V Operation, Advanced 0.35 μ CMOS Technology
- Guaranteed Across Commercial and Industrial Temperature Ranges
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



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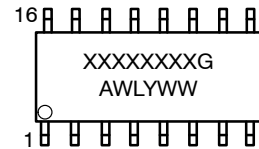
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### MARKING DIAGRAMS\*



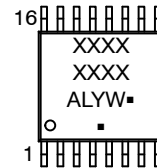
1

**SOIC-16  
D SUFFIX  
CASE 751B**



1

**TSSOP-16  
DT SUFFIX  
CASE 948F**



- XXXX = Device Code
  - A = Assembly Location
  - WL, L = Wafer Lot
  - Y = Year
  - W, WW = Work Week
  - G or ■ = Pb-Free Package
- (Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 7 of this data sheet.

# NB2309A

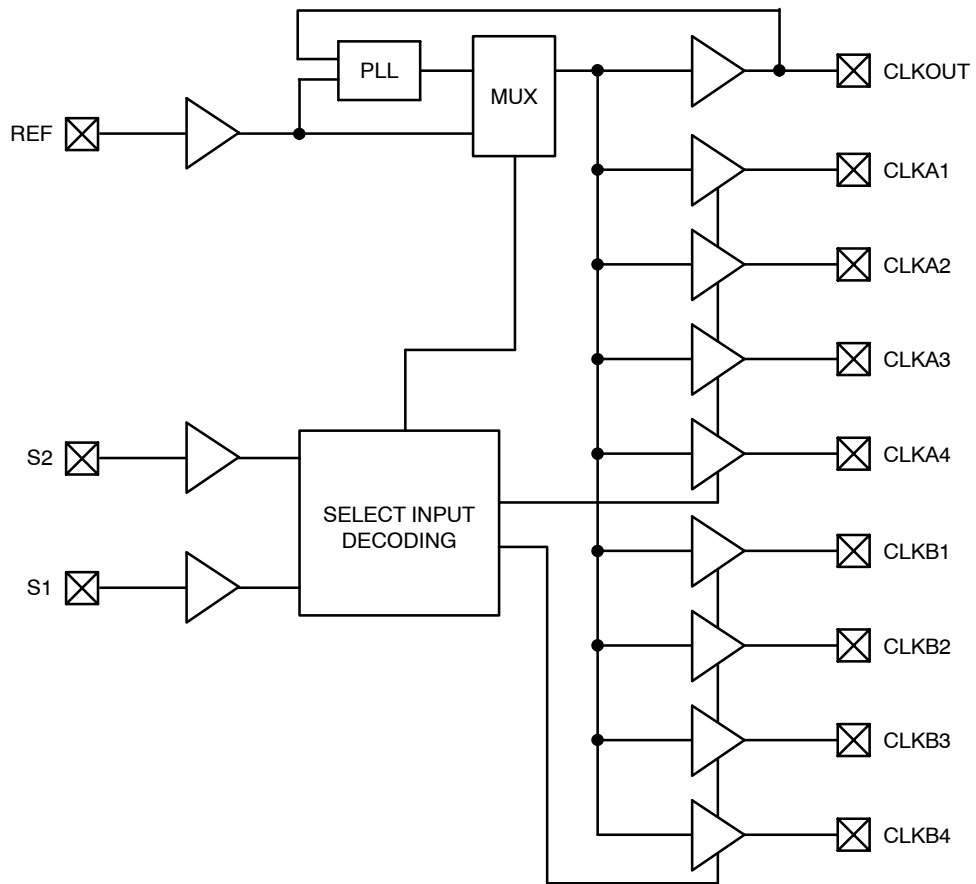


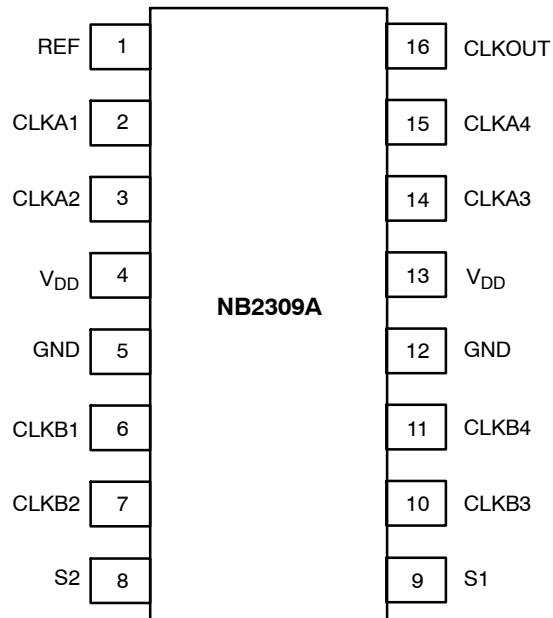
Figure 1. Block Diagram

Table 1. SELECT INPUT DECODING

S2	S1	Clock A1 - A4	Clock B1 - B4	CLKOUT (Note 1)	Output Source	PLL ShutDown
0	0	Three-state	Three-state	Driven	PLL	N
0	1	Driven	Three-state	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

1. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and the output.

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**Figure 2. Pin Configuration**

**Table 2. PIN DESCRIPTION**

Pin #	Pin Name	Description
1	REF (Note 2)	Input reference frequency, 5 V tolerant input.
2	CLKA1 (Note 3)	Buffered clock output, Bank A.
3	CLKA2 (Note 3)	Buffered clock output, Bank A.
4	V <sub>DD</sub>	3.3 V supply.
5	GND	Ground.
6	CLKB1 (Note 3)	Buffered clock output, Bank B.
7	CLKB2 (Note 3)	Buffered clock output, Bank B.
8	S2 (Note 4)	Select input, bit 2.
9	S1 (Note 4)	Select input, bit 1.
10	CLKB3 (Note 3)	Buffered clock output, Bank B.
11	CLKB4 (Note 3)	Buffered clock output, Bank B.
12	GND	Ground.
13	V <sub>DD</sub>	3.3 V supply.
14	CLKA3 (Note 3)	Buffered clock output, Bank A.
15	CLKA4 (Note 3)	Buffered clock output, Bank A.
16	CLKOUT (Note 3)	Buffered output, internal feedback on this pin.

2. Weak pulldown.
3. Weak pulldown on all outputs.
4. Weak pullup on these inputs.

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**Table 3. MAXIMUM RATINGS**

Parameter	Min	Max	Unit
Supply Voltage to Ground Potential	-0.5	+7.0	V
DC Input Voltage (Except REF)	-0.5	$V_{DD} + 0.5$	V
DC Input Voltage (REF)	-0.5	7	V
Storage Temperature	-65	+150	°C
Maximum Soldering Temperature (10 sec)		260	°C
Junction Temperature		150	°C
Static Discharge Voltage (per MIL-STD-883, Method 3015)		>2000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 4. RECOMMENDED OPERATING CONDITIONS**

Parameter	Description	Min	Max	Unit
$V_{DD}$	Supply Voltage	3.0	3.6	V
$T_A$	Operating Temperature (Ambient Temperature)	-40 0	85 70	°C
$C_L$	Load Capacitance, below 100 MHz		30	pF
$C_L$	Load Capacitance, from 100 MHz to 133 MHz		10	pF
$C_{IN}$	Input Capacitance		7	pF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Table 5. ELECTRICAL CHARACTERISTICS**  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$

Parameter	Description	Test Conditions	Min	Max	Unit
$V_{IL}$	Input LOW Voltage (Note 5)			0.8	V
$V_{IH}$	Input HIGH Voltage (Note 5)		2.0		V
$I_{IL}$	Input LOW Current	$V_{IN} = 0\text{ V}$		50.0	$\mu\text{A}$
$I_{IH}$	Input HIGH Current	$V_{IN} = V_{DD}$		100.0	$\mu\text{A}$
$V_{OL}$	Output LOW Voltage	$I_{OL} = 8\text{ mA (-1)}$ $I_{OL} = 12\text{ mA (-1H)}$		0.4	V
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -8\text{ mA (-1)}$ $I_{OH} = -12\text{ mA (-1H)}$	2.4		V
$I_{DD}$	Supply Current (Commercial Temp)	Unloaded outputs at 66.67 MHz, Select inputs at $V_{DD}$		34	mA
$I_{DD}$	Supply Current (Industrial Temp)	Unloaded outputs at 100 MHz 66.67 MHz 33 MHz Select inputs at $V_{DD}$ or GND, at Room Temp		50 34 19	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. REF input has a threshold voltage of  $V_{DD}/2$ .

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**Table 6. SWITCHING CHARACTERISTICS**  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$  (Note 6)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
$1/t_1$	Output Frequency	30 pF load 10 pF load	15 15		100 133	MHz
$1/t_1$	Duty Cycle = $(t_2 / t_1) * 100$ (-1, -1H)	Measured at 1.4 V, $F_{OUT} = 66.67$ MHz < 50 MHz	40 45	50 50	60 55	%
$t_3$	Output Rise Time (-1) (-1H)	Measured between 0.8 V and 2.0 V			2.5 1.5	ns
$t_4$	Output Fall Time	Measured between 2.0 V and 0.8 V			1.5	ns
$t_5$	Output-to-Output Skew	All outputs equally loaded			250	ps
$t_6$	Delay, REF Rising Edge to CLKOUT Rising Edge	Measured at $V_{DD}/2$		0	$\pm 350$	ps
$t_7$	Device-to-Device Skew	Measured at $V_{DD}/2$ on the CLKOUT pins of the device		0	700	ps
$t_8$	Output Slew Rate	Measured between 0.8 V and 2.0 V using Test Circuit #2	1			V/ns
$t_j$	Cycle-to-Cycle Jitter	Measured at 66.67 MHz, loaded out- puts			200	ps
$t_{LOCK}$	PLL Lock Time	Stable power supply, valid clock pre- sented on REF pin			1.0	ms

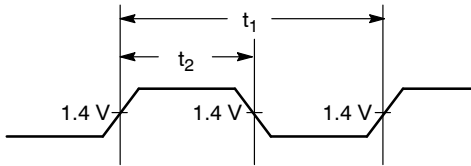
6. All parameters specified with loaded outputs in PLL-Mode.

**Zero Delay and Skew Control**

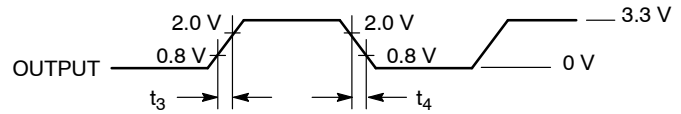
All outputs should be uniformly loaded to achieve Zero Delay between input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input-output delay.

For applications requiring zero input-output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load equal to that on other outputs, for obtaining zero-input-output delay.

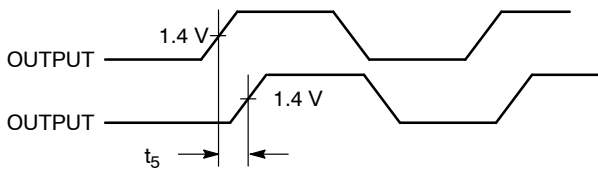
**SWITCHING WAVEFORMS**



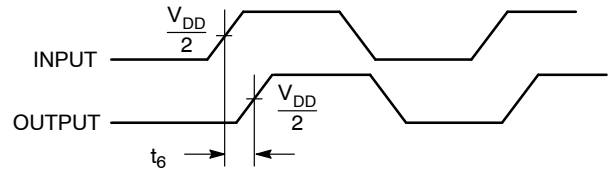
**Figure 3. Duty Cycle Timing**



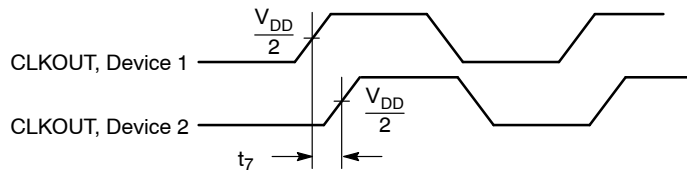
**Figure 4. All Outputs Rise/Fall Time**



**Figure 5. Output - Output Skew**

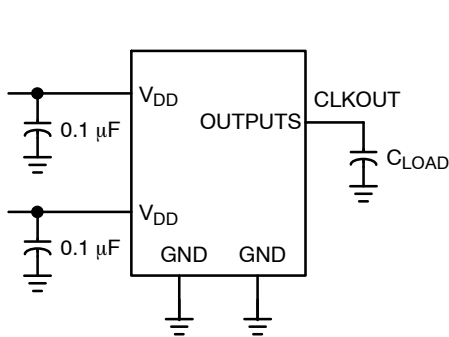


**Figure 6. Input - Output Propagation Delay**

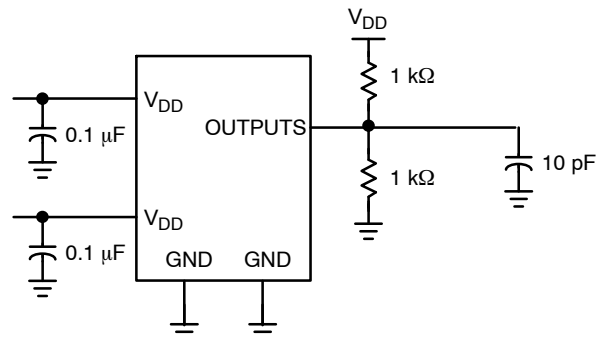


**Figure 7. Device - Device Skew**

**TEST CIRCUITS**



**Figure 8. Test Circuit #1**



**Figure 9. Test Circuit #2  
For parameter  $t_8$  (output slew rate) on -1H devices**

# NB2309A

## ORDERING INFORMATION

Device	Marking	Operating Range	Package	Shipping <sup>†</sup>
NB2309AI1DR2G	2309AI1G	Industrial & Commercial	SOIC-16 (Pb-Free)	2500 Tape & Reel
NB2309AI1DTR2G	2309 AI1	Industrial & Commercial	TSSOP-16 (Pb-Free)	2500 Tape & Reel
NB2309AI1HDTR2G	2309 AI1H	Industrial & Commercial	TSSOP-16 (Pb-Free)	2500 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

## SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

- |  |  |  |  |
|--|--|--|--|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p>                           | <p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p>   | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p>                                 | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p> |  |

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DIMENSIONS: MILLIMETERS

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



TSSOP-16  
CASE 948F-01  
ISSUE B

DATE 19 OCT 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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