MC74VHCT240A

Octal Bus Buffer/Line Driver
Inverting with 3–State Outputs

The MC74VHCT240A is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHCT240A is an inverting 3–state buffer, and has two active–low output enables. This device is designed to be used with 3–state memory address drivers, etc.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The VHCT240A input and output (when disabled) structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. These input and output structures help prevent device destruction caused by supply voltage–input/output voltage mismatch, battery backup, hot insertion, etc.

Features

• High Speed: $t_{PD} = 5.6 \text{ ns (Typ)}$ at $V_{CC} = 5.0 \text{ V}$
• Low Power Dissipation: $I_{CC} = 4 \mu A \text{ (Max)}$ at $T_A = 25^\circ \text{C}$
• TTL–Compatible Inputs: $V_{IL} = 0.8 \text{ V}; V_{IH} = 2.0 \text{ V}$
• Power Down Protection Provided on Inputs and Outputs
• Balanced Propagation Delays
• Designed for 4.5 V to 5.5 V Operating Range
• Low Noise: $V_{OLP} = 1.1 \text{ V (Max)}$
• Pin and Function Compatible with Other Standard Logic Families
• Latchup Performance Exceeds 300 mA
• ESD Performance:
  Human Body Model > 2000 V;
  Machine Model > 200 V
• Chip Complexity: 110 FETs or 27.5 Equivalent Gates
• These Devices are Pb–Free and are RoHS Compliant

[Diagram of VHCT240A and SOIC–20WB packaging]

MARKING DIAGRAMS

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or \* = Pb–Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.
The Recommended Operating Ranges limits may affect device reliability. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
MC74VHCT240A

DC ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>$V_{CC}$ V</th>
<th>$T_A = 25^\circ C$</th>
<th>$T_A = -40$ to $85^\circ C$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Minimum High–Level Input Voltage</td>
<td>4.5 to 5.5</td>
<td>2.0</td>
<td>2.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Maximum Low–Level Input Voltage</td>
<td>4.5 to 5.5</td>
<td>0.8</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Minimum High–Level Output Voltage $V_{in} = V_{IH}$ or $V_{IL}$</td>
<td>$I_{OH} = -50 \mu A$</td>
<td>4.5</td>
<td>4.4</td>
<td>4.5</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Maximum Low–Level Output Voltage $V_{in} = V_{IH}$ or $V_{IL}$</td>
<td>$I_{OL} = 50 \mu A$</td>
<td>4.5</td>
<td>0.0</td>
<td>0.1</td>
</tr>
<tr>
<td>$I_{in}$</td>
<td>Maximum Input Leakage Current $V_{in} = 5.5 , V$ or GND</td>
<td>0 to 5.5</td>
<td>± 0.1</td>
<td>± 1.0</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{OZ}$</td>
<td>Maximum 3–State Leakage Current $V_{in} = V_{IL}$ or $V_{IH}$, $V_{out} = V_{CC}$ or GND</td>
<td>5.5</td>
<td>± 0.25</td>
<td>± 2.5</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Maximum Quiescent Supply Current $V_{in} = V_{CC}$ or GND</td>
<td>5.5</td>
<td>4.0</td>
<td>40.0</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{CCT}$</td>
<td>Quiescent Supply Current Per Input: $V_{in} = 3.4 , V$ Other Input: $V_{CC}$ or GND</td>
<td>5.5</td>
<td>1.35</td>
<td>1.50</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{OPD}$</td>
<td>Output Leakage Current $V_{OUT} = 5.5 , V$</td>
<td>0</td>
<td>0.5</td>
<td>5.0</td>
<td>µA</td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Input $t_{i} = 3.0 \, ns$)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>$V_{CC}$ V</th>
<th>$T_A = 25^\circ C$</th>
<th>$T_A = -40$ to $85^\circ C$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>$I_{PLH}$, $I_{PHL}$</td>
<td>Maximum Propagation Delay A to $\overline{Y}$ or B to $\overline{Y}$</td>
<td>$V_{CC} = 5.0 \pm 0.5 , V$</td>
<td>$C_L = 15 , pF$</td>
<td>5.6</td>
<td>7.8</td>
</tr>
<tr>
<td>$I_{PZH}$</td>
<td>Output Enable Time $OEA$ to $\overline{Y}$ or $OEB$ to $\overline{Y}$</td>
<td>$V_{CC} = 5.0 \pm 0.5 , V$</td>
<td>$R_L = 1 , k\Omega$</td>
<td>7.7</td>
<td>10.4</td>
</tr>
<tr>
<td>$I_{PLZ}$</td>
<td>Output Disable Time $OEA$ to $Y$ or $OEB$ to $Y$</td>
<td>$V_{CC} = 5.0 \pm 0.5 , V$</td>
<td>$R_L = 1 , k\Omega$</td>
<td>8.8</td>
<td>11.4</td>
</tr>
<tr>
<td>$I_{OSLH}$, $I_{OSH}$</td>
<td>Output to Output Skew</td>
<td>$V_{CC} = 5.0 \pm 0.5 , V$ (Note 1)</td>
<td>$C_L = 50 , pF$</td>
<td>1.0</td>
<td>1.0</td>
</tr>
<tr>
<td>$C_{in}$</td>
<td>Maximum Input Capacitance</td>
<td>4</td>
<td>10</td>
<td>10</td>
<td>pF</td>
</tr>
<tr>
<td>$C_{out}$</td>
<td>Maximum Three–State Output Capacitance (Output in High–Impedance State)</td>
<td>9</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

$C_{PD}$ | Power Dissipation Capacitance (Note 2) | 19              |            |                   | pF                            |

Typical @ $25^\circ C$, $V_{CC} = 5.0 \, V$

1. Parameter guaranteed by design. $I_{OSLH} = |I_{PLH}| - |I_{PHL}|$, $I_{OSH} = |I_{PLH}| - |I_{PHL}|$.
2. CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{OPR} = CPD \cdot V_{CC} \cdot (I_{in} + I_{CC})/8$ (per bit). CPD is used to determine the no-load dynamic power consumption; $P_D = CPD \cdot V_{CC}^2 \cdot I_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_{i} = 3.0 \, ns$, $C_L = 50 \, pF$, $V_{CC} = 5.0 \, V$)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>$T_A = 25^\circ C$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Typ</td>
</tr>
<tr>
<td>$V_{OLP}$</td>
<td>Quiet Output Maximum Dynamic $V_{OL}$</td>
<td>0.9</td>
</tr>
<tr>
<td>$V_{OLV}$</td>
<td>Quiet Output Minimum Dynamic $V_{OL}$</td>
<td>– 0.9</td>
</tr>
<tr>
<td>$V_{IHLD}$</td>
<td>Minimum High Level Dynamic Input Voltage</td>
<td>2.0</td>
</tr>
<tr>
<td>$V_{ILD}$</td>
<td>Maximum Low Level Dynamic Input Voltage</td>
<td>0.8</td>
</tr>
</tbody>
</table>

http://onsemi.com
**Figure 3. Switching Waveform**

**Figure 4. Switching Waveform**

**Figure 5. Test Circuit**

**Figure 6. Test Circuit**

**Figure 7. Input Equivalent Circuit**

### Ordering Information

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC74VHCT240ADWRG</td>
<td>SOIC−20WB (Pb−Free)</td>
<td>1000 / Tape &amp; Reel</td>
</tr>
<tr>
<td>MC74VHCT240ADTRG</td>
<td>TSSOP−20 (Pb−Free)</td>
<td>2500 / Tape &amp; Reel</td>
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</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC–20 WB
CASE 751D–05
ISSUE H

DATE 22 APR 2015

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

<table>
<thead>
<tr>
<th>DIMENSIONS</th>
<th>MILLIMETERS</th>
</tr>
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<tbody>
<tr>
<td>A1</td>
<td>0.10 0.25</td>
</tr>
<tr>
<td>b</td>
<td>0.35 0.49</td>
</tr>
<tr>
<td>c</td>
<td>0.23 0.32</td>
</tr>
<tr>
<td>D</td>
<td>12.65 12.95</td>
</tr>
<tr>
<td>E</td>
<td>7.40 7.60</td>
</tr>
<tr>
<td>h</td>
<td>0.25 0.75</td>
</tr>
<tr>
<td>L</td>
<td>0.50 0.90</td>
</tr>
<tr>
<td>θ</td>
<td>8 7</td>
</tr>
</tbody>
</table>

SEATING PLANE

RECOMMENDED SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

PITCH 1.27

1. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “*”, may or may not be present.

DOCUMENT NUMBER: 98ASB42343B
DESCRIPTION: SOIC–20 WB

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**MECHANICAL CASE OUTLINE**

**PACKAGE DIMENSIONS**

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**TSSOP–20 WB**

**CASE 948E**

**ISSUE D**

**DATE 17 FEB 2016**

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**SCALE 2:1**

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**NOTES:**

2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

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### SOLDERING FOOTPRINT

- **DIMENSIONS:** MILLIMETERS

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### GENERIC MARKING DIAGRAM*

- **A** = Assembly Location
- **L** = Wafer Lot
- **Y** = Year
- **W** = Work Week
- **= Pb-Free Package**

*(Note: Microdot may be in either location)*

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " "*, may or may not be present.*

---

**DOCUMENT NUMBER:** 98ASH70169A

**DESCRIPTION:** TSSOP–20 WB

**Page 1 of 1**

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