

3.3 V/5 V ECL Differential Receiver/Driver with High Gain and Enable Output



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MC100EP16VC

Description

The EP16VC is a differential receiver/driver. The device is functionally equivalent to the EP16 and LVEP16 devices but with high gain and enable output.

The EP16VC provides an \overline{EN} input which is synchronized with the data input (D) signal in a way that provides glitchless gating of the QHG and \overline{QHG} outputs.

When the \overline{EN} signal is LOW, the input is passed to the outputs and the data output equals the data input. When the data input is HIGH and \overline{EN} goes HIGH, it will force the QHG LOW and the \overline{QHG} HIGH on the next negative transition of the data input. If the data input is LOW when the \overline{EN} goes HIGH, the next data transition to a HIGH is ignored and QHG remains LOW and \overline{QHG} remains HIGH. The next positive transition of the data input is not passed on to the data outputs under these conditions. The QHG and \overline{QHG} outputs remain in their disabled state as long as the \overline{EN} input is held HIGH. The \overline{EN} input has no influence on the \overline{Q} output and the data input is passed on (inverted) to this output whether \overline{EN} is HIGH or LOW. This configuration is ideal for crystal oscillator applications where the oscillator can be free running and gated on and off synchronously without adding extra counts to the output.

The V_{BB}/\overline{D} pin is internally dedicated and available for differential interconnect. V_{BB}/\overline{D} may rebias AC coupled inputs. When used, decouple V_{BB}/\overline{D} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 1.5 mA. When not used, V_{BB}/\overline{D} should be left open.

The 100 Series contains temperature compensation.

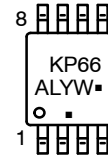
Features

- 310 ps Typical Prop Delay \overline{Q} ,
380 ps Typical Prop Delay QHG, \overline{QHG}
- Gain > 200
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range:
 - ◆ $V_{CC} = 3.0$ V to 5.5 V with $V_{EE} = 0$ V
- NECL Mode Operating Range:
 - ◆ $V_{CC} = 0$ V with $V_{EE} = -3.0$ V to -5.5 V
- Open Input Default State
- QHG Output Will Default LOW with D Inputs Open or at V_{EE}
- V_{BB} Output
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



TSSOP-8
DT SUFFIX
CASE 948R-02

MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

Device	Package	Shipping†
MC100EP16VCDTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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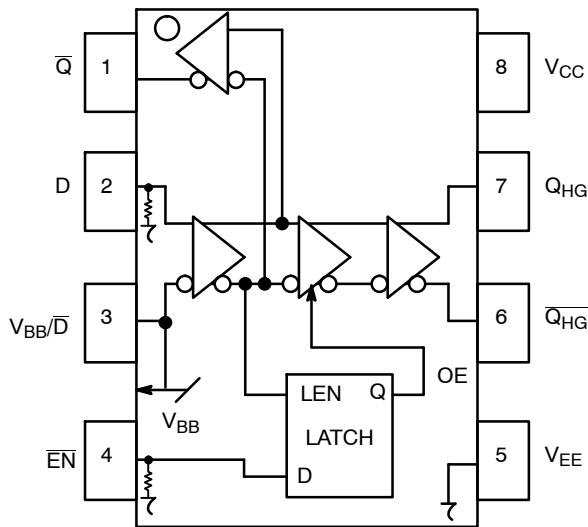


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

Pin	Function
D*	ECL Data Input
\bar{Q}	ECL Data Output
Q_{HG}, \bar{Q}_{HG}	ECL High Gain Data Outputs
\bar{EN}^*	ECL Enable Input
V_{BB}/\bar{D}	Reference Voltage Output / ECL Data Input
V_{CC}	Positive Supply
V_{EE}	Negative Supply

*Pins will default LOW when left open.

Table 2. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 k Ω
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	> 4 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb-Free Pkg
TSSOP-8	Level 3
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	167 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note [AND8003/D](#).

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Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		6	V
V_{EE}	NECL Mode Power Supply	$V_{CC} = 0\text{ V}$		-6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 -6	V
I_{out}	Output Current	Continuous Surge		50 100	mA
I_{BB}	V_{BB} Sink/Source			± 1.5	mA
T_A	Operating Temperature Range			-40 to +85	$^{\circ}\text{C}$
T_{stg}	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm		185 140	$^{\circ}\text{C}/\text{W}$
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board		41 to 44	$^{\circ}\text{C}/\text{W}$
T_{sol}	Wave Solder (Pb-Free)			265	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

Table 4. 100EP DC CHARACTERISTICS, PECL ($V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 1))

Symbol	Characteristic	-40 $^{\circ}\text{C}$			25 $^{\circ}\text{C}$			85 $^{\circ}\text{C}$			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	27	37	47	32	42	52	34	44	54	mA
V_{OH}	Output HIGH Voltage (Note 2)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 2)	1305	1400	1555	1305	1400	1555	1305	1400	1555	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
V_{BB}	Output Voltage Reference	1775	1890	2045	1775	1890	2045	1775	1890	2045	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.3 V to -2.2 V.
2. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.
3. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 5. 100EP DC CHARACTERISTICS, PECL ($V_{CC} = 5.0\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	27	37	47	32	42	52	34	44	54	mA
V_{OH}	Output HIGH Voltage (Note 2)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage (Note 2)	3005	3100	3255	3005	3100	3255	3005	3100	3255	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3775		4120	3775		4120	3775		4120	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3055		3375	3055		3375	3055		3375	mV
V_{BB}	Output Voltage Reference	3475	3490	3705	3475	3490	3705	3475	3490	3705	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +2.0 V to -0.5 V.
2. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.
3. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 6. 100EP DC CHARACTERISTICS, NECL ($V_{CC} = 0\text{ V}$; $V_{EE} = -5.5\text{ V}$ to -3.0 V (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	27	37	47	32	42	52	34	44	54	mA
V_{OH}	Output HIGH Voltage (Note 2)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V_{OL}	Output LOW Voltage (Note 2)	-1995	-1900	-1745	-1995	-1900	-1745	-1995	-1900	-1745	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1225		-880	-1225		-880	-1225		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
V_{BB}	Output Voltage Reference	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	$V_{EE} + 2.0$		0.0	$V_{EE} + 2.0$		0.0	$V_{EE} + 2.0$		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Input and output parameters vary 1:1 with V_{CC} .
2. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.
3. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 7. AC CHARACTERISTICS ($V_{CC} = 0\text{ V}$; $V_{EE} = -3.0\text{ V to } -5.5\text{ V}$ or $V_{CC} = 3.0\text{ V to } 5.5\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{\max}	Maximum Frequency (Figure 2)		> 3			> 3			> 3		GHz
t_{PLH} , t_{PHL}	Propagation Delay (Differential) \bar{Q} (Differential) QHG, $\overline{QH\bar{G}}$ (Single-Ended) \bar{Q} (Single-Ended) QHG, $\overline{QH\bar{G}}$	200 250 250 300	280 360 330 410	350 450 400 500	250 300 300 350	310 380 360 430	400 500 450 550	275 325 325 375	340 430 390 480	425 525 475 575	ps
t_S	Setup Time $\overline{EN} = L$ to D $\overline{EN} = H$ to D	50 100	15 60		50 100	5 40		50 100	18 10		ps
t_H	Hold Time $\overline{EN} = L$ to D $\overline{EN} = H$ to D	100 50	50 15		100 50	40 20		100 50	5 20		ps
t_{SKEW}	Duty Cycle Skew (Note 2)		5.0	20		5.0	20		5.0	20	ps
t_{JITTER}	RMS Random Clock Jitter (Figure 2)		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Input Voltage Swing HG (Differential Configuration) \bar{Q}	25 150	800 800	1200 1200	25 150	800 800	1200 1200	25 150	800 800	1200 1200	mV
t_r , t_f	Output Rise/Fall Times \bar{Q} (20% – 80%) QHG, $\overline{QH\bar{G}}$	200 70	300 130	400 220	250 80	350 150	450 240	250 100	350 170	500 270	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.
2. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

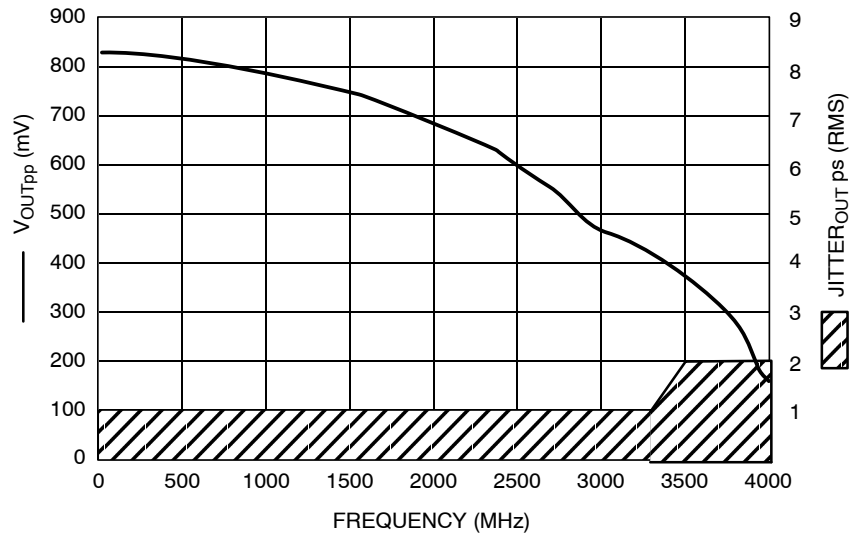


Figure 2. F_{\max} /Jitter for QHG, $\overline{QH\bar{G}}$ Output

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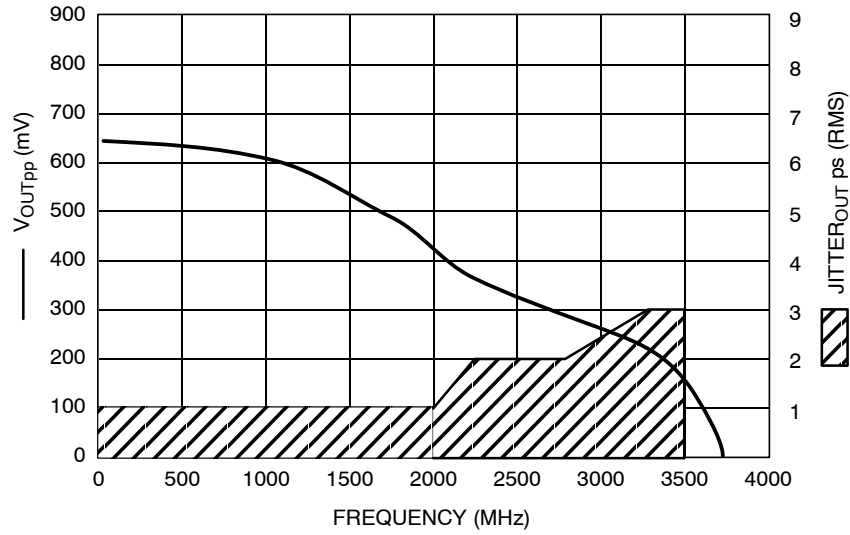


Figure 3. F_{max} /Jitter for \bar{Q} Output

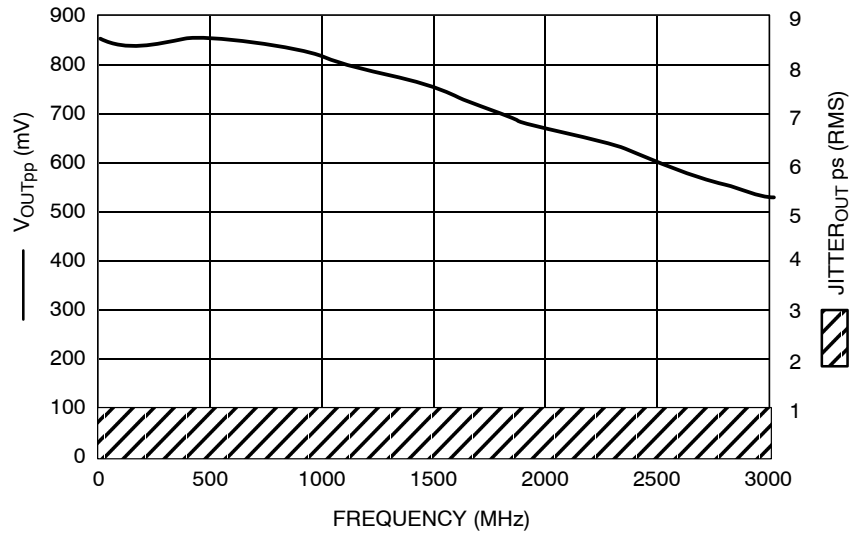


Figure 4. F_{max} /Jitter for QHG, \bar{QHG} Output

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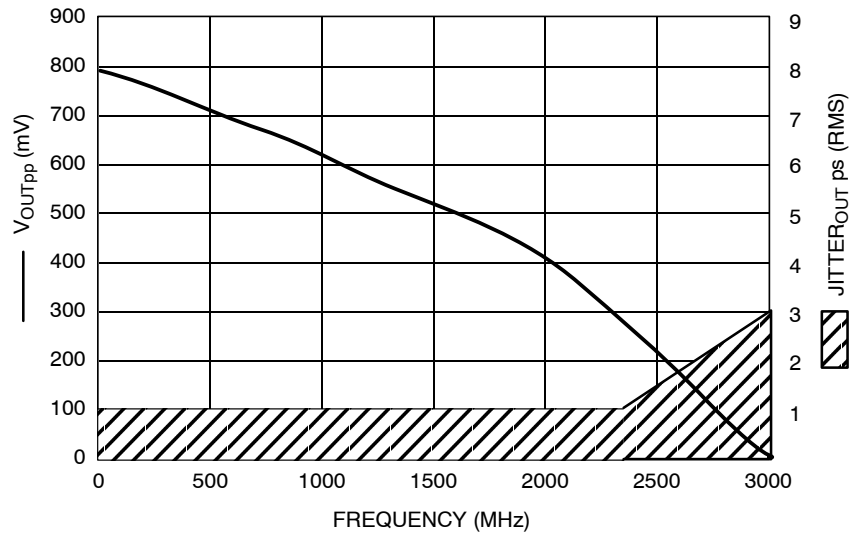


Figure 5. F_{max}/Jitter for \bar{Q} Output

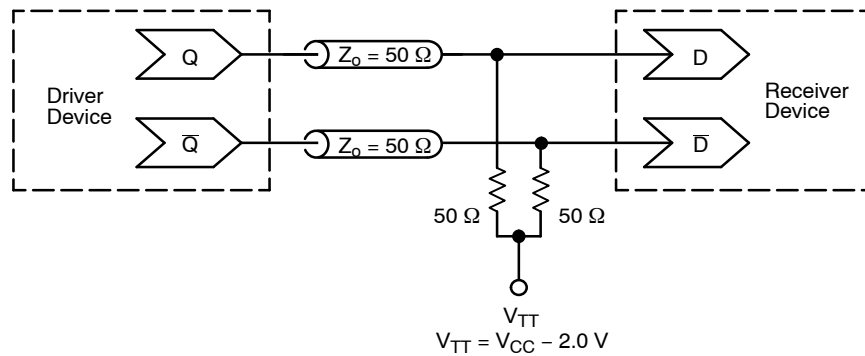


Figure 6. Typical Termination for Output Driver and Device Evaluation
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

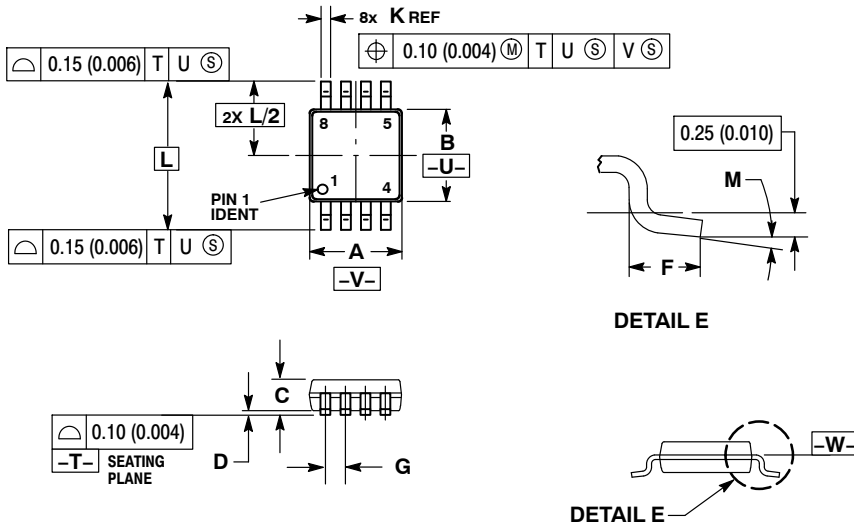
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SCALE 2:1

TSSOP 8 CASE 948R-02 ISSUE A

DATE 04/07/2000



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -V-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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