NCP331

Soft-Start Controlled Load Switch with Auto Discharge

The NCP331 is a low Ron N-channel MOSFET controlled by a soft-start sequence of 2 ms for mobile applications. The very low $R_{DS(on)}$ allows system supplying or battery charging up to DC 2A. The device is enabled due to external, active high, enable pin.

Due to a current consumption optimization, leakage current is drastically decreased from the battery connected to the device, allowing long battery life.

Features

- 1.8 V – 5.5 V Operating Range
- 33 mΩ N MOSFET
- DC Current Up to 2 A
- Peak Current Up to 5 A
- Built-in Soft-Start 2 ms
- Reverse Voltage Protection
- Output Discharge
- EN Logic Pin: Active High
- ESD Ratings:
  - Machine Model = B
  - Human Body Model = 2
- TSOP23–6 package
- This is a Pb–Free Device

Typical Applications

- Mobile Phones
- Tablets
- Digital Cameras
- GPS
- Computers

Figure 1. Typical Application Circuit

ORDERING INFORMATION
See detailed ordering and shipping information on page 7 of this data sheet.
## PIN FUNCTION DESCRIPTION

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN</td>
<td>5,6</td>
<td>POWER</td>
<td>Power-switch input voltage; connect a 0.1 μF or greater ceramic capacitor from IN to GND as close as possible to the IC.</td>
</tr>
<tr>
<td>GND</td>
<td>4</td>
<td>POWER</td>
<td>Ground connection.</td>
</tr>
<tr>
<td>EN</td>
<td>3</td>
<td>INPUT</td>
<td>Enable input, logic high turns on power switch.</td>
</tr>
<tr>
<td>OUT</td>
<td>1,2</td>
<td>OUTPUT</td>
<td>Power-switch output; connect a 0.1 μF ceramic capacitor from OUT to GND as close as possible to the IC is recommended.</td>
</tr>
</tbody>
</table>

### BLOCK DIAGRAM

![Block Diagram](image)

*Figure 2. Block Diagram*
MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN, OUT, EN, Pins:</td>
<td>$V_{\text{EN, IN, }}V_{\text{OUT}}$</td>
<td>−0.3 to +7.0</td>
<td>V</td>
</tr>
<tr>
<td>From IN to OUT Pins: Input/Output</td>
<td>$V_{\text{IN, VOUT}}$</td>
<td>−7.0 to +7.0</td>
<td>V</td>
</tr>
<tr>
<td>Maximum Junction Temperature Range</td>
<td>$T_J$</td>
<td>−40 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_{\text{STG}}$</td>
<td>−40 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>ESD Withstand Voltage</td>
<td>$V_{\text{esd}}$</td>
<td>2500</td>
<td>V</td>
</tr>
<tr>
<td>Moisture Sensitivity (Note 2)</td>
<td>MSL</td>
<td>Level 1</td>
<td></td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. According to JEDEC standard JESD22−A108.

OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{IN}}$</td>
<td>Operational Power Supply</td>
<td></td>
<td>1.8</td>
<td>5.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{EN}}$</td>
<td>Enable Voltage</td>
<td></td>
<td>0</td>
<td>5.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_A$</td>
<td>Ambient Temperature Range</td>
<td></td>
<td>−40</td>
<td>25</td>
<td>+ 85</td>
<td>°C</td>
</tr>
<tr>
<td>$T_J$</td>
<td>Junction Temperature Range</td>
<td></td>
<td>−40</td>
<td>25</td>
<td>+ 125</td>
<td>°C</td>
</tr>
<tr>
<td>$C_{\text{IN}}$</td>
<td>Decoupling Input Capacitor</td>
<td></td>
<td>0.1</td>
<td></td>
<td></td>
<td>μF</td>
</tr>
<tr>
<td>$C_{\text{OUT}}$</td>
<td>Decoupling Output Capacitor</td>
<td></td>
<td>0.1</td>
<td></td>
<td></td>
<td>μF</td>
</tr>
<tr>
<td>$R_{\text{JA}}$</td>
<td>Thermal Resistance – Junction-to-Air (Notes 3 and 4)</td>
<td></td>
<td>305</td>
<td></td>
<td></td>
<td>°C/W</td>
</tr>
<tr>
<td>$I_{\text{OUT}}$</td>
<td>Maximum DC Current</td>
<td></td>
<td></td>
<td>2</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>$P_D$</td>
<td>Power Dissipation Rating (Note 7)</td>
<td>$T_A \leq 25^\circ C$</td>
<td>0.37</td>
<td></td>
<td></td>
<td>W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = 85^\circ C$</td>
<td>0.13</td>
<td></td>
<td></td>
<td>W</td>
</tr>
</tbody>
</table>

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. The $R_{\text{JA}}$ is dependent of the PCB heat dissipation.
4. The maximum power dissipation ($P_D$) is given by the following formula:
## ELECTRICAL CHARACTERISTICS

Min & Max Limits apply for $T_A$ between $-40^\circ C$ to $+85^\circ C$ and $T_J$ up to $+125^\circ C$ for $V_{IN}$ between 1.8 V to 5.5 V (Unless otherwise noted). Typical values are referenced to $T_A = +25^\circ C$ and $V_{IN} = 5$ V.

### POWER SWITCH

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{DS(on)}$</td>
<td>Static drain–source on–state resistance</td>
<td>$V_{IN} = 3$ V, $V_{IN} = 5$ V, TSOP package</td>
<td>$T_J = 25^\circ C$</td>
<td>$-40^\circ C &lt; T_J &lt; 125^\circ C$</td>
<td>33</td>
<td>m$\Omega$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>60</td>
<td></td>
</tr>
<tr>
<td>$T_{EN}$</td>
<td>Gate turn on</td>
<td>$V_{IN} = 3.3$ V</td>
<td>From $EN$ $V_{IH}$ to $V_{OUT}$ rising. ($Note 5$), $C_{LOAD} = 0.1$ $\mu$F, $R_{LOAD} = 10$ $\Omega$</td>
<td>60</td>
<td>200</td>
<td>$\mu$s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} = 3.0$ V</td>
<td>From $EN$ $V_{IH}$ to 10% $V_{OUT}$ rising. $C_{LOAD} = 1$ $\mu$F, $R_{LOAD} = 25$ $\Omega$</td>
<td>278</td>
<td>500</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>$T_R$</td>
<td>Output rise time</td>
<td>$V_{IN} = 3.3$ V</td>
<td>$C_{LOAD} = 0.1$ $\mu$F, $R_{LOAD} = 10$ $\Omega$ ($Note 5$), from $En$ to 95% $V_{OUT}$</td>
<td>1.2</td>
<td>2.05</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} = 3.0$ V</td>
<td>$C_{LOAD} = 1$ $\mu$F, $R_{LOAD} = 25$ $\Omega$ ($Note 6$), from 10% to 90% $V_{OUT}$</td>
<td>1.00</td>
<td>1.65</td>
<td>2.36</td>
</tr>
<tr>
<td>$T_{dis}$</td>
<td>Disable time</td>
<td>$V_{IN} = 3.0$ V</td>
<td>From $EN$ high to low to $V_{OUT}$ falling</td>
<td>0.3</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>$T_F$</td>
<td>Output fall time</td>
<td>$V_{IN} = 3$ V</td>
<td>$C_{LOAD} = 1$ $\mu$F, $R_{LOAD} = 25$ $\Omega$ ($Note 6$)</td>
<td>0.1</td>
<td>0.18</td>
<td>0.5</td>
</tr>
<tr>
<td>$T_{OFF}$</td>
<td>Output off time</td>
<td>$V_{IN} = 3$ V</td>
<td>$C_{LOAD} = 1$ $\mu$F, $R_{LOAD} = 25$ $\Omega$ (Notes 6 &amp; 7), from $EN$ to 10% $V_{OUT}$</td>
<td>0.3</td>
<td>0.5</td>
<td>0.8</td>
</tr>
</tbody>
</table>

### ENABLE INPUT $EN$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>High–level input voltage</td>
<td></td>
<td>1.15</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Low–level input voltage</td>
<td></td>
<td></td>
<td>0.85</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$R_{pd}$</td>
<td>En pull–down resistor</td>
<td></td>
<td>1.1</td>
<td>1.5</td>
<td>1.8</td>
<td>M$\Omega$</td>
</tr>
<tr>
<td>$R_{dis}$</td>
<td>Output discharge resistor</td>
<td></td>
<td>200</td>
<td>400</td>
<td>600</td>
<td>$\Omega$</td>
</tr>
</tbody>
</table>

### REVERSE–LEAKAGE PROTECTION

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{REV}$</td>
<td>Reverse–current protection</td>
<td>$V_{IN} = 0$ V, $V_{OUT} = 4.2$ V (part disable), $T_A = 25^\circ C$</td>
<td>0.3</td>
<td>1.2</td>
<td></td>
<td>$\mu$A</td>
</tr>
</tbody>
</table>

### QUIESCENT CURRENT

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{stb}$</td>
<td>Standby current</td>
<td>$En$ low, $Vin = 3$ V</td>
<td>1.3</td>
<td>3</td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$I_{q}$</td>
<td>Current consumption</td>
<td>No load, $En$ high, $Vin = 3$ V</td>
<td>11</td>
<td>15</td>
<td></td>
<td>$\mu$A</td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Guaranteed by correlation with 3.0 V production test.
6. Parameters are guaranteed for $C_{LOAD}$ and $R_{LOAD}$ connected to the OUT pin with respect to the ground.
7. Guaranteed by $T_{fall}$ and $R_{discharge}$ tests.
Figure 3. Timings
TYPICAL CHARACTERISTICS

Figure 4. $R_{DS(on)}$ versus Temperature

Figure 5. $R_{DS(on)}$ versus Input Voltage, Ambient Temperature

Figure 6. Standby Current versus Input Voltage

Figure 7. Quiescent Current versus Input Voltage
FUNCTIONAL DESCRIPTION

Overview
The NCP331 is a high side N channel MOSFET power
distribution switch designed to connect external voltage
directly to the system.

Enable Input
Enable pin is an active high.
The part is in disable mode when EN is tied to low. Power
MOSFET is opened. Pull down resistor is placed to
maintained the part off if En pin is not externally driven.
The parts becomes in enable mode if EN is tied high and
Power MOSFET is turned of after ten and $t_{rise}$ times.

Auto Discharge
NMOS FET is placed between the output pin and GND,
in order to discharge the application capacitor connected on
OUT pin.

The auto-discharge is activated when EN pin is set to low
level (disable state).
The discharge path (Pull down NMOS) stays activated as
long as EN pin is set at low level.

Blocking Control
The blocking control circuitry switches the bulk of the
power NMOS. When the part is off (No $V_{IN}$ or EN tied to
GND externally), the body diode limits the leakage current
$I_{REV}$ from OUT to IN. In this mode, anode of the body diode
is connected to IN pin and cathode is connected to OUT pin.
In operating condition, anode of the body diode is connected
to OUT pin and cathode is connected to IN pin preventing
the discharge of the power supply.

APPLICATION INFORMATION

Power Dissipation
The device’s junction temperature depends on different
contributor factor such as board layout, ambient
temperature, device environment, etc... Yet, the main
contributor in term of junction temperature is the power
dissipation of the power MOSFET. Assuming this, the
power dissipation and the junction temperature in normal
mode can be calculated with the following equations:

\[
P_D = R_{DS(on)} \times (I_{OUT})^2
\]

$n = Power$ dissipation (W)
$n = Power$ MOSFET on resistance ($\Omega$)
$n = Output$ current (A)

\[
T_J = P_D \times R_{thA} + T_A
\]

$n = Junction$ temperature ($^\circ$C)
$n = Package$ thermal resistance ($^\circ$C/W)
$n = Ambient$ temperature ($^\circ$C)

PCB Recommendations
The NCP331 integrates an up to 2A rated NMOS FET, and
the PCB design rules must be respected to properly evacuate
the heat out of the silicon. By increasing PCB area, the $R_{thA}$
of the package can be decreased, allowing higher power
dissipation.

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Marking</th>
<th>Package</th>
<th>Shipping¹</th>
</tr>
</thead>
<tbody>
<tr>
<td>NCP331SNT1G</td>
<td>331</td>
<td>TSOP–6 (Pb–Free)</td>
<td>3000 / Tape &amp; Reel</td>
</tr>
</tbody>
</table>

¹For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

DIMENSIONS: MILLIMETERS

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. DRAIN
2. DRAIN
3. COLLECTOR
4. EMITTER
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 6:
PIN 1. COLLECTOR
2. DRAIN
3. BASE
4. SOURCE
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. DRAIN
3. SOURCE
4. DRAIN
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out+)
5. DOUT
6. GND

STYLE 9:
PIN 1. I/O
2. D(out)+
3. DOUT
4. D(in)
5. DOUT
6. GND

STYLE 10:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. I/O

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. I/O
6. I/O

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. SOURCE 2
5. COLLECTOR
6. COLLECTOR

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. SOURCE 1
5. SOURCE
6. DRAIN 1

STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. SOURCE
3. GATE
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. GATE
4. COLLECTOR
5. ANODE
6. COLLECTOR

RECOMMENDED SOLDERING FOOTPRINT*

For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERAL MARKING DIAGRAM*

XXXAYW

IC

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week

XXX M

STANDARD

XXX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "+", may or may not be present. Some products may not follow the Generic Marking.