Boost Regulators, 1.5 A, 280 kHz/560 kHz

**CS5171, CS5172, CS5173**

The CS5171/2/3 products are 280 kHz/560 kHz switching regulators with a high efficiency, 1.5 A integrated switch. These parts operate over a wide input voltage range, from 2.7 V to 30 V. The flexibility of the design allows the chips to operate in most power supply configurations, including boost, flyback, forward, inverting, and SEPIC. The ICs utilize current mode architecture, which allows excellent load and line regulation, as well as a practical means for limiting current. Combining high frequency operation with a highly integrated regulator circuit results in an extremely compact power supply solution. The circuit design includes provisions for features such as frequency synchronization, shutdown, and feedback controls for either positive or negative voltage regulation. These parts are pin–to–pin compatible with LT1372/1373.

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Frequency</th>
<th>Feedback Voltage Polarity</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS5171</td>
<td>280 kHz</td>
<td>positive</td>
</tr>
<tr>
<td>CS5172</td>
<td>280 kHz</td>
<td>negative</td>
</tr>
<tr>
<td>CS5173</td>
<td>560 kHz</td>
<td>positive</td>
</tr>
</tbody>
</table>

**Features**
- Integrated Power Switch: 1.5 A Guaranteed
- Wide Input Range: 2.7 V to 30 V
- High Frequency Allows for Small Components
- Minimum External Components
- Easy External Synchronization
- Built in Overcurrent Protection
- Frequency Foldback Reduces Component Stress During an Overcurrent Condition
- Thermal Shutdown with Hysteresis
- Regulates Either Positive or Negative Output Voltages
- Shut Down Current: 50 μA Maximum
- Pin–to–Pin Compatible with LT1372/1373
- Wide Temperature Range
  - Industrial Grade: –40°C to 125°C
  - Commercial Grade: 0°C to 125°C
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

**MARKING DIAGRAM AND PIN CONNECTIONS**

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 20 of this data sheet.
Figure 1. Applications Diagram

MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction Temperature Range, $T_J$</td>
<td>$-40$ to $+150$</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range, $T_{STORAGE}$</td>
<td>$-65$ to $+150$</td>
<td>°C</td>
</tr>
<tr>
<td>Package Thermal Resistance, $R_{Th JC}$</td>
<td>45</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{Th JA}$</td>
<td>165</td>
<td>°C/W</td>
</tr>
<tr>
<td>Lead Temperature Soldering: Reflow (Note 1)</td>
<td>260 Peak</td>
<td>°C</td>
</tr>
<tr>
<td>ESD, Human Body Model</td>
<td>1.2</td>
<td>kV</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. 60 second maximum above 183°C.

MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Symbol</th>
<th>$V_{MAX}$</th>
<th>$V_{MIN}$</th>
<th>$I_{SOURCE}$</th>
<th>$I_{SINK}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC Power Input</td>
<td>$V_{CC}$</td>
<td>35 V</td>
<td>$-0.3$ V</td>
<td>N/A</td>
<td>200 mA</td>
</tr>
<tr>
<td>Shutdown/Sync</td>
<td>SS</td>
<td>30 V</td>
<td>$-0.3$ V</td>
<td>1.0 mA</td>
<td>1.0 mA</td>
</tr>
<tr>
<td>Loop Compensation</td>
<td>$V_{C}$</td>
<td>6.0 V</td>
<td>$-0.3$ V</td>
<td>10 mA</td>
<td>10 mA</td>
</tr>
<tr>
<td>Voltage Feedback Input</td>
<td>FB</td>
<td>10 V</td>
<td>$-0.3$ V</td>
<td>1.0 mA</td>
<td>1.0 mA</td>
</tr>
<tr>
<td>Negative Feedback Input (transient, 10 ms)</td>
<td>NFB (CS5171/3 only)</td>
<td>$-10$ V</td>
<td>10 V</td>
<td>1.0 mA</td>
<td>1.0 mA</td>
</tr>
<tr>
<td>Test Pin</td>
<td>Test</td>
<td>6.0 V</td>
<td>$-0.3$ V</td>
<td>1.0 mA</td>
<td>1.0 mA</td>
</tr>
<tr>
<td>Power Ground</td>
<td>PGND</td>
<td>0.3 V</td>
<td>$-0.3$ V</td>
<td>4 A</td>
<td>10 mA</td>
</tr>
<tr>
<td>Analog Ground</td>
<td>AGND</td>
<td>0 V</td>
<td>0 V</td>
<td>N/A</td>
<td>10 mA</td>
</tr>
<tr>
<td>Switch Input</td>
<td>$V_{SW}$</td>
<td>40 V</td>
<td>$-0.3$ V</td>
<td>10 mA</td>
<td>3.0 A</td>
</tr>
</tbody>
</table>
### ELECTRICAL CHARACTERISTICS

(2.7 V < V_{CC} < 30 V; Industrial Grade: −40°C < T_J < 125°C; Commercial Grade: 0°C < T_J < 125°C; For all CS5171/2/3/4 specifications unless otherwise stated.)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Positive and Negative Error Amplifiers</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FB Reference Voltage (CS5171/3 only)</td>
<td>( V_C ) tied to FB; measure at FB</td>
<td>1.246</td>
<td>1.276</td>
<td>1.300</td>
<td>V</td>
</tr>
<tr>
<td>NFB Reference Voltage (CS5172 only)</td>
<td>( V_C = 1.25 \text{ V} )</td>
<td>−2.55</td>
<td>−2.45</td>
<td>−2.35</td>
<td>V</td>
</tr>
<tr>
<td>FB Input Current (CS5171/3 only)</td>
<td>( \text{FB} = \text{V}_{\text{REF}} )</td>
<td>−1.0</td>
<td>0.1</td>
<td>1.0</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>NFB Input Current (CS5172 only)</td>
<td>( \text{NFB} = \text{NV}_{\text{REF}} )</td>
<td>−16</td>
<td>−10</td>
<td>−5.0</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>FB Reference Voltage Line Regulation (CS5171/3 only)</td>
<td>( V_C = \text{FB} )</td>
<td>–</td>
<td>0.01</td>
<td>0.03</td>
<td>%/V</td>
</tr>
<tr>
<td>NFB Reference Voltage Line Regulation (CS5172 only)</td>
<td>( V_C = 1.25 \text{ V} )</td>
<td>–</td>
<td>0.01</td>
<td>0.05</td>
<td>%/V</td>
</tr>
<tr>
<td><strong>Positive and Negative Error Amplifiers</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Positive Error Amp Transconductance</td>
<td>( I_{V_C} = \pm 25 \text{ ( \mu \text{A} )} )</td>
<td>300</td>
<td>550</td>
<td>800</td>
<td>( \mu \text{Mho} )</td>
</tr>
<tr>
<td>Negative Error Amp Transconductance</td>
<td>( I_{V_C} = \pm 5 \text{ ( \mu \text{A} )} )</td>
<td>115</td>
<td>160</td>
<td>225</td>
<td>( \mu \text{Mho} )</td>
</tr>
<tr>
<td>Positive Error Amp Gain (Note 2)</td>
<td></td>
<td>200</td>
<td>500</td>
<td>–</td>
<td>V/V</td>
</tr>
<tr>
<td>Negative Error Amp Gain (Note 2)</td>
<td></td>
<td>100</td>
<td>180</td>
<td>320</td>
<td>V/V</td>
</tr>
<tr>
<td><strong>Oscillator</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Base Operating Frequency</td>
<td>CS5171/2, ( \text{FB} = 1 \text{ V or NFB} = -1.9 \text{ V} )</td>
<td>230</td>
<td>280</td>
<td>310</td>
<td>kHz</td>
</tr>
<tr>
<td>Reduced Operating Frequency</td>
<td>CS5171/2, ( \text{FB} = 0 \text{ V or NFB} = 0 \text{ V} )</td>
<td>30</td>
<td>52</td>
<td>120</td>
<td>kHz</td>
</tr>
<tr>
<td>Maximum Duty Cycle</td>
<td>CS5171/2</td>
<td>90</td>
<td>94</td>
<td>–</td>
<td>%</td>
</tr>
<tr>
<td>Base Operating Frequency</td>
<td>CS5173/4, ( \text{FB} = 1 \text{ V or NFB} = -1.9 \text{ V} )</td>
<td>460</td>
<td>560</td>
<td>620</td>
<td>kHz</td>
</tr>
<tr>
<td>Reduced Operating Frequency</td>
<td>CS5173/4, ( \text{FB} = 0 \text{ V or NFB} = 0 \text{ V} )</td>
<td>60</td>
<td>104</td>
<td>160</td>
<td>kHz</td>
</tr>
<tr>
<td>Maximum Duty Cycle</td>
<td>CS5173/4</td>
<td>62</td>
<td>90</td>
<td>–</td>
<td>%</td>
</tr>
<tr>
<td>NFB Frequency Shift Threshold</td>
<td>Frequency drops to reduced operating frequency</td>
<td>−0.80</td>
<td>−0.65</td>
<td>−0.50</td>
<td>V</td>
</tr>
<tr>
<td>FB Frequency Shift Threshold</td>
<td>Frequency drops to reduced operating frequency</td>
<td>0.36</td>
<td>0.40</td>
<td>0.44</td>
<td>V</td>
</tr>
<tr>
<td><strong>Sync/ Shutdown</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sync Range</td>
<td>CS5171/2</td>
<td>320</td>
<td>–</td>
<td>500</td>
<td>kHz</td>
</tr>
<tr>
<td>Sync Range</td>
<td>CS5173/4</td>
<td>640</td>
<td>–</td>
<td>1000</td>
<td>kHz</td>
</tr>
<tr>
<td>Sync Pulse Transition Threshold</td>
<td>Rise time = 20 ns</td>
<td>2.5</td>
<td>–</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>SS Bias Current</td>
<td>( \text{SS} = 0 \text{ V} )</td>
<td>−15</td>
<td>−3.0</td>
<td>–</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td></td>
<td>( \text{SS} = 3.0 \text{ V} )</td>
<td>–</td>
<td>3.0</td>
<td>8.0</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>Shutdown Threshold</td>
<td></td>
<td>0.50</td>
<td>0.85</td>
<td>1.20</td>
<td>V</td>
</tr>
<tr>
<td>Shutdown Delay</td>
<td>( 2.7 \text{ V} \leq V_{\text{CC}} \leq 12 \text{ V} )</td>
<td>12</td>
<td>80</td>
<td>350</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td></td>
<td>( 12 \text{ V} &lt; V_{\text{CC}} \leq 30 \text{ V} )</td>
<td>12</td>
<td>36</td>
<td>200</td>
<td>( \mu \text{s} )</td>
</tr>
</tbody>
</table>

2. Guaranteed by design, not 100% tested in production.
**ELECTRICAL CHARACTERISTICS** (2.7 V < VCC < 30 V; Industrial Grade: −40°C < TJ < 125°C; Commercial Grade: 0°C < TJ < 125°C; For all CS5171/2/3/4 specifications unless otherwise stated.)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power Switch</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switch Saturation Voltage</td>
<td>ISWITCH = 1.5 A, (Note 3)</td>
<td></td>
<td>0.8</td>
<td>1.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>ISWITCH = 1.0 A, 0°C ≤ TJ ≤ 85°C</td>
<td></td>
<td>0.55</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>ISWITCH = 1.0 A, −40°C ≤ TJ ≤ 0°C</td>
<td></td>
<td>0.75</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>ISWITCH = 10 mA</td>
<td></td>
<td>0.09</td>
<td>0.45</td>
<td>V</td>
</tr>
<tr>
<td>Switch Current Limit</td>
<td>50% duty cycle, (Note 3)</td>
<td>1.6</td>
<td>1.9</td>
<td>2.4</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>80% duty cycle, (Note 3)</td>
<td>1.5</td>
<td>1.7</td>
<td>2.2</td>
<td>A</td>
</tr>
<tr>
<td>Minimum Pulse Width</td>
<td>FB = 0 V or NFB = 0 V, ISW = 4.0 A, (Note 3)</td>
<td>200</td>
<td>250</td>
<td>300</td>
<td>ns</td>
</tr>
<tr>
<td>ΔICC/ΔVSW</td>
<td>2.7 V ≤ VCC ≤ 12 V, 10 mA ≤ ISW ≤ 1.0 A</td>
<td></td>
<td>10</td>
<td>30</td>
<td>mA/A</td>
</tr>
<tr>
<td></td>
<td>12 V ≤ VCC ≤ 30 V, 10 mA ≤ ISW ≤ 1.0 A</td>
<td></td>
<td>−</td>
<td>100</td>
<td>mA/A</td>
</tr>
<tr>
<td></td>
<td>2.7 V ≤ VCC ≤ 12 V, 10 mA ≤ ISW ≤ 1.5 A, (Note 3)</td>
<td></td>
<td>17</td>
<td>30</td>
<td>mA/A</td>
</tr>
<tr>
<td></td>
<td>12 V &lt; VCC ≤ 30 V, 10 mA ≤ ISW ≤ 1.5 A, (Note 3)</td>
<td></td>
<td>−</td>
<td>100</td>
<td>mA/A</td>
</tr>
<tr>
<td>Switch Leakage</td>
<td>VSW = 40 V, VCC = 0V</td>
<td>−</td>
<td>2.0</td>
<td>100</td>
<td>μA</td>
</tr>
<tr>
<td><strong>General</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Current</td>
<td>ISW = 0</td>
<td>−</td>
<td>5.5</td>
<td>8.0</td>
<td>mA</td>
</tr>
<tr>
<td>Shutdown Mode Current</td>
<td>VC &lt; 0.8 V, SS = 0 V, 2.7 V ≤ VCC ≤ 12 V</td>
<td>−</td>
<td>12</td>
<td>60</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>VC &lt; 0.8 V, SS = 0 V, 12 V ≤ VCC ≤ 30 V</td>
<td>−</td>
<td>−</td>
<td>100</td>
<td>μA</td>
</tr>
<tr>
<td>Minimum Operation Input Voltage</td>
<td>VSW switching, maximum ISW = 10 mA</td>
<td>−</td>
<td>2.45</td>
<td>2.70</td>
<td>V</td>
</tr>
<tr>
<td>Thermal Shutdown</td>
<td>(Note 3)</td>
<td>150</td>
<td>180</td>
<td>210</td>
<td>°C</td>
</tr>
<tr>
<td>Thermal Hysteresis</td>
<td>(Note 3)</td>
<td>−</td>
<td>25</td>
<td>−</td>
<td>°C</td>
</tr>
</tbody>
</table>

3. Guaranteed by design, not 100% tested in production.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**PACKAGE PIN DESCRIPTION**

<table>
<thead>
<tr>
<th>Package Pin #</th>
<th>Pin Symbol</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VC</td>
<td>Loop compensation pin. The VC pin is the output of the error amplifier and is used for loop compensation, current limit and soft start. Loop compensation can be implemented by a simple RC network as shown in the application diagram on page 2 as R1 and C1.</td>
</tr>
<tr>
<td>2 (CS5171/3 only)</td>
<td>FB</td>
<td>Positive regulator feedback pin. This pin senses a positive output voltage and is referenced to 1.276 V. When the voltage at this pin falls below 0.4 V, chip switching frequency reduces to 20% of the nominal frequency.</td>
</tr>
<tr>
<td>2 (CS5172) 3 CS5171/3</td>
<td>Test</td>
<td>These pins are connected to internal test logic and should either be left floating or tied to ground. Connection to a voltage between 2 V and 6 V shuts down the internal oscillator and leaves the power switch running.</td>
</tr>
<tr>
<td>3 (CS5172)</td>
<td>NFB</td>
<td>Negative feedback pin. This pin senses a negative output voltage and is referenced to −2.5 V. When the voltage at this pin goes above −0.65 V, chip switching frequency reduces to 20% of the nominal frequency.</td>
</tr>
<tr>
<td>4</td>
<td>SS</td>
<td>Synchronization and shutdown pin. This pin may be used to synchronize the part to nearly twice the base frequency. A TTL low will shut the part down and put it into low current mode. If synchronization is not used, this pin should be either tied high or left floating for normal operation.</td>
</tr>
<tr>
<td>5</td>
<td>VCC</td>
<td>Input power supply pin. This pin supplies power to the part and should have a bypass capacitor connected to AGND.</td>
</tr>
</tbody>
</table>
### PACKAGE PIN DESCRIPTION

<table>
<thead>
<tr>
<th>Package Pin #</th>
<th>Pin Symbol</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>AGND</td>
<td>Analog ground. This pin provides a clean ground for the controller circuitry and should not be in the path of large currents. The output voltage sensing resistors should be connected to this ground pin. This pin is connected to the IC substrate.</td>
</tr>
<tr>
<td>7</td>
<td>PGND</td>
<td>Power ground. This pin is the ground connection for the emitter of the power switching transistor. Connection to a good ground plane is essential.</td>
</tr>
<tr>
<td>8</td>
<td>VSW</td>
<td>High current switch pin. This pin connects internally to the collector of the power switch. The open voltage across the power switch can be as high as 40 V. To minimize radiation, use a trace as short as practical.</td>
</tr>
</tbody>
</table>

---

**Figure 2. Block Diagram**
**TYPICAL PERFORMANCE CHARACTERISTICS**

**Figure 3.** $I_{CC}$ (No Switching) vs. Temperature

**Figure 4.** $\Delta I_{CC}/\Delta I_{SW}$ vs. Temperature

**Figure 5.** $V_{CE(SAT)}$ vs. $I_{SW}$

**Figure 6.** Minimum Input Voltage vs. Temperature

**Figure 7.** Switching Frequency vs. Temperature (CS5171/2 only)

**Figure 8.** Switching Frequency vs. Temperature (CS5173 only)
TYPICAL PERFORMANCE CHARACTERISTICS

**Figure 9.** Switching Frequency vs. $V_{FB}$ (CS5171/3 only)

**Figure 10.** Switching Frequency vs. $V_{NFB}$ (CS5172 only)

**Figure 11.** Reference Voltage vs. Temperature (CS5171/3 only)

**Figure 12.** Reference Voltage vs. Temperature (CS5172 only)

**Figure 13.** $I_{FB}$ vs. Temperature (CS5171/3 only)

**Figure 14.** $I_{NFB}$ vs. Temperature (CS5172 only)
TYPICAL PERFORMANCE CHARACTERISTICS

Figure 15. Current Limit vs. Temperature

Figure 16. Maximum Duty Cycle vs. Temperature

Figure 17. V_C Threshold and High Clamp Voltage vs. Temperature

Figure 18. Shutdown Threshold vs. Temperature

Figure 19. Shutdown Delay vs. Temperature

Figure 20. I_SS vs. V_SS
CS5171, CS5172, CS5173

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 21. ICC vs. VIN During Shutdown

Figure 22. Error Amplifier Transconductance vs. Temperature (CS5171/3 only)

Figure 23. Negative Error Amplifier Transconductance vs. Temperature (CS5172 only)

Figure 24. Error Amplifier IOUT vs. VFB (CS5171/3 only)

Figure 25. Error Amplifier IOUT vs. VNFB (CS5172 only)

Figure 26. Switch Leakage vs. Temperature
The CS517x family incorporates a current mode control scheme, in which the PWM ramp signal is derived from the power switch current. This ramp signal is compared to the output of the error amplifier to control the on–time of the power switch. The oscillator is used as a fixed–frequency clock to ensure a constant operational frequency. The resulting control scheme features several advantages over conventional voltage mode control. First, derived directly from the inductor, the ramp signal responds immediately to line voltage changes. This eliminates the delay caused by the output filter and error amplifier, which is commonly found in voltage mode controllers. The second benefit comes from inherent pulse–by–pulse current limiting by merely clamping the peak switching current. Finally, since current mode commands an output current rather than voltage, the filter offers only a single pole to the feedback loop. This allows both a simpler compensation and a higher gain–bandwidth over a comparable voltage mode circuit.

Without discrediting its apparent merits, current mode control comes with its own peculiar problems, mainly, subharmonic oscillation at duty cycles over 50%. The CS517x family solves this problem by adopting a slope compensation scheme in which a fixed ramp generated by the oscillator is added to the current ramp. A proper slope rate is provided to improve circuit stability without sacrificing the advantages of current mode control.

**Oscillator and Shutdown**

The oscillator is trimmed to guarantee an 18% frequency accuracy. The output of the oscillator turns on the power switch at a frequency of 280 kHz (CS5171/2) or 560 kHz (CS5173/4), as shown in Figure 27. The power switch is turned off by the output of the PWM Comparator.

A TTL–compatible sync input at the SS pin is capable of syncing up to 1.8 times the base oscillator frequency. As shown in Figure 28, in order to sync to a higher frequency, a positive transition turns on the power switch before the output of the oscillator goes high, thereby resetting the oscillator. The sync operation allows multiple power supplies to operate at the same frequency.

A sustained logic low at the SS pin will shut down the IC and reduce the supply current.

An additional feature includes frequency shift to 20% of the nominal frequency when either the NFB or FB pins trigger the threshold. During power up, overload, or short circuit conditions, the minimum switch on–time is limited by the PWM comparator minimum pulse width. Extra switch off–time reduces the minimum duty cycle to protect external components and the IC itself.

As previously mentioned, this block also produces a ramp for the slope compensation to improve regulator stability.

**Error Amplifier**

The NFB pin is internally referenced to −2.5 V with approximately a 250 kΩ input impedance. For CS5171/3, the FB pin is directly connected to the inverting input of the positive error amplifier, whose non–inverting input is fed by the 1.276 V reference. Both amplifiers are transconducance amplifiers with a high output impedance of approximately 1 MΩ, as shown in Figure 29. The VC pin is connected to the output of the error amplifiers and is internally clamped between 0.5 V and 1.7 V. A typical connection at the VC pin includes a capacitor in series with a resistor to ground, forming a pole/zero for loop compensation.

An external shunt can be connected between the VC pin and ground to reduce its clamp voltage. Consequently, the current limit of the internal power transistor current is reduced from its nominal value.
Switch Driver and Power Switch

The switch driver receives a control signal from the logic section to drive the output power switch. The switch is grounded through emitter resistors (63 mΩ total) to the PGND pin. PGND is not connected to the IC substrate so that switching noise can be isolated from the analog ground. The peak switching current is clamped by an internal circuit. The clamp current is guaranteed to be greater than 1.5 A and varies with duty cycle due to slope compensation. The power switch can withstand a maximum voltage of 40 V on the collector (VSW pin). The saturation voltage of the switch is typically less than 1 V to minimize power dissipation.

Short Circuit Condition

When a short circuit condition happens in a boost circuit, the inductor current will increase during the whole switching cycle, causing excessive current to be drawn from the input power supply. Since control ICs don’t have the means to limit load current, an external current limit circuit (such as a fuse or relay) has to be implemented to protect the load, power supply and ICs.

In other topologies, the frequency shift built into the IC prevents damage to the chip and external components. This feature reduces the minimum duty cycle and allows the transformer secondary to absorb excess energy before the switch turns back on.

Figure 30. Startup Waveforms of Circuit Shown in the Application Diagram. Load = 400 mA.

The high DC gain in Figure 32 is desirable for achieving DC accuracy over line and load variations. The DC gain of a transconductance error amplifier can be calculated as follows:

\[
\text{Gain}_{\text{DC}} = G_M \times R_O
\]

where:

- \(G_M\) = error amplifier transconductance;
- \(R_O\) = error amplifier output resistance = 1 MΩ

The low frequency pole, \(f_{P1}\), is determined by the error amplifier output resistance and \(C_1\) as:

\[
f_{P1} = \frac{1}{2\pi C_1 R_O}
\]
The first zero generated by C1 and R1 is:

\[ f_{Z1} = \frac{1}{2\pi C_1 R_1} \]

The phase lead provided by this zero ensures that the loop has at least a 45° phase margin at the crossover frequency. Therefore, this zero should be placed close to the pole generated in the power stage which can be identified at frequency:

\[ f_P = \frac{1}{2\pi C_0 R_{LOAD}} \]

where:

- \( C_0 \) = output capacitor of the boost regulator.
- \( R_{LOAD} \) = load resistance.

The high frequency pole, \( f_{P2} \), can be placed at the output filter’s ESR zero or at half the switching frequency. Placing the pole at this frequency will cut down on switching noise. The frequency of this pole is determined by the value of C2 and R1:

\[ f_{P2} = \frac{1}{2\pi C_2 R_1} \]

One simple method to ensure adequate phase margin is to design the frequency response with a \(-20\) dB per decade slope, until unity-gain crossover. The crossover frequency should be selected at the midpoint between \( f_{Z1} \) and \( f_{P2} \) where the phase margin is maximized.

\[ \text{Figure 32. Bode Plot of the Compensation Network Shown in Figure 31} \]

**Negative Voltage Feedback**

Since the negative error amplifier has finite input impedance as shown in Figure 33, its induced error has to be considered. If a voltage divider is used to scale down the negative output voltage for the NFB pin, the equation for calculating output voltage is:

\[ -V_{OUT} = \left( \frac{-2.5 (R_1 + R_2)}{R_2} \right) - 10 \mu A \times R_1 \]

**Figure 33. Negative Error Amplifier and NFB Pin**

It is shown that if \( R_1 \) is less than 10 k, the deviation from the design target will be less than 0.1 V. If the tolerances of the negative voltage reference and NFB pin input current are considered, the possible offset of the output \( V_{OFFSET} \) varies in the range of:

\[ \left( -0.05 \times \frac{R_1 + R_2}{R_2} \right) \leq V_{OFFSET} \leq \left( 0.05 \times \frac{R_1 + R_2}{R_2} \right) \]

**VSW Voltage Limit**

In the boost topology, \( V_{SW} \) pin maximum voltage is set by the maximum output voltage plus the output diode forward voltage. The diode forward voltage is typically 0.5 V for Schottky diodes and 0.8 V for ultrafast recovery diodes

\[ V_{SW(MAX)} = V_{OUT(MAX)} + V_F \]

where:

- \( V_F \) = output diode forward voltage.

In the flyback topology, peak \( V_{SW} \) voltage is governed by:

\[ V_{SW(MAX)} = V_{CC(MAX)} + (V_{OUT} + V_F) \times N \]

where:

- \( N \) = transformer turns ratio, primary over secondary.

When the power switch turns off, there exists a voltage spike superimposed on top of the steady-state voltage. Usually this voltage spike is caused by transformer leakage inductance charging stray capacitance between the \( V_{SW} \) and \( PGND \) pins. To prevent the voltage at the \( V_{SW} \) pin from exceeding the maximum rating, a transient voltage suppressor in series with a diode is paralleled with the primary windings. Another method of clamping switch voltage is to connect a transient voltage suppressor between the \( V_{SW} \) pin and ground.
Magnetic Component Selection

When choosing a magnetic component, one must consider factors such as peak current, core and ferrite material, output voltage ripple, EMI, temperature range, physical size and cost. In boost circuits, the average inductor current is the product of output current and voltage gain ($V_{OUT}/V_{CC}$), assuming 100% energy transfer efficiency. In continuous conduction mode, inductor ripple current is

$$I_{RIPPLE} = \frac{V_{CC}(V_{OUT} - V_{CC})}{(f)(L)(V_{OUT})}$$

where:

- $f = 280$ kHz for CS5171/2 and 560 kHz for CS5173/4.

The peak inductor current is equal to average current plus half of the ripple current, which should not cause inductor saturation. The above equation can also be referenced when selecting the value of the inductor based on the tolerance of the ripple current in the circuits. Small ripple current provides the benefits of small input capacitors and greater output current capability. A core geometry like a rod or barrel is prone to generating high magnetic field radiation, but is relatively cheap and small. Other core geometries, such as toroids, provide a closed magnetic loop to prevent EMI.

Input Capacitor Selection

In boost circuits, the inductor becomes part of the input filter, as shown in Figure 35. In continuous mode, the input current waveform is triangular and does not contain a large pulsed current, as shown in Figure 34. This reduces the requirements imposed on the input capacitor selection. During continuous conduction mode, the peak to peak inductor ripple current is given in the previous section. As we can see from Figure 34, the product of the inductor current ripple and the input capacitor’s effective series resistance (ESR) determine the $V_{CC}$ ripple. In most applications, input capacitors in the range of 10 μF to 100 μF with an ESR less than 0.3 Ω work well up to a full 1.5 A switch current.

Output Capacitor Selection

By examining the waveforms shown in Figure 36, we can see that the output voltage ripple comes from two major sources, namely capacitor ESR and the charging/discharging of the output capacitor. In boost circuits, when the power switch turns off, $I_L$ flows into the output capacitor causing an instant $\Delta V = I_{IN} \times ESR$. At the same time, current $I_L - I_{OUT}$ charges the capacitor and increases the output voltage gradually. When the power switch is turned on, $I_L$ is shunted to ground and $I_{OUT}$ discharges the output capacitor. When the $I_C$ ripple is small enough, $I_L$ can be treated as a constant and is equal to input current $I_{IN}$.

Figure 34. Boost Input Voltage and Current Ripple Waveforms

Figure 35. Boost Circuit Effective Input Filter

Figure 36. Typical Output Voltage Ripple
Summing up, the output voltage peak−peak ripple can be calculated by:

\[ V_{OUT(ripple)} = \frac{(I_{IN} - I_{OUT})(1 - D)}{(C_{OUT})(f)} + \frac{I_{OUT}D}{(C_{OUT})(f)} + I_{IN} \times ESR \]

The equation can be expressed more conveniently in terms of \( V_{CC} \), \( V_{OUT} \), and \( I_{OUT} \) for design purposes as follows:

\[ V_{OUT(ripple)} = \frac{I_{OUT}(V_{OUT} - V_{CC})}{(C_{OUT})(f)} \times \frac{1}{(C_{OUT})(f)} + \frac{(I_{OUT})(V_{OUT})(ESR)}{V_{CC}} \]

The capacitor RMS ripple current is:

\[ I_{RIPPLE} = \sqrt{(I_{IN} - I_{OUT})^2(1 - D) + (I_{OUT})^2(1 - D)} \]

\[ = I_{OUT} \sqrt{\frac{V_{OUT} - V_{CC}}{V_{CC}}} \]

Although the above equations apply only for boost circuits, similar equations can be derived for flyback circuits.

**Reducing the Current Limit**

In some applications, the designer may prefer a lower limit on the switch current than 1.5 A. An external shunt can be connected between the \( V_{C} \) pin and ground to reduce its clamp voltage. Consequently, the current limit of the internal power transistor current is reduced from its nominal value.

The voltage on the \( V_{C} \) pin can be evaluated with the equation

\[ V_{C} = I_{SW}R_{EAV} \]

where:

- \( R_{E} = .063 \Omega \), the value of the internal emitter resistor;
- \( A_{V} = 5 \text{ V/\text{V}} \), the gain of the current sense amplifier.

Since \( R_{E} \) and \( A_{V} \) cannot be changed by the end user, the only available method for limiting switch current below 1.5 A is to clamp the \( V_{C} \) pin at a lower voltage. If the maximum switch or inductor current is substituted into the equation above, the desired clamp voltage will result.

A simple diode clamp, as shown in Figure 37, clamps the \( V_{C} \) voltage to a diode drop above the voltage on resistor \( R_{3} \).

Unfortunately, such a simple circuit is not generally acceptable if \( V_{IN} \) is loosely regulated.

---

**Figure 37. Current Limiting using a Diode Clamp**

Another solution to the current limiting problem is to externally measure the current through the switch using a sense resistor. Such a circuit is illustrated in Figure 38.

---

**Figure 38. Current Limiting using a Current Sense Resistor**

The switch current is limited to

\[ I_{SWITCH(PEAK)} = \frac{V_{BE(Q1)}}{R_{SENSE}} \]

where:

- \( V_{BE(Q1)} \) = the base−emitter voltage drop of Q1, typically 0.65 V.
The improved circuit does not require a regulated voltage to operate properly. Unfortunately, a price must be paid for this convenience in the overall efficiency of the circuit. The designer should note that the input and output grounds are no longer common. Also, the addition of the current sense resistor, \( R_{SENSE} \), results in a considerable power loss which increases with the duty cycle. Resistor \( R2 \) and capacitor \( C3 \) form a low-pass filter to remove noise.

**Subharmonic Oscillation**

Subharmonic oscillation (SHM) is a problem found in current-mode control systems, where instability results when duty cycle exceeds 50%. SHM only occurs in switching regulators with a continuous inductor current. This instability is not harmful to the converter and usually does not affect the output voltage regulation. SHM will increase the radiated EM noise from the converter and can cause, under certain circumstances, the inductor to emit high-frequency audible noise.

SHM is an easily remedied problem. The rising slope of the inductor current is supplemented with internal “slope compensation” to prevent any duty cycle instability from carrying through to the next switching cycle. In the CS517x family, slope compensation is added during the entire switch on-time, typically in the amount of 180 mA/μs.

In some cases, SHM can rear its ugly head despite the presence of the onboard slope compensation. The simple cure to this problem is to add an external circuit, shown in Figure 39, to increase the amount of slope compensation used. This circuit requires only a few components and is “tacked on” to the compensation network.

The dashed box contains the normal compensation circuitry to limit the bandwidth of the error amplifier. Resistors \( R2 \) and \( R3 \) form a voltage divider off of the \( V_{SW} \) pin. In normal operation, \( V_{SW} \) looks similar to a square wave, and is dependent on the converter topology. Formulas for calculating \( V_{SW} \) in the boost and flyback topologies are given in the section “\( V_{SW} \) Voltage Limit.” The voltage on \( V_{SW} \) charges capacitor \( C3 \) when the switch is off, causing the voltage at the \( V_C \) pin to shift upwards. When the switch turns on, \( C3 \) discharges through \( R3 \), producing a negative slope at the \( V_C \) pin. This negative slope provides the slope compensation.

The amount of slope compensation added by this circuit is

\[
\frac{\Delta I}{\Delta T} = V_{SW} \left( \frac{R3}{R2 + R3} \right) \left( 1 - e^{-\frac{(1-D)}{f_{SW}}} \right) \left( \frac{f_{SW}}{(1 - D)R_E A_V} \right)
\]

where:
- \( \Delta I/\Delta T \) = the amount of slope compensation added (A/s);
- \( V_{SW} \) = the voltage at the switch node when the transistor is turned off (V);
- \( f_{SW} \) = the switching frequency, typically 280 kHz (CS5171/3) or 560 kHz (CS5172/4) (Hz);
- \( D \) = the duty cycle;
- \( R_E = 0.063 \) Ω, the value of the internal emitter resistor;
- \( A_V = 5 \) V/V, the gain of the current sense amplifier.

In selecting appropriate values for the slope compensation network, the designer is advised to choose a convenient capacitor, then select values for \( R2 \) and \( R3 \) such that the amount of slope compensation added is 100 mA/μs. Then \( R2 \) may be increased or decreased as necessary. Of course, the series combination of \( R2 \) and \( R3 \) should be large enough to avoid drawing excessive current from \( V_{SW} \). Additionally, to ensure that the control loop stability is improved, the time constant formed by the additional components should be chosen such that

\[
R_3C_3 < \frac{1 - D}{f_{SW}}
\]

Finally, it is worth mentioning that the added slope compensation is a tradeoff between duty cycle stability and transient response. The more slope compensation a designer adds, the slower the transient response will be, due to the external circuitry interfering with the proper operation of the error amplifier.

**Soft–Start**

Through the addition of an external circuit, a Soft–Start function can be added to the CS5171/2/3/4 family of components. Soft–Start circuitry prevents the \( V_C \) pin from slamming high during startup, thereby inhibiting the inductor current from rising at a high slope.
This circuit, shown in Figure 40, requires a minimum number of components and allows the Soft–Start circuitry to activate any time the SS pin is used to restart the converter.

![Figure 40. Soft Start](image)

Resistor R1 and capacitors C1 and C2 form the compensation network. At turn on, the voltage at the VC pin starts to come up, charging capacitor C3 through Schottky diode D2, clamping the voltage at the VC pin such that switching begins when VC reaches the VC threshold, typically 1.05 V (refer to graphs for detail over temperature). VC = VF(D2) + VC3

Therefore, C3 slows the startup of the circuit by limiting the voltage on the VC pin. The Soft–Start time increases with the size of C3.

Diode D1 discharges C3 when SS is low. If the shutdown function is not used with this part, the cathode of D1 should be connected to VIN.

**Calculating Junction Temperature**

To ensure safe operation of the CS5171/2/3/4, the designer must calculate the on–chip power dissipation and determine its expected junction temperature. Internal thermal protection circuitry will turn the part off once the junction temperature exceeds 180°C ± 30°C. However, repeated operation at such high temperatures will ensure a reduced operating life.

Calculation of the junction temperature is an imprecise but simple task. First, the power losses must be quantified. There are three major sources of power loss on the CS517x:

- biasing of internal control circuitry, PBIAS
- switch driver, PDRIVER
- switch saturation, PSAT

The internal control circuitry, including the oscillator and linear regulator, requires a small amount of power even when the switch is turned off. The specifications section of this datasheet reveals that the typical operating current, IQ, due to this circuitry is 5.5 mA. Additional guidance can be found in the graph of operating current vs. temperature. This graph shows that IQ is strongly dependent on input voltage, VIN, and temperature. Then

\[ P_{BIAS} = V_{IN}I_Q \]

Since the onboard switch is an NPN transistor, the base drive current must be factored in as well. This current is drawn from the VIN pin, in addition to the control circuitry current. The base drive current is listed in the specifications as \( \Delta I_{CC}/\Delta I_{SW} \) or switch transconductance. As before, the designer will find additional guidance in the graphs. With that information, the designer can calculate

\[ P_{DRIVER} = V_{IN}I_{SW} \times \frac{I_{CC}}{\Delta I_{SW}} \times D \]

where:

- \( I_{SW} \) = the current through the switch;
- \( D \) = the duty cycle or percentage of switch on–time.

\( I_{SW} \) and \( D \) are dependent on the type of converter. In a boost converter,

\[ I_{SW(AVG)} = \frac{I_{L(AVG)} \times D \times \frac{1}{\text{Efficiency}}}{V_{OUT} - V_{IN}} \]

In a flyback converter,

\[ I_{SW(AVG)} = \frac{V_{OUT}I_{LOAD} \times \frac{1}{\text{Efficiency}} \times \frac{1}{D}}{V_{IN}} \]

\[ D = \frac{V_{OUT}}{V_{OUT} + N_{NP}V_{IN}} \]

The switch saturation voltage, \( V_{(CE)SAT} \), is the last major source of on–chip power loss. \( V_{(CE)SAT} \) is the collector–emitter voltage of the internal NPN transistor when it is driven into saturation by its base drive current. The value for \( V_{(CE)SAT} \) can be obtained from the specifications or from the graphs, as “Switch Saturation Voltage.” Thus,

\[ P_{SAT} = V_{(CE)SAT}I_{SW} \times D \]

Finally, the total on–chip power losses are

\[ P_D = P_{BIAS} + P_{DRIVER} + P_{SAT} \]

Power dissipation in a semiconductor device results in the generation of heat in the junctions at the surface of the chip. This heat is transferred to the surface of the IC package, but a thermal gradient exists due to the resistive properties of the package molding compound. The magnitude of the thermal gradient is expressed in manufacturers’ data sheets as \( \theta_{JA} \), or junction–to–ambient thermal resistance. The on–chip junction temperature can be calculated if \( \theta_{JA} \), the air temperature near the surface of the IC, and the on–chip power dissipation are known.
\[ T_J = T_A + (P_{D\theta_{JA}}) \]

where:
- \( T_J \) = IC or FET junction temperature (°C);
- \( T_A \) = ambient temperature (°C);
- \( P_D \) = power dissipated by part in question (W);
- \( \theta_{JA} \) = junction-to-ambient thermal resistance (°C/W).

For the CS517x, \( \theta_{JA} = 165 \text{°C/W} \).

Once the designer has calculated \( T_J \), the question of whether the CS517x can be used in an application is settled. If \( T_J \) exceeds 150°C, the absolute maximum allowable junction temperature, the CS517x is not suitable for that application.

If \( T_J \) approaches 150°C, the designer should consider possible means of reducing the junction temperature. Perhaps another converter topology could be selected to reduce the switch current. Increasing the airflow across the surface of the chip might be considered to reduce \( T_A \).

Circuit Layout Guidelines

In any switching power supply, circuit layout is very important for proper operation. Rapidly switching currents combined with trace inductance generates voltage transitions that can cause problems. Therefore the following guidelines should be followed in the layout.

1. In boost circuits, high AC current circulates within the loop composed of the diode, output capacitor, and on–chip power transistor. The length of associated traces and leads should be kept as short as possible. In the flyback circuit, high AC current loops exist on both sides of the transformer. On the primary side, the loop consists of the input capacitor, transformer, and on–chip power transistor, while the transformer, rectifier diodes, and output capacitors form another loop on the secondary side. Just as in the boost circuit, all traces and leads containing large AC currents should be kept short.

2. Separate the low current signal grounds from the power grounds. Use single point grounding or ground plane construction for the best results.

3. Locate the voltage feedback resistors as near the IC as possible to keep the sensitive feedback wiring short. Connect feedback resistors to the low current analog ground.

![Figure 41. Additional Application Diagram, 5.0 V to −12 V/ 75 mA Inverting Converter](image-url)
Figure 42. Additional Application Diagram, 3.3 V Input, 5.0 V/400 mA Output Boost Converter

Figure 43. Additional Application Diagram, 2.7 to 13 V Input, ±12 V/200 mA Output Flyback Converter

Figure 44. Additional Application Diagram, −9.0 V to −28 V Input, −5.0 V/700 mA Output Inverted Buck Converter
Figure 45. Additional Application Diagram, 2.7 V to 28 V Input, 5.0 V Output SEPIC Converter

Figure 46. Additional Application Diagram, 4.0 V Input, 100 V/10 mA Output Boost Converter with Output Voltage Multiplier

Figure 47. Additional Application Diagram, 5.0 V Input, ±12 V Output Dual Boost Converter
## ORDERING INFORMATION

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<th>Operating Temperature Range</th>
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†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
**NOTES:**
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

**SOLDERING FOOTPRINT**

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “*”, may or may not be present. Some products may not follow the Generic Marking.

**GENERIC MARKING DIAGRAM**

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**

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**DOCUMENT NUMBER:** 98ASB42564B

**DESCRIPTION:** SOIC−8 NB

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**DESCRIPTION:**
- **SOIC–8 NB**
- **CASE 751–07**
- **ISSUE AK**

**DATE 16 FEB 2011**

**DOCUMENT NUMBER:** 98ASB42564B

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