Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

AN-9718
FXMA2102 I²C Translator

Introduction

The FXMA2102 is a high-performance voltage-level translator, or level shifter, specifically designed for I²C and SMBUS open-drain applications. It features auto-direction and can translate either side (A or B) from 1.65V to 5.5V.

The FXMA2102 has open-drain I/Os and requires external pull-up resistors on the four data I/O pins, as shown in Figure 1. If a pair of data I/O pins (A_N/B_N) is not used, both pins should be tied to GND (or both to V_{CC}). In this case, pull-down or pull-up resistors are not required. The recommended values for the pull-up resistors (R_{PU}) are 1KΩ to 10KΩ. However, depending on the total bus capacitance, the pull-up resister value can vary to meet the maximum I²C edge rate per the I²C specification (UM10204 rev. 03, June 19, 2007). For example, the maximum rise time (30% - 70%) during fast mode (400Kbit/s) is 300ns. So, if bus capacitance is approaching the maximum 400pF, lower the RPU value to keep the rise time below 300ns (Fast Mode). Section 7.1 of the I²C specification provides an excellent guideline for pull-up resistor sizing.

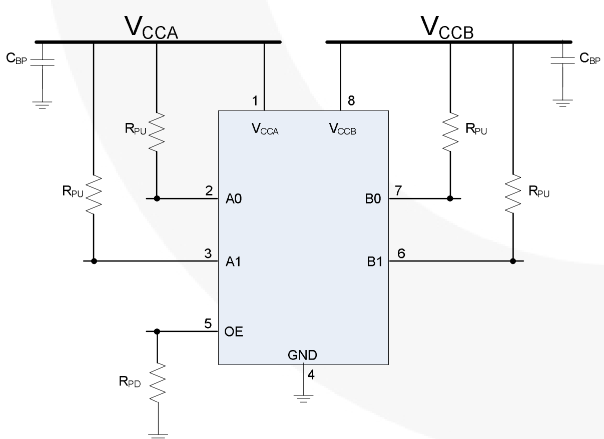

Figure 1. Application Circuit

Theory of Operation

The FXMA2102 is designed for high-performance level shifting and buffer/repeating in an I²C application. As seen in Figure 2, each bi-directional channel contains two series Npassgates and two dynamic drivers. This hybrid architecture is highly beneficial in an I²C application where auto-direction is a necessity.

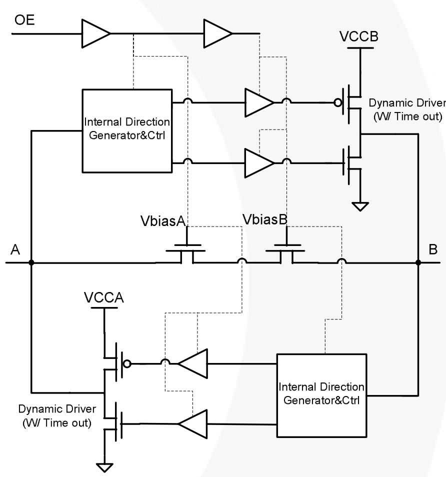

Figure 2. FXMA2102 Architecture

For example, during these three I²C protocol events:

- Clock stretching
- Slave acknowledgement: the slave's ACK bit (9th bit = 0) following a master's write bit (8th bit = 0)
- Clock synchronization and multi-master arbitration

The bus direction needs to change from master-to-slave to slave-to-master without the occurrence of an edge. If there is an I²C translator between the master and slave in these examples, the I²C translator must change direction when both A and B ports are LOW. The Npassgates can accomplish this efficiently because, when both A and B ports are LOW, the Npassgates act as a low-resistive short between the two (A and B) ports.

Due to I²C's open-drain topology, I²C masters and slaves are not push/pull drivers. Logic LOWs are pulled down (I_{sink}), while logic HIGHs are "let go" (tri-state). For example, when the master lets go of SCL (SCL always comes from the master), the rise time of SCL is largely determined by the RC time constant where R = R_{PU} and C = the bus capacitance. If the FXMA2102 is attached to the master in this example, say on the A port, and there is a slave on the B port, the Npassgates acts as a low-resistive short between both ports until either of the port's $V_{CC}/2$ thresholds are reached. After the RC time constant has reached the $V_{CC}/2$ threshold of either port, the port's edge detector triggers both dynamic drivers to drive their respective ports in the LOW-to-HIGH (LH) direction, accelerating the rising edge. The resulting rise time resembles the scope shot of Figure 3. Effectively, there are two distinct slew rates to the rise time. The first slew rate (slower) is the RC time constant of the bus. The second slew rate (much faster) is the dynamic driver accelerating the edge.

If both the A and B ports of the translator are HIGH, a high-impedance path exists between the A and B ports. This is because both the Npassgates are turned off. If a master or slave device pulls SCL or SDA LOW, that device's driver pulls down (I_{sink}) SCL or SDA until the edge reaches the A or B port $V_{CC}/2$ threshold. When either the A or B port threshold is reached, the port's edge detector triggers both dynamic drivers to drive their respective ports in the HIGH-to-LOW (HL) direction, accelerating the falling edge.

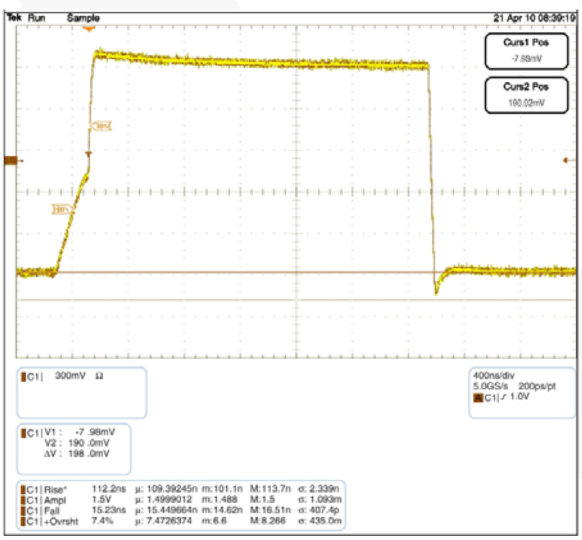

Figure 3. Waveform C: 600pF, R_{PU}: 2.2KΩ

Clock Stretching

Clock stretching allows a slave to hold SCL LOW, forcing the master to wait until the slave releases SCL. According to the I²C specification, there is not a maximum time limit for how long SCL can be held LOW by a slave; however, most masters provide a time-out algorithm during clock stretching so the I²C bus does not hang.

Clock stretching occurs in many smart-phone applications. For example, there may be an I²C master host processor that has requested the current GPS coordinates from a GPS slave. Meanwhile, the GPS device may have stored the last GPS coordinates in an internal register from a previous master request. The master does not want the previously stored GPS coordinates. The master wants real-time GPS coordinates. This means that the GPS slave device must produce the new coordinates. This effort may take milliseconds. Therefore, the GPS slave must force the master to wait until it is ready to service the request for new GPS coordinates.

The interesting aspect of clock stretching for an I²C translator application configuration like Figure 4 is that the translator's auto-direction circuitry must change direction when both sides of SCL are LOW. The FXMA2102 tested 100% compliant during I²C clock stretching.

Multi-Master

The I²C specification also describes protocol timing requirements for "clock synchronization and arbitration" when multiple I²C masters attempt to transmit on an idle I²C bus at the same time. The FXMA2102 has been tested and verified in a multi-master application.

Buffer / Repeater Performance

The FXMA2102 dynamic drivers have current sourcing capability and can drive a 400pF capacitive bus. This is beneficial when an I²C buffer/repeater is required. The I²C specification stipulates a maximum bus capacitance of 400pF. If an I²C segment exceeds 400pF, an I²C buffer/repeater is required to split the segment into two segments, each of which is less than 400pF. Figure 3 is a scope shot of an FXMA2102 driving a lumped load of 600pF. Notice the (30% - 70%) rise time is only 112ns (R_{PU} = 2.2KΩ). This is well below the maximum rise time of 300ns. So, not only does the FXMA2102 drive 400pF, but it also provides headroom below the I²C specification maximum rise time of 300ns.

V_{OL} vs. V_{IL} & I_{OL}

The I²C specification mandates a maximum V_{IL} (assuming a minimum I_{OL} of 3mA) of V_{CC}*0.3 and a maximum V_{OL} of 0.4V. If, for example (*see Figure 4*), there is a master on the A port of an I²C translator with a V_{CC} of 1.65V and a slave on the I²C translator B port with a V_{CC} of 3.3V, the maximum V_{IL} of the master is (1.65V x 0.3) 495mV.

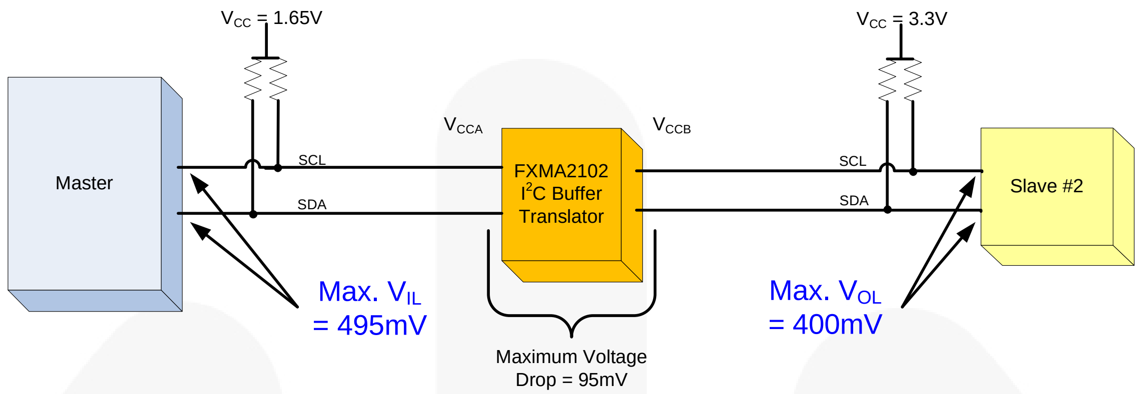

Figure 4. Clock Stretching

The slave in the Figure 4 example could legally transmit a valid logic LOW of 0.4V to the master. If the I²C translator's channel resistance is too high, the voltage drop across the translator could present a V_{IL} to master > 495mV. To complicate matters, the I²C specification states that 6mA of I_{OL} is recommended for bus capacitances approaching 400pF. More I_{OL} increases the voltage drop across the I²C translator. The I²C application benefits when I²C translators exhibit low V_{OL} performance. Figure 5 depicts the typical FXMA2102 V_{OL} performance, given a 0.4V V_{IL}.

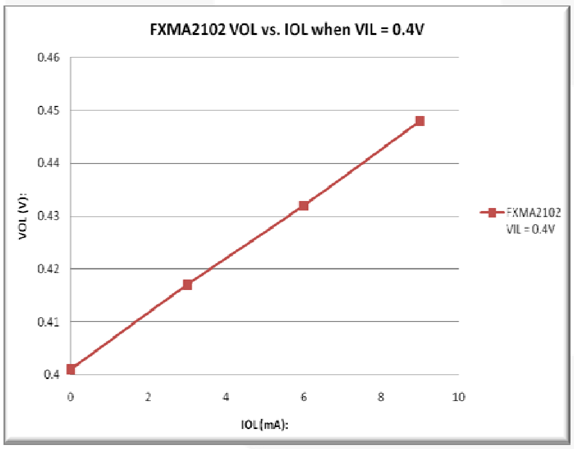

Figure 5. V_{OL} vs. I_{OL}

I²C Bus Isolation

FXMA2102 supports I²C bus isolation for these conditions:

- Bus isolation in the event of bus clear
- Bus isolation in the event of either V_{CC} going to ground.

Bus Clear

The I²C specification defines the minimum SCL frequency of 0Hz. Therefore, the SCL signal can legally be held LOW forever. However, this condition shuts down the I²C bus. The I²C specification refers to this condition as "Bus Clear." In Figure 6, if slave #2 holds down SCL forever, the master and slave #1 are not able to communicate because the FXMA2102 passes the SCL stuck-LOW condition from slave 2 to slave 1 as well as the master. However, if the OE pin of the FXMA2102 is pulled LOW (disabled), both ports (A and B) of are in tri-state. This results in the FXMA2102 isolating slave #2 from the master and slave #1, allowing full communication between master and slave #1.

Either V_{CC} to GND

If, in an application such as Figure 6, slave #2 is a camera that is suddenly removed from the I²C bus, resulting in V_{CCB} transitioning from a valid V_{CC} (1.65V – 5.5V) to 0V, the FXMA2102 automatically forces SCL and SDA on both its A and B ports into tri-state. Once V_{CCB} reaches 0V, there is full I²C communication between the master and slave #1.

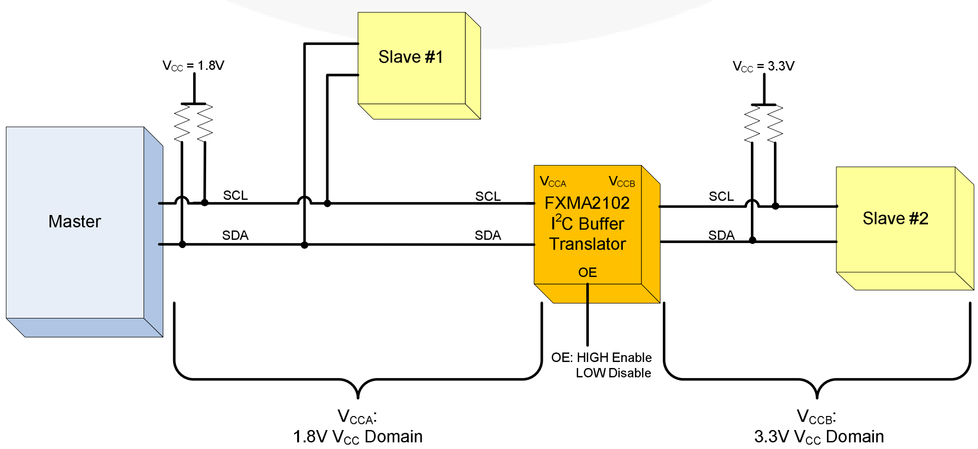

Figure 6. Bus Clear

Power-Good Voltage

Typically, if V_{CCA} or V_{CCB} are below 600mV, the I^2C signals (SDA and SCL) are tri-state on both the FXMA2102 A port and B port. OE is tied to V_{CCA}.

Typically, if V_{CCA} and V_{CCB} are above 600mV, the I^2C signals (SDA and SCL) are active on both the FXMA2102 A port and B port. OE is tied to V_{CCA}.

Parallel I^2C Voltage Segments

Smart-phone applications are driving demand for a variety of mobile IC devices like accelerometers, gyroscopes, compasses, GPS, proximity sensors, and temperature sensors. Many of these devices communicate with the mobile host processor via I^2C, while most of these devices do not share a common V_{CC}. Therefore, to maintain proper I^2C communication, the smart-phone architect must segment these individual I^2C sensors into parallel voltage segments/domains where their respective V_{CC}'s agree. Figure 7 illustrates this concept.

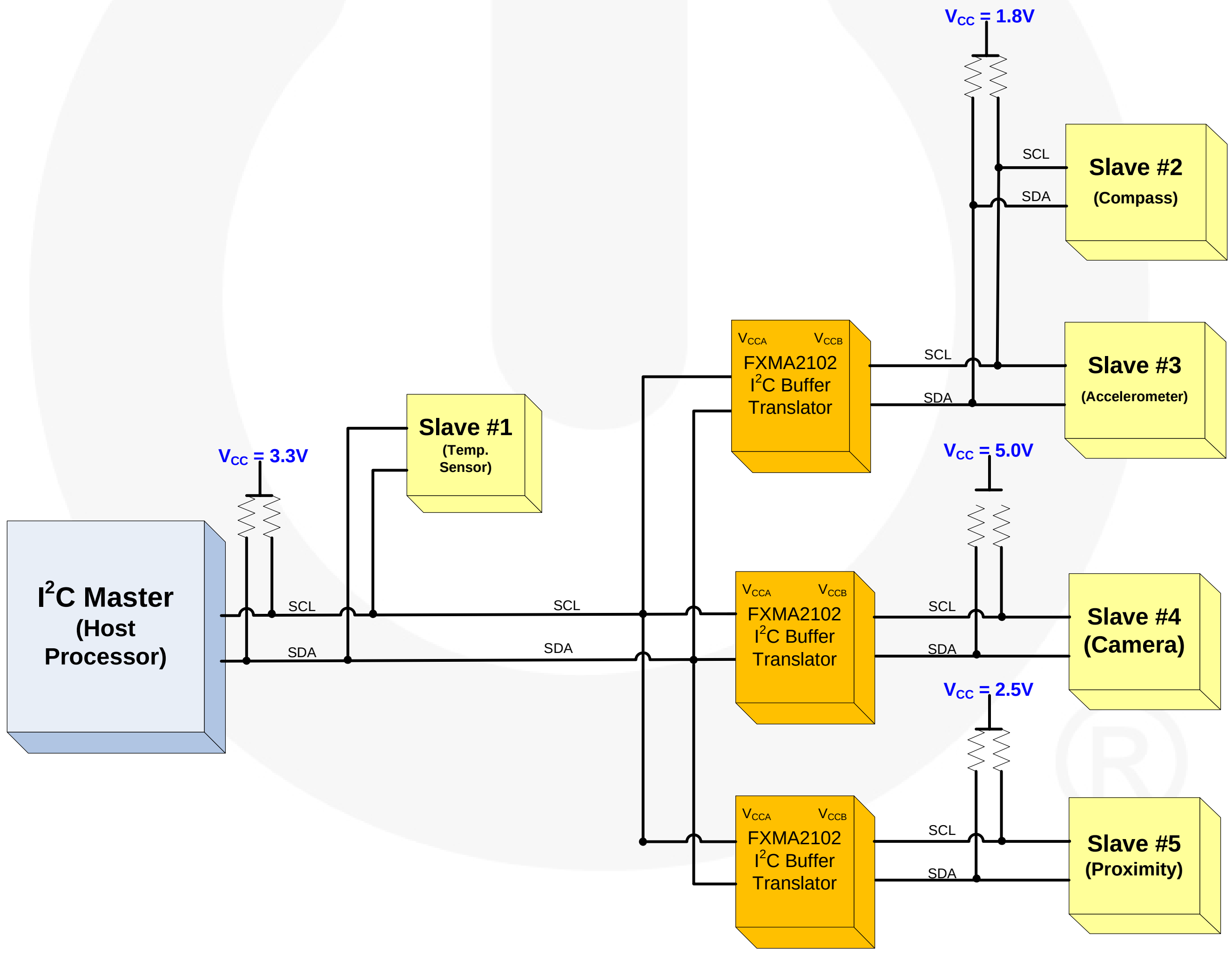

Figure 7. Three V_{CC} Domain Segments in Parallel

Figure 7 depicts a hypothetical example of I^2C V_{CC} domain segmentation typical of today's mobile smart-phone architectures. At the physical layer, multiple I^2C voltage translators are placed in parallel to resolve V_{CC} disagreement. Figure 7 illustrates three V_{CC} domain segments in parallel, each of which is electrically connected to the V_{CCB} sides of each I^2C translator.

- I^2C V_{CC} Domain Segment #1: Slave #2 and Slave #3 at 1.8V
- I^2C V_{CC} Domain Segment #2: Slave #4 at 5.0V
- I^2C V_{CC} Domain Segment #3: Slave #2 at 2.5V

Meanwhile, the I^2C master and slave #1 represent a fourth V_{CC} domain segment at 3.3V on the V_{CCA} sides of the three I^2C translators.

Related Datasheets

FXMA2102 — Dual Supply, 2-Bit Voltage Translator / Buffer / Repeater / Isolator for I^2C Applications

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative