AND9968/D

X’tal Selection and PLL Setting of LC823455 Series for Audio Applications

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APPLICATION NOTE

Introduction

This application note describes the X’tal (XT1) selection and PLL setting for desired application.

Intended audience is customers who are building audio application using LC823455 Series (called LC823455 hereafter).

BACKGROUND

LC823455 has three oscillators and two PLLs inside.

Three oscillators are RC OSC (1 MHz, typical), XTRTC OSC (32.768 kHz) and XT1 OSC (12−24 MHz). RC OSC is internal RC oscillator for initial operation after reset. XTRTC is 32.768 kHz X’tal oscillator for RTC (Real Time Clock). XT1 OSC is X’tal oscillator for main operation. BASIC clock as fundamental clock for CPU, bus system, internal memories and so on can be generated from RC, XTRTC or XT1 depending on the situation.

Two PLLs are PLL1 for BASIC clock and PLL2 for audio clock. By controlling of the register configuration for these, the suitable clocks can be generated respectively. We can provide the software stack including Middleware with Application Interface (API) to control these H/W modules without accessing to their registers directly.

LC823455 has a PLL loop filter as built−in. You can select either the internal loop filter or the external loop filter. However, in some packages of LC823455, you can only use internal loop filter.

X’tal (XT1) Selection

LC823455 contains a 2−bit terminal named XTALINFO[1:0] to set the frequency of connected XT1 outside. XTALINFO[1:0] terminal should be set in accordance with the frequency of XT1 as shown in Table 1.

Table 1. VARIATION OF AVAILABLE FREQUENCY OF XT1

XT1 Frequency [MHz]	XTALINFO[1:0]
12	“01”
19.2	“10”
24	“00”

In some packages of LC823455, XTALINFO[1:0] terminal is not prepared. It is set internally in accordance with the prescribed frequency of XT1. The frequency of XT1 other than 12, 19.2, 24 MHz may cause functional error during ROM boot, because some internal clock frequencies are determined automatically according to the XTALINFO[1:0] input and connected XT1 frequency .

Instead of using a crystal, you can use the external clock signal that is generated by some oscillation module outside of LC823455 through XIN1 terminal with unconnected XOUT terminal. However, the XT1 oscillator is supposed to be used with quartz resonator or ceramic resonator. Therefore, we have not ever evaluated the case of external clock signal input.

PLL1 Setting

The system clock configuration diagram is as shown in Figure1. The source of BASIC clock can be selected from one of four clocks, RC OSC, XTRTC OSC, XT1 OSC and PLL1.

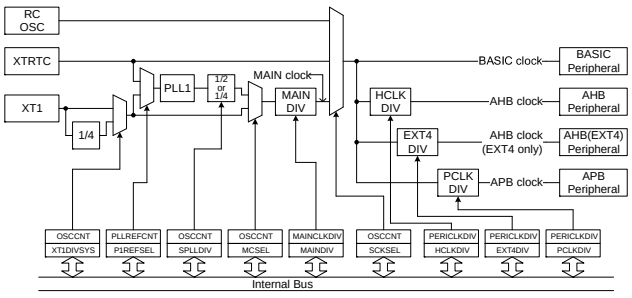

Figure 1. System Clock Configuration Diagram

Table 2 shows the relationship between XT1 frequency and Division ratio of SysPLLMDIV and SysPLLNDIV.

Table 2. XT1 SELECTION AND DIVISION RATIO

XT1 Frequency [MHz]	PLL Output Frequency [MHz]	SysPLLMDIV	SysPLLNDIV
12	100 to 400	12	100 to 400
19.2	100.8 to 399.6	16	84 to 333
24	100 to 400	24	100 to 400

The relationship of input XT1 frequency and PLL1 output frequency is as follows:

$$\text{PLL1 output frequency} = \frac{\text{Input XT1 frequency}}{\text{SysPLLMDIV}} \times \text{SysPLLNDIV}$$

Table 3 shows the characteristics of PLL1.

Table 3. PLL1 CHARACTERISTICS

Vdd1 (Note 1) = 0.95 to 1.155 V, AVddPLL1 (Note 1) = 0.95 to 1.155 V, Ta = −20°C to +65°C

Item	Symbol	Condition	Min	Typ	Max	Unit
PLL1 output frequency	Fout		100		400	MHz
Phase comparison frequency (Note 2)	Fref				10	MHz
PLL1 lock time (Note 2)	Tlock1 (Note 3)	Internal loop filter Fref = 1.0 MHz, 1.2 MHz			0.61	ms
	Tlock2 (Note 3)	External loop filter Fref = 1.0 MHz, 1.2 MHz			1.25	ms
Jitter (Note 2)	Jitter	PLL frequency = 400 MHz		±5.94	±10.1	%

1. Power up and power down timing of AVddPLL1 and Vdd1 should be as close as possible.
2. Electrical specifications are based on simulation results.
3. PLL lock time and appropriate LPF circuit depend on phase comparison frequency (Fref).

When PLL1 is selected as the BASIC clock source, there is one clock divider just after PLL1 output, then the BASIC clock is 1/2 or 1/4 of PLL1 output frequency. Table 4 shows the range of internal clock frequencies. There is a frequency limit depending on Vdd1 voltage supply, maximum clock at Vdd1 = 0.95 to 1.155 V is up to 100 MHz while one at Vdd1 = 1.05 to 1.155 V is up to 170 MHz.

Table 4. INTERNAL CLOCK FREQUENCY

Clock Frequency	Vdd1 = 0.95 to 1.155 V			Vdd1 = 1.05 to 1.155 V			Unit
	Min	Typ	Max	Min	Typ	Max	
Cortex−M3	0		115	0		170	MHz
AHB	0		115	0		170	MHz
APB	0		115	0		170	MHz
DSP	0		115	0		170	MHz

You can divide Basic clock frequency depending on each applications by another division ratio. Therefore, LC823455 can do an intermittent action of change the frequency to reduce the current consumption with appropriate frequency suitable for each applications.

PLL2 Setting

The audio clock configuration diagram is as shown in Figure 2. Normally, the audio clock uses PLL2 output clock as the clock source.

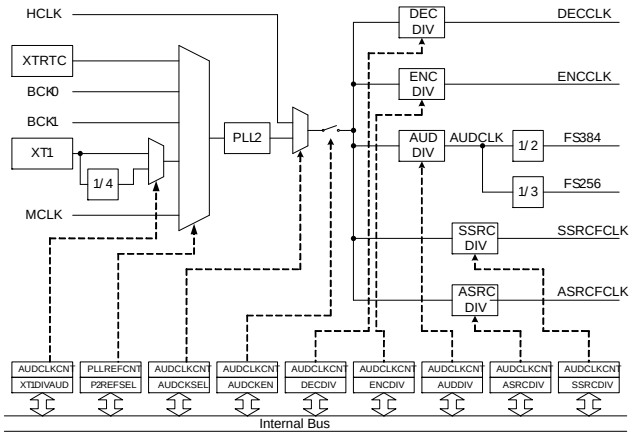

Figure 2. Audio Clock Configuration Diagram

PLL2 can generate required clock based on various sampling frequencies depending on the audio application. Table 5 shows the relationship between XT1 frequency, Fs and Division ratio of AudPLLMDIV and AudPLLNDIV.

Table 5. XT1 SELECTION AND SAMPLING FREQUENCY

PLL output frequency = 768 × Fs × n (n = 16, 8, 4, 2, and 1)

XT1 Frequency [MHz]	PLL2 Output Frequency [MHz]	Sampling Frequency Fs [kHz]	AudPLLMDIV	AudPLLNDIV
12	98.304	8 / 16 / 32 / 64 / 128	125	1024
	135.4752	11.025 / 22.05 / 44.1 / 88.2 / 176.4	625	7056
	147.456	12 / 24 / 48 / 96 / 192	125	1536
19.2	98.304	8 / 16 / 32 / 64 / 128	25	128
	135.4752	11.025 / 22.05 / 44.1 / 88.2 / 176.4	125	882
	147.456	12 / 24 / 48 / 96 / 192	25	192
24	98.304	8 / 16 / 32 / 64 / 128	125	256
	135.4752	11.025 / 22.05 / 44.1 / 88.2 / 176.4	625	1764
	147.456	12 / 24 / 48 / 96 / 192	125	768

The relationship of input XT1 frequency and PLL2 output frequency is as follows:

$$\text{PLL2 output frequency} = \frac{\text{Input XT1 frequency}}{\text{AudPLLMDIV}} \times \text{AudPLLNDIV}$$

Table 6 shows the characteristics of PLL2.

Table 6. PLL2 CHARACTERISTICS

Vdd1 (Note 4) = 0.95 to 1.155 V, AVddPLL2 (Note 4) = 0.95 to 1.155 V, Ta = −20°C to +65°C

Item	Symbol	Condition	Min	Typ	Max	Unit
PLL2 output frequency	Fout		95		150	MHz
Phase comparison frequency (Note 5)	Fref				10	MHz
PLL2 lock time	Tlock1 (Note 7)	Internal loop filter Fref = 96 KHz, 19.2 KHz, 768 KHz, 153.6 KHz, 192 KHz, 38.4 KHz			15.4	ms
	Tlock2 (Note 7)	External loop filter Fref = 96 KHz, 19.2 KHz, 768 KHz, 153.6 KHz, 192 KHz, 38.4 KHz			7.7	ms
Jitter (Note 6)	Jitter1	PLL frequency = 98.304 MHz		±2.88	±4.9	%
	Jitter2	PLL frequency = 135.4752 MHz		±3.41	±5.8	%
	Jitter3	PLL frequency = 147.456 MHz		±3.59	±6.1	%

4. Power up and power down timing of AVddPLL2 and Vdd1 should be as close as possible.
5. Electrical specifications are based on simulation results.
6. Each electrical specification is the results of simulation.
7. PLL lock time and appropriate LPF circuit depend on Phase comparison frequency (Fref).

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