AND9346/D

LC717A30
Application Note

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APPLICATION NOTE

Features

Adhesive Free, Air-gap Available

- Dielectric Materials Such as Light Guide Plates are Completely Removed
- Adhesive Process are Taken Away From the Assembly Process
- Mechanical and Electrical Components can be Mounted on Both Sides of PCB

Long Sensor Trace Available

- Long Sensor Traces Provide for a More Effective Design. The Touch Controller can be Placed Anywhere on PCB, so That PCB can be Downsized Thus Reducing Cost

Proximity Sensing Available

- Proximity detection is possible by Superior Sensitivity Technology

Wide Range Operational Temperature

- The Ambient Temperature Range is −40 to +105°C, and a Temperature Range is Wider Than General LSI

No Extra Components Necessary

- No Extra Components for Sensing, such as Resistance or Capacitance

Touch ON/OFF Judgment Possible Without a Program

- Nonvolatile Memory is not Built-in. It is Unnecessary for Developers to Develop Touch ON/OFF Determination Process

SELECTION GUIDE FOR LC717A SERIES

LC717A series are designed for the customers to use easily and introduce into their applications quickly. All necessary functions for determining ON and OFF switching are built in one chip. Customers do not need to create any software programs to determine switching. The table below shows the comparison between LC717A series.

Table 1. COMPARISON BETWEEN LC717A SERIES

Product Name	LC717A00	LC717A10	LC717A30
Sensor Channels	8 ch	16 ch	**8 ch**
Output Channels	Yes (8 ch)	No	**No**
Touch-ON Interrupt is Availability	No	Yes	**Yes**
Capable of Measuring of the Capacitance	4 pF or less	←	**Unlimited**
MPU Interface	I^2C bus / SPI	←	←
Interface Choice Method	Input an Edge Into nCS pin (Reset is Necessary for Switching)	←	**Select by IFSEL Pin**
Ambient Temperature Range	−40 to +105°C	←	←
Package	SSOP30 (225mil) VCT28	SSOP30 (225mil) VCT28	**SSOP30 (225mil) VCT28**
AEC−Q100	No	No	**Yes**
Key Features	– To Exchange Mechanical Switches – To Reduce Design Resources during Introducing Products	– More than 9 Inputs are Necessary	**– To focus proximity detection and regard sensitivity up and noise tolerance as important**

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REGISTERS

Register Address is described such as “0x00” and Register Data is described such as “00h” and “0”.

Table 2. REGISTER MAP

Register Address	R/W	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	RW	Use Channel Register	Cin7EN	Cin6EN	Cin5EN	Cin4EN	Cin3EN	Cin2EN	Cin1EN	Cin0EN
0x01	RW	Dynamic OffCal Threshold Register	DCalTHM3	DCalTHM2	DCalTHM1	DCalTHM0	DCalTHP3	DCalTHP2	DCalTHP1	DCalTHP0
0x02	RW	Cin1/0 2nd Gain Register	Gain1S3	Gain1S2	Gain1S1	Gain1S0	Gain0S3	Gain0S2	Gain0S1	Gain0S0
0x03	RW	Cin3/2 2nd Gain Register	Gain3S3	Gain3S2	Gain3S1	Gain3S0	Gain2S3	Gain2S2	Gain2S1	Gain2S0
0x04	RW	Cin5/4 2nd Gain Register	Gain5S3	Gain5S2	Gain5S1	Gain5S0	Gain4S3	Gain4S2	Gain4S1	Gain4S0
0x05	RW	Cin7/6 2nd Gain Register	Gain7S3	Gain7S2	Gain7S1	Gain7S0	Gain6S3	Gain6S2	Gain6S1	Gain6S0
0x06	RW	Cin0/4 Digital Offset Register	Doff07	Doff06	Doff05	Doff04	Doff03	Doff02	Doff01	Doff00
0x07	RW	Cin1/5 Digital Offset Register	Doff17	Doff16	Doff15	Doff14	Doff13	Doff12	Doff11	Doff10
0x08	RW	Cin2/6 Digital Offset Register	Doff27	Doff26	Doff25	Doff24	Doff23	Doff22	Doff21	Doff20
0x09	RW	Cin3/7 Digital Offset Register	Doff37	Doff36	Doff35	Doff34	Doff33	Doff32	Doff31	Doff30
0x0A	RW	Cin0 ON Threshold Register	TH0On7	TH0On6	TH0On5	TH0On4	TH0On3	TH0On2	TH0On1	TH0On0
0x0B	RW	Cin1 ON Threshold Register	TH1On7	TH1On6	TH1On5	TH1On4	TH1On3	TH1On2	TH1On1	TH1On0
0x0C	RW	Cin2 ON Threshold Register	TH2On7	TH2On6	TH2On5	TH2On4	TH2On3	TH2On2	TH2On1	TH2On0
0x0D	RW	Cin3 ON Threshold Register	TH3On7	TH3On6	TH3On5	TH3On4	TH3On3	TH3On2	TH3On1	TH3On0
0x0E	RW	Cin4 ON Threshold Register	TH4On7	TH4On6	TH4On5	TH4On4	TH4On3	TH4On2	TH4On1	TH4On0
0x0F	RW	Cin5 ON Threshold Register	TH5On7	TH5On6	TH5On5	TH5On4	TH5On3	TH5On2	TH5On1	TH5On0
0x10	RW	Cin6 ON Threshold Register	TH6On7	TH6On6	TH6On5	TH6On4	TH6On3	TH6On2	TH6On1	TH6On0
0x11	RW	Cin7 ON Threshold Register	TH7On7	TH7On6	TH7On5	TH7On4	TH7On3	TH7On2	TH7On1	TH7On0
0x12	RW	Cin0 OFF Threshold Register	TH0Off7	TH0Off6	TH0Off5	TH0Off4	TH0Off3	TH0Off2	TH0Off1	TH0Off0
0x13	RW	Cin1 OFF Threshold Register	TH1Off7	TH1Off6	TH1Off5	TH1Off4	TH1Off3	TH1Off2	TH1Off1	TH1Off0
0x14	RW	Cin2 OFF Threshold Register	TH2Off7	TH2Off6	TH2Off5	TH2Off4	TH2Off3	TH2Off2	TH2Off1	TH2Off0
0x15	RW	Cin3 OFF Threshold Register	TH3Off7	TH3Off6	TH3Off5	TH3Off4	TH3Off3	TH3Off2	TH3Off1	TH3Off0
0x16	RW	Cin4 OFF Threshold Register	TH4Off7	TH4Off6	TH4Off5	TH4Off4	TH4Off3	TH4Off2	TH4Off1	TH4Off0
0x17	RW	Cin5 OFF Threshold Register	TH5Off7	TH5Off6	TH5Off5	TH5Off4	TH5Off3	TH5Off2	TH5Off1	TH5Off0
0x18	RW	Cin6 OFF Threshold Register	TH6Off7	TH6Off6	TH6Off5	TH6Off4	TH6Off3	TH6Off2	TH6Off1	TH6Off0
0x19	RW	Cin7 OFF Threshold Register	TH7Off7	TH7Off6	TH7Off5	TH7Off4	TH7Off3	TH7Off2	TH7Off1	TH7Off0
0x1A	R	Cin0 Data Register	DATA07	DATA06	DATA05	DATA04	DATA03	DATA02	DATA01	DATA00
0x1B	R	Cin1 Data Register	DATA17	DATA16	DATA15	DATA14	DATA13	DATA12	DATA11	DATA10
0x1C	R	Cin2 Data Register	DATA27	DATA26	DATA25	DATA24	DATA23	DATA22	DATA21	DATA20
0x1D	R	Cin3 Data Register	DATA37	DATA36	DATA35	DATA34	DATA33	DATA32	DATA31	DATA30
0x1E	R	Cin4 Data Register	DATA47	DATA46	DATA45	DATA44	DATA43	DATA42	DATA41	DATA40
0x1F	R	Cin5 Data Register	DATA57	DATA56	DATA55	DATA54	DATA53	DATA52	DATA51	DATA50
0x20	R	Cin6 Data Register	DATA67	DATA66	DATA65	DATA64	DATA63	DATA62	DATA61	DATA60
0x21	R	Cin7 Data Register	DATA77	DATA76	DATA75	DATA74	DATA73	DATA72	DATA71	DATA70
0x22	RW	Cin0/4 CDAC Plus Register	CdacP07	CdacP06	CdacP05	CdacP04	CdacP03	CdacP02	CdacP01	CdacP00
0x23	RW	Cin0/4 CDAC Minus Register	CdacM07	CdacM06	CdacM05	CdacM04	CdacM03	CdacM02	CdacM01	CdacM00
0x24	RW	Cin1/5 CDAC Plus Register	CdacP17	CdacP16	CdacP15	CdacP14	CdacP13	CdacP12	CdacP11	CdacP10
0x25	RW	Cin1/5 CDAC Minus Register	CdacM17	CdacM16	CdacM15	CdacM14	CdacM13	CdacM12	CdacM11	CdacM10
0x26	RW	Cin2/6 CDAC Plus Register	CdacP27	CdacP26	CdacP25	CdacP24	CdacP23	CdacP22	CdacP21	CdacP20
0x27	RW	Cin2/6 CDAC Minus Register	CdacM27	CdacM26	CdacM25	CdacM24	CdacM23	CdacM22	CdacM21	CdacM20
0x28	RW	Cin3/7 CDAC Plus Register	CdacP37	CdacP36	CdacP35	CdacP34	CdacP33	CdacP32	CdacP31	CdacP30
0x29	RW	Cin3/7 CDAC Minus Register	CdacM37	CdacM36	CdacM35	CdacM34	CdacM33	CdacM32	CdacM31	CdacM30
0x2A	R	Result Data Register	Cin7ACT	Cin6ACT	Cin5ACT	Cin4ACT	Cin3ACT	Cin2ACT	Cin1ACT	Cin0ACT
0x2B	RW	Control 3 Register	MedMode1	MedMode0	AmpMode	CdacSel	Rsvd3	Rsvd2	Rsvd1	Rsvd0

Table 2. REGISTER MAP (continued)

Register Address	R/W	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x2C	R	Error Status Register	SYSERR	Readd6	Readd5	Readd4	Readd3	DALM1	DALM0	CALERR
0x2D	R	Error Channel Status Register	Cin7ERR	Cin6ERR	Cin5ERR	Cin4ERR	Cin3ERR	Cin2ERR	Cin1ERR	Cin0ERR
0x2E	–	Reserved area (Write prohibited)	–	–	–	–	–	–	–	–
0x2F	RW	Control 1 Register	WriteReq	Rsvd6	Rsvd5	MDtHold	IntMode	ParaCh	StaCal	Measure
0x30	RW	Average Count Register	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
0x31	RW	Filter Parameter Register	FP23	FP22	FP21	FP20	FP13	FP12	FP11	FP10
0x32	RW	Debounce Count 1 Register	DCT17	DCT16	DCT15	DCT14	DCT13	DCT12	DCT11	DCT10
0x33	RW	Debounce Count 2 Register	DCT27	DCT26	DCT25	DCT24	DCT23	DCT22	DCT21	DCT20
0x34	RW	Short Interval Time Register	SIVAL7	SIVAL6	SIVAL5	SIVAL4	SIVAL3	SIVAL2	SIVAL1	SIVAL0
0x35	RW	Long Interval Time Register	LIVAL7	LIVAL6	LIVAL5	LIVAL4	LIVAL3	LIVAL2	LIVAL1	LIVAL0
0x36	RW	Short Interval Dynamic OffCal Cycle Register	DCYC7	DCYC6	DCYC5	DCYC4	DCYC3	DCYC2	DCYC1	DCYC0
0x37	RW	Dynamic OffCal Count Plus Register	DCALP7	DCALP6	DCALP5	DCALP4	DCALP3	DCALP2	DCALP1	DCALP0
0x38	RW	Dynamic OffCal Count Minus Register	DCALM7	DCALM6	DCALM5	DCALM4	DCALM3	DCALM2	DCALM1	DCALM0
0x39	RW	Static OffCal CDAC Base Register	DACB7	DACB6	DACB5	DACB4	DACB3	DACB2	DACB1	DACB0
0x3A	RW	Measurement Mode 1 Register	INTMD1	INTMD2	PDCLP	DmCyc	LIVALB	MCIN1	MCIN0	Rsvd0
0x3B	RW	Measurement Mode 2 Register	CDRVB	CADD4EN	CADD0EN	CIN4CINP2	CIN0CINP2	CIN4CINP	CIN0CINP	Rsvd0
0x3C	RW	Long Interval Mode Start Count Register	LIMSC7	LIMSC6	LIMSC5	LIMSC4	LIMSC3	LIMSC2	LIMSC1	LIMSC0
0x3D	RW	Cin 1st Gain Adjust Register	Gain4F3	Gain4F2	Gain4F1	Gain4F0	Gain0F3	Gain0F2	Gain0F1	Gain0F0
0x3E	–	Reserved area (Write prohibited)	–	–	–	–	–	–	–	–
0x3F	–	Reserved area (Write prohibited)	–	–	–	–	–	–	–	–
0x40	RW	Control 2 Register	SoftRst	Rsvd6	Rsvd5	Rsvd4	Rsvd3	DyCalAck	IntOut	WakeUp
0x41 to 0x7E	–	Reserved area (Write prohibited)	–	–	–	–	–	–	–	–
0x7F	R	SLAVE Address Register	Rsvd7	Slave6	Slave5	Slave4	Slave3	Slave2	Slave1	SA0
0x80 to 0xFF	–	Reserved area (Write prohibited)	–	–	–	–	–	–	–	–

NOTE: If you read a register in the reserved area, the value is not guaranteed.

Register State at the Time of the Reset

Table 3. REGISTER STATE AT THE TIME OF THE RESET

Register Address	Reset Value	Name	Register State at the Time of the Reset
0x00	FFh	Use Channel Register	• Used from Cin0 to Cin7
0x01	C4h	Dynamic OffCal Threshold Register	• The plus side's threshold AD level for dynamic offset calibration operation is 4 • The minus side's threshold AD level for dynamic offset calibration operation is −4
0x02	44h	Cin1/0 2nd Gain Register	• The 2nd AMP gain level of Cin0 is 5 • The 2nd AMP gain level of Cin1 is 5
0x03	44h	Cin3/2 2nd Gain Register	• The 2nd AMP gain level of Cin2 is 5 • The 2nd AMP gain level of Cin3 is 5
0x04	44h	Cin5/4 2nd Gain Register	• The 2nd AMP gain level of Cin4 is 5 • The 2nd AMP gain level of Cin5 is 5
0x05	44h	Cin7/6 2nd Gain Register	• The 2nd AMP gain level of Cin6 is 5 • The 2nd AMP gain level of Cin7 is 5
0x06	00h	Cin0/4 Digital Offset Register	• The digital offset value of Cin0
0x07	00h	Cin1/5 Digital Offset Register	• The digital offset value of Cin1
0x08	00h	Cin2/6 Digital Offset Register	• The digital offset value of Cin2
0x09	00h	Cin3/7 Digital Offset Register	• The digital offset value of Cin3
0x0A	0Ah	Cin0 ON Threshold Register	• The Touch ON threshold level of Cin0 is 10
0x0B	0Ah	Cin1 ON Threshold Register	• The Touch ON threshold level of Cin1 is 10
0x0C	0Ah	Cin2 ON Threshold Register	• The Touch ON threshold level of Cin2 is 10
0x0D	0Ah	Cin3 ON Threshold Register	• The Touch ON threshold level of Cin3 is 10
0x0E	0Ah	Cin4 ON Threshold Register	• The Touch ON threshold level of Cin4 is 10
0x0F	0Ah	Cin5 ON Threshold Register	• The Touch ON threshold level of Cin5 is 10
0x10	0Ah	Cin6 ON Threshold Register	• The Touch ON threshold level of Cin6 is 10
0x11	0Ah	Cin7 ON Threshold Register	• The Touch ON threshold level of Cin7 is 10
0x12	07h	Cin0 OFF Threshold Register	• The Touch OFF threshold level of Cin0 is 7
0x13	07h	Cin1 OFF Threshold Register	• The Touch OFF threshold level of Cin1 is 7
0x14	07h	Cin2 OFF Threshold Register	• The Touch OFF threshold level of Cin2 is 7
0x15	07h	Cin3 OFF Threshold Register	• The Touch OFF threshold level of Cin3 is 7
0x16	07h	Cin4 OFF Threshold Register	• The Touch OFF threshold level of Cin4 is 7
0x17	07h	Cin5 OFF Threshold Register	• The Touch OFF threshold level of Cin5 is 7
0x18	07h	Cin6 OFF Threshold Register	• The Touch OFF threshold level of Cin6 is 7
0x19	07h	Cin7 OFF Threshold Register	• The Touch OFF threshold level of Cin7 is 7
0x1A	00h	Cin0 Data Register	• The measurement data AD level of Cin0
0x1B	00h	Cin1 Data Register	• The measurement data AD level of Cin1
0x1C	00h	Cin2 Data Register	• The measurement data AD level of Cin2
0x1D	00h	Cin3 Data Register	• The measurement data AD level of Cin3
0x1E	00h	Cin4 Data Register	• The measurement data AD level of Cin4
0x1F	00h	Cin5 Data Register	• The measurement data AD level of Cin5
0x20	00h	Cin6 Data Register	• The measurement data AD level of Cin6
0x21	00h	Cin7 Data Register	• The measurement data AD level of Cin7
0x22	00h	Cin0/4 CDAC Plus Register	• The offset plus side's capacitor "CdacP" value of Cin0

Table 3. REGISTER STATE AT THE TIME OF THE RESET (continued)

Register Address	Reset Value	Name	Register State at the Time of the Reset
0x23	00h	Cin0/4 CDAC Minus Register	• The offset minus side's capacitor "CdacM" value of Cin0
0x24	00h	Cin1/5 CDAC Plus Register	• The offset plus side's capacitor "CdacP" value of Cin1
0x25	00h	Cin1/5 CDAC Minus Register	• The offset minus side's capacitor "CdacM" value of Cin1
0x26	00h	Cin2/6 CDAC Plus Register	• The offset plus side's capacitor "CdacP" value of Cin2
0x27	00h	Cin2/6 CDAC Minus Register	• The offset minus side's capacitor "CdacM" value of Cin2
0x28	00h	Cin3/7 CDAC Plus Register	• The offset plus side's capacitor "CdacP" value of Cin3
0x29	00h	Cin3/7 CDAC Minus Register	• The offset minus side's capacitor "CdacM" value of Cin3
0x2A	00h	Result Data Register	• The touch ON/OFF judgment results from Cin0 to Cin7 are OFF
0x2B	80h	Control 3 Register	• MedMode1,0 = "1,0": Filter processing enable • AmpMode = "0": Measurement with the differential mode • CdacSel = "0": Enabled to read and write the CdacP value, CdacM value, and the digital offset value of Cin0 to Cin3
0x2C	00h	Error Status Register	• SYSERR = "0": System error clears • DALM1,0 = "0,0": Abnormality alarm level of AD level is "0" • CALERR = "0": Calibration error clears
0x2D	00h	Error Channel Status Register	• There aren't error channels
0x2F	0Bh	Control 1 Register	• WriteReq = "0": Not reflect setting • IntMode = "1": Operation in interval mode • ParaCh = "0": Not request for changing parameters • StaCal = "1": Static offset calibration is requested • Measure = "1": Measurement
0x30	40h	Average Count Register	• Average counts of measurement data are 64
0x31	02h	Filter Parameter Register	• Filter parameter 2 value is "0h" • Filter parameter 1 value is "2h"
0x32	01h	Debounce Count 1 Register	• The number of debounce count from OFF to ON is 2
0x33	01h	Debounce Count 2 Register	• The number of debounce count from ON to OFF is 2
0x34	05h	Short Interval Time Register	• Short interval time is 5 ms (Typ)
0x35	01h	Long Interval Time Register	• Long interval time is 101 ms (Typ)
0x36	03h	Short Interval Dynamic OffCal Cycle Register	• In the short interval mode, the cycle to judge whether or not to operate dynamic offset calibration is set once by 3 measurements
0x37	03h	Dynamic OffCal Count Plus Register	• The number of constant judgement to operate the plus side's dynamic offset calibration is 24
0x38	03h	Dynamic OffCal Count Minus Register	• The number of constant judgement to operate the minus side's dynamic offset calibration is 3
0x39	80h	Static OffCal CDAC Base Register	• In the static offset calibration, the reference capacitor is set 4 pF
0x3A	00h	Measurement Mode 1 Register	• INTMD1 = "0": INTOUT is asserted after each measurement • INTMD2 = "0": INTOUT is not negated automatically • PDCLP = "0": When the measurement results of all channels are less than the touch ON threshold or equal it, the judgement of the dynamic offset calibration is run • DmCyc = "0": The dummy cycle counts are 4 • LIVALB = "0": The base time of long interval is 100 ms • MCIN1,0 = "0,0": The status of channel not to measure during measurement is low level

Table 3. REGISTER STATE AT THE TIME OF THE RESET (continued)

Register Address	Reset Value	Name	Register State at the Time of the Reset
0x3B	00h	Measurement Mode 2 Register	• CdrvBar output pin: High impedance state • In the measurement from Cin4 to Cin7, CMAdd4 pin isn't used • In the measurement from Cin0 to Cin3, CMAdd0 pin isn't used • In the measurement from Cin4 to Cin7, the plus input of 1st AMP is only Cref • In the measurement from Cin0 to Cin3, the plus input of 1st AMP is only Cref
0x3C	05h	Long Interval Mode Start Count Register	• The counts until shifting to long interval mode are 20
0x3D	00h	Cin 1st Gain Adjust Register	• The 1st AMP gain level of Cin0 to Cin3 is 1600 fF (Minimum gain) • The 1st AMP gain level of Cin4 to Cin7 is 1600 fF (Minimum gain)
0x40	00h	Control 2 Register	• SoftRst = "0": Normal operation. • DyCalAck = "0": The operation flag of the dynamic offset calibration isn't shown • IntOut = "0": INTOUT is negated ("Low") • WakeUp = "0": Normal operation
0x7F	16h/17h	SLAVE Address Register	• The 7bit slave address is "16h" or "17h"

Details of Registers

- Use Channel Register

Address 0x00	Bit	7	6	5	4	3	2	1	0
	Name	Cin7EN	Cin6EN	Cin5EN	Cin4EN	Cin3EN	Cin2EN	Cin1EN	Cin0EN
	Reset	1	1	1	1	1	1	1	1
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

This register is used to enable/disable each channel. The Cin0EN bit (Bit 0) is used to enable or disable Cin0, and the Cin7EN bit (Bit 7) is used to enable or disable Cin7.

CinXEN (X = 0 to 7)
0: Disable the channel.
1: Enable the channel. (Initial value)

- Dynamic OffCal Threshold Register

Address 0x01	Bit	7	6	5	4	3	2	1	0
	Name	DCalTHM3	DCalTHM2	DCalTHM1	DCalTHM0	DCalTHP3	DCalTHP2	DCalTHP1	DCalTHP0
	Reset	1	1	0	0	0	1	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

This register is used to dynamic offset calibration operating range (Threshold level).

DCalTHM0 to DCalTHM3

These bits set the upper limit AD level of the minus level side of the dynamic offset calibration operating range. The initial value is “Ch” showing “−4”. When the measurement data under the constant number of times continues in the minus level side of the dynamic offset calibration operating range (from −128 to upper limit AD level of minus level side), this LSI automatically carries out dynamic offset calibration. In addition, this LSI does not carry out the dynamic offset calibration of minus level side when these bits set to 0h. For more information about dynamic offset calibration, refer to “Explanation of the Dynamic Offset Calibration”.

DCalTHM3	DCalTHM2	DCalTHM1	DCalTHM0	The Upper Limit AD Level of the Minus Level Side of the Dynamic Offset Calibration Operating Range
0	0	0	0	Don’t carry out the dynamic offset calibration of minus level side
1	1	1	1	−1
1	1	1	0	−2
1	1	0	1	−3
1	1	0	0	−4 (Initial value)
. . .	. . .	. . .	. . .	. . .
0	0	1	0	−14
0	0	0	1	−15

DCalTHP0 to DCalTHP3

These bits set the lower limit AD level of the plus level side of the dynamic offset calibration operating range. The initial value is “4h” showing “4”.

This LSI performs judgment processing of the dynamic offset calibration enforcement in the following cases by the PDCLP bit in the Measurement Mode Register [Address=0x3A] is set.

Case1: When the PDCLP bit is set to “0” and all channels are touch OFF states (OFF detection of all channels), this LSI carries out judgment processing.

Case2: When the PDCLP bit is set to “1”, this LSI carries out judgment processing for a channel of touch OFF state because dynamic offset calibration is determined and performed at each individual enabled channel.

When the measurement data of the judgment processing under the constant number of times continues in the plus level side of the dynamic offset calibration operating range (from the lower limit AD level of plus level side to the threshold level of touch ON), this LSI automatically carries out dynamic offset calibration under the following. In addition, this LSI doesn’t carry out the dynamic offset calibration of plus level side when these bits set to 0h.

If measurement data more than the touch ON threshold are even once, this LSI does operate the dynamic offset calibration when the measurement data at the time of the judgment processing entered the dynamic offset calibration operating range of the plus level side for the number of times of the debounce count of the Debounce Count 2 Register [Address=0x33] and lasted the number of times of the Dynamic OffCal Count Plus Register [Address= 0x36].

Application has to keep the condition of

“Lower limit AD level of plus level side (DcalTHP0 to DcalTHP3) < Threshold of touch ON”.

For more information about dynamic offset calibration, refer to “Explanation of the Dynamic Offset Calibration”.

DCalTHP3	DCalTHP2	DCalTHP1	DCalTHP0	The Lower Limit AD Level of the Plus Level Side of the Dynamic Offset Calibration Operating Range
0	0	0	0	Don’t carry out the dynamic offset calibration of plus level side.
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4 (Initial value)
. . .	. . .	. . .	. . .	. . .
1	1	1	0	14
1	1	1	1	15

- Cin1/0 2nd Gain Register

Address 0x02	Bit	7	6	5	4	3	2	1	0
	Name	Gain1S3	Gain1S2	Gain1S1	Gain1S0	Gain0S3	Gain0S2	Gain0S1	Gain0S0
	Reset	0	1	0	0	0	1	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

In this LSI, there is a two-stage amplifier that detects changes in the capacitance and outputs an analog signal corresponding to the changes. The two stage amplifier consists of 1st-amplifier and 2nd-amplifier. This register is used to specify the 2nd-amplifier gain and to adjust sensitivity of Cin0 and Cin1. Specify the gain of Cin0 with the lower 4bits of the Cin1/0 2nd Gain Register. Specify the gain of Cin1 with the upper 4bits of the Cin1/0 2nd Gain Register. The gain of 1st-amplifier is specified with the Cin 1st Gain Adjust Register [Address=0x3D].

Gain1S0 to 3: This field is used to specify the 2nd-amplifier gain for Cin1 by the upper 4bits. (The initial value is “4h” showing “5 times”.)

Gain0S0 to 3: This field is used to specify the 2nd-amplifier gain for Cin0 by the lower 4bits. (The initial value is “4h” showing “5 times”.)

The 2nd-amplifier gain setting

Gain0S3 Gain1S3	Gain0S2 Gain1S2	Gain0S1 Gain1S1	Gain0S0 Gain1S0	2nd-amplifier Gain ga2 [times]
0	0	0	0	1 (Minimum gain setting)
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5 (Initial value)
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16 (Maximum gain setting)

<Approximate Calculation Formula of the Amplifier Output Voltage>

Output voltage of 1st and 2nd in the two-stage amplifier

Output voltage of the 1st-amplifier: $\Delta V_1 = (\Delta C/Cf) \times V_{CDRV}$ $\Delta V_1 < 0.8 \times V_{DD}$

Output voltage of the 2nd-amplifier: $\Delta V_2 = \Delta V_1 \times ga2$ $\Delta V_2 < 0.8 \times V_{DD}$

ΔC : Change in input capacitance (Capacitance change when touch)

Cf : The 1st-amplifier gain setting (Feedback capacitance in the LSI)

V_{CDRV} : High output voltage of Cdrv (=V_{DD})

ga2 : The 2nd-amplifier gain setting (times)

- Cin3/2 2nd Gain Register

Address 0x03	Bit	7	6	5	4	3	2	1	0
	Name	Gain3S3	Gain3S2	Gain3S1	Gain3S0	Gain2S3	Gain2S2	Gain2S1	Gain2S0
	Reset	0	1	0	0	0	1	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

This register is used to specify the 2nd-amplifier gain and to adjust sensitivity of Cin2 and Cin3. Specify the gain of Cin2 with the lower 4bits of the Cin3/2 2nd Gain Register. Specify the gain of Cin3 with the upper 4bits of the Cin3/2 2nd Gain Register.

Gain3S0 to 3: This field is used to specify the 2nd-amplifier gain for Cin3 by the upper 4bits. (The initial value is “4h” showing “5 times”)

Gain2S0 to 3: This field is used to specify the 2nd-amplifier gain for Cin2 by the lower 4bits. (The initial value is “4h” showing “5 times”)

- Cin5/4 2nd Gain Register

Address 0x04	Bit	7	6	5	4	3	2	1	0
	Name	Gain5S3	Gain5S2	Gain5S1	Gain5S0	Gain4S3	Gain4S2	Gain4S1	Gain4S0
	Reset	0	1	0	0	0	1	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

This register is used to specify the 2nd-amplifier gain and to adjust sensitivity of Cin4 and Cin5. Specify the gain of Cin4 with the lower 4bits of "Cin5/4 2nd Gain Register". Specify the gain of Cin5 with the upper 4bits of "Cin5/4 2nd Gain Register".

Gain5S0 to 3: This field is used to specify the 2nd-amplifier gain for Cin5 by the upper 4bits. (The initial value is "4h" showing "5 times")

Gain4S0 to 3: This field is used to specify the 2nd-amplifier gain for Cin4 by the lower 4bits. (The initial value is "4h" showing "5 times")

- Cin7/6 2nd Gain Register

Address 0x05	Bit	7	6	5	4	3	2	1	0
	Name	Gain7S3	Gain7S2	Gain7S1	Gain7S0	Gain6S3	Gain6S2	Gain6S1	Gain6S0
	Reset	0	1	0	0	0	1	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

This register is used to specify the 2nd-amplifier gain and to adjust sensitivity of Cin6 and Cin7. Specify the gain of Cin6 with the lower 4bits of "Cin7/6 2nd Gain Register". Specify the gain of Cin7 with the upper 4bits of "Cin7/6 2nd Gain Register".

Gain7S0 to 3: This field is used to specify the 2nd-amplifier gain for Cin7 by the upper 4bits. (The initial value is "4h" showing "5 times")

Gain6S0 to 3: This field is used to specify the 2nd-amplifier gain for Cin6 by the lower 4bits. (The initial value is "4h" showing "5 times")

- Cin0/4 Digital Offset Register

Address 0x06	Bit	7	6	5	4	3	2	1	0
	Name	Doff07	Doff06	Doff05	Doff04	Doff03	Doff02	Doff01	Doff00
	Reset	0	0	0	0	0	0	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

- Cin1/5 Digital Offset Register

Address 0x07	Bit	7	6	5	4	3	2	1	0
	Name	Doff17	Doff16	Doff15	Doff14	Doff13	Doff12	Doff11	Doff10
	Reset	0	0	0	0	0	0	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

- Cin2/6 Digital Offset Register

Address 0x08	Bit	7	6	5	4	3	2	1	0
	Name	Doff27	Doff26	Doff25	Doff24	Doff23	Doff22	Doff21	Doff20
	Reset	0	0	0	0	0	0	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

- Cin3/7 Digital Offset Register

Address 0x09	Bit	7	6	5	4	3	2	1	0
	Name	Doff37	Doff36	Doff35	Doff34	Doff33	Doff32	Doff31	Doff30
	Reset	0	0	0	0	0	0	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

These registers store digital offset values of Cin0−Cin3 or Cin4−Cin7 which is adjusted by the offset calibration operation. The microcontroller can read and write data for these registers. The stored values are expressed by 2 complement number form such as between −128=80h, 0=00h and 127=7Fh.

The target channel of data stored to the registers are specified either Cin0−Cin3 or Cin4−Cin7 by the CdacSel bit in the Control 3 Register [Address=0x2B]. For example, about the Cin0/4 Digital Offset Register [Address=0x06]. When the CdacSel bit is “0”, the microcontroller can read and write the digital offset values of Cin0. When the CdacSel bit is “1”, the microcontroller can read and write the digital offset values of Cin4.

When the value of the digital offset registers written with the microcontroller, the microcontroller enforces changing parameters processing by the ParaCh bit in the Control 1 Register [Address=0x2F] is set to “1”, and reflected inside the LC717A30 by changing parameters, the following processing changes. In addition, after having changed the target channels by the CdacSel bit, the value of new digital offset reflects it to registers when the measurement processing is completed.

For more information, refer to “In the Case of Reading and Writing of the CdacP/CdacM/DigitalOffset Registers” in this document.

- CinX ON Threshold Register (X = 0 to 7)

Address 0x0A to 0x11	Bit	7	6	5	4	3	2	1	0
	Name	THXOn7	THXOn6	THXOn5	THXOn4	THXOn3	THXOn2	THXOn1	THXOn0
	Reset	0	0	0	0	1	0	1	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

These register are used to set a threshold (0 to 127) to judge touch ON from measurement data of each channel. Specify the threshold of Cin0 by the Cin0 ON Threshold Register [Address=0x0A], and specify the threshold of Cin7 by the Cin7 ON Threshold Register [Address=0x11].

The threshold for touch ON judgment has to be changed when changing gain setting. In addition, refer to the description of the Cin0 to Cin7 OFF Threshold Register [Address=0x12 to 0x19] about the threshold for touch OFF judgement.

Only a positive value can be set. (The TH7On7 bit is fixed to “0”. Setting the TH7On7 bit to “1” is prohibited.)

The initial value of threshold is “0Ah” showing “10”.

THXOn7	THXOn6	THXOn5	THXOn4	THXOn3	THXOn2	THXOn1	THXOn0	Touch ON Threshold
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
0	0	0	0	1	0	1	0	10 (Initial value)
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
0	1	1	1	1	1	1	0	126
0	1	1	1	1	1	1	1	127
1	0	0	0	0	0	0	0	Prohibited setting
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	1	1	1	1	1	Prohibited setting

- CinX OFF Threshold Register (X = 0 to 7)

Address 0x12 to 0x19	Bit	7	6	5	4	3	2	1	0
	Name	THXOff7	THXOff6	THXOff5	THXOff4	THXOff3	THXOff2	THXOff1	THXOff0
	Reset	0	0	0	0	0	1	1	1
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

These register are used to set a threshold (0 to 127) to judge touch OFF from measurement data of each channel. Specify the threshold of Cin0 by the Cin0 OFF Threshold Register [Address=0x12], and specify the threshold of Cin7 by the Cin7 OFF Threshold Register [Address=0x19].

The threshold for touch OFF judgment has to be changed when changing gain setting. In addition, refer to the description of the CinX ON Threshold Register [Address=0x0A to 0x11] about the threshold for touch ON judgement.

Only a positive value can be set. (The TH7Off7 bit is fixed to “0”. Setting the TH7Off7 bit to “1” is prohibited.)

The initial value of threshold is “07h” showing “7”.

THXOff7	THXOff6	THXOff5	THXOff4	THXOff3	THXOff2	THXOff1	THXOff0	Touch OFF Threshold
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
0	0	0	0	0	1	1	1	7 (Initial value)
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
0	1	1	1	1	1	1	0	126
0	1	1	1	1	1	1	1	127
1	0	0	0	0	0	0	0	Prohibited setting
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	1	1	1	1	1	Prohibited setting

- CinX Data Register (X = 0 to 7)

Address 0x1A to 0x21	Bit	7	6	5	4	3	2	1	0
	Name	DATAX7	DATAX6	DATAX5	DATAX4	DATAX3	DATAX2	DATAX1	DATAX0
	Reset	0	0	0	0	0	0	0	0
	R/W	R	R	R	R	R	R	R	R

These register are used to read out the measurement data obtained through each channel (−128 to 0 to 127). The stored data is in 2's complement form (−128=80h to 0=0h to 127=7Fh). The measurement data of Cin0 is stored in the Cin0 Data Register [Address=0x1A] and the measurement data of Cin7 is stored in the Cin7 Data Register [Address=0x21].

This measurement data is used to judge the touch "ON/OFF" status in the microcontroller.

DATAX7	DATAX6	DATAX5	DATAX4	DATAX3	DATAX2	DATAX1	DATAX0	Measurement Data
1	0	0	0	0	0	0	0	−128
1	0	0	0	0	0	0	1	−127
1	0	0	0	0	0	1	0	−126
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	1	1	1	0	1	−3
1	1	1	1	1	1	1	0	−2
1	1	1	1	1	1	1	1	−1
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
0	1	1	1	1	1	1	0	126
0	1	1	1	1	1	1	1	127

- Cin0/4 CDAC Plus Register

Address 0x22	Bit	7	6	5	4	3	2	1	0
	Name	CdacP07	CdacP06	CdacP05	CdacP04	CdacP03	CdacP02	CdacP01	CdacP00
	Reset	1	0	0	0	0	0	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

- Cin1/5 CDAC Plus Register

Address 0x24	Bit	7	6	5	4	3	2	1	0
	Name	CdacP17	CdacP16	CdacP15	CdacP14	CdacP13	CdacP12	CdacP11	CdacP10
	Reset	1	0	0	0	0	0	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

- Cin2/6 CDAC Plus Register

Address 0x26	Bit	7	6	5	4	3	2	1	0
	Name	CdacP27	CdacP26	CdacP25	CdacP24	CdacP23	CdacP22	CdacP21	CdacP20
	Reset	1	0	0	0	0	0	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

- Cin3/7 CDAC Plus Register

Address 0x28	Bit	7	6	5	4	3	2	1	0
	Name	CdacP37	CdacP36	CdacP35	CdacP34	CdacP33	CdacP32	CdacP31	CdacP30
	Reset	1	0	0	0	0	0	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

These registers store CDAC Plus values of Cin0−Cin3 or Cin4−Cin7 which is adjusted by the offset calibration operation. The microcontroller can read and write data for these registers. The stored values are expressed by 8bit form between 00h to FFh.

The target channel of data stored to the registers are specified either Cin0−Cin3 or Cin4−Cin7 by the CdacSel bit in the Control 3 Register [Address=0x2B]. For example, about the Cin0/4 CDAC Plus Register [Address=0x22]. When the CdacSel bit is “0”, the microcontroller can read and write the CDAC Plus values of Cin0. When the CdacSel bit is “1”, the microcontroller can read and write the CDAC Plus values of Cin4.

When the value of the CDAC plus registers written with the microcontroller, the microcontroller enforces changing parameters processing by the ParaCh bit in the Control 1 Register [Address= 0x2F] is set to “1”, and reflected inside the LC717A30 by changing parameters, the following processing changes. In addition, after having changed the target channels by the CdacSel bit, the value of new CDAC plus reflects it to registers when the measurement processing is completed.

For more information, refer to “In the Case of Reading and Writing of the CdacP/CdacM/DigitalOffset Registers” in this document.

- Cin0/4 CDAC Minus Register

Address 0x23	Bit	7	6	5	4	3	2	1	0
	Name	CdacM07	CdacM06	CdacM05	CdacM04	CdacM03	CdacM02	CdacM01	CdacM00
	Reset	1	0	0	0	0	0	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

- Cin1/5 CDAC Minus Register

Address 0x25	Bit	7	6	5	4	3	2	1	0
	Name	CdacM17	CdacM16	CdacM15	CdacM14	CdacM13	CdacM12	CdacM11	CdacM10
	Reset	1	0	0	0	0	0	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

- Cin2/6 CDAC Minus Register

Address 0x27	Bit	7	6	5	4	3	2	1	0
	Name	CdacM27	CdacM26	CdacM25	CdacM24	CdacM23	CdacM22	CdacM21	CdacM20
	Reset	1	0	0	0	0	0	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

- Cin3/7 CDAC Minus Register

Address 0x29	Bit	7	6	5	4	3	2	1	0
	Name	CdacM37	CdacM36	CdacM35	CdacM34	CdacM33	CdacM32	CdacM31	CdacM30
	Reset	1	0	0	0	0	0	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

These registers store CDAC Minus values of Cin0−Cin3 or Cin4−Cin7 which is adjusted by the offset calibration operation. The microcontroller can read and write data for these registers. The stored values are expressed by 8bit form between 00h to FFh.

The target channel of data stored to the registers are specified either Cin0−Cin3 or Cin4−Cin7 by the CdacSel bit in the Control 3 Register [Address=0x2B]. For example, about the Cin0/4 CDAC Minus Register [Address=0x23]. When the CdacSel bit is “0”, the microcontroller can read and write the CDAC Minus values of Cin0. When the CdacSel bit is “1”, the microcontroller can read and write the CDAC Minus values of Cin4.

When the value of the CDAC minus registers written with the microcontroller, the microcontroller enforces changing parameters processing by the ParaCh bit in the Control 1 Register [Address= 0x2F] is set to “1”, and reflected inside the LC717A30 by changing parameters, the following processing changes. In addition, after having changed the target channels by the CdacSel bit, the value of new CDAC minus reflects it to registers when the measurement processing is completed.

For more information, refer to “In the Case of Reading and Writing of the CdacP/CdacM/DigitalOffset Registers” in this document.

- Result Data Register

Address 0x2A	Bit	7	6	5	4	3	2	1	0
	Name	Cin7ACT	Cin6ACT	Cin5ACT	Cin4ACT	Cin3ACT	Cin2ACT	Cin1ACT	Cin0ACT
	Reset	0	0	0	0	0	0	0	0
	R/W	R	R	R	R	R	R	R	R

This register is used to output the result of touch “ON/OFF” judgment of each channel. The result data of Cin0 corresponds to the Cin0ACT bit (Bit0), the result data of Cin7 corresponds to the Cin7ACT bit (Bit7).

The touch “ON/OFF” is judged by both the measurement data of each channel and the touch “ON/OFF” threshold of each channel. The decision timing of data (end of measurement) is notified to microcontroller by INTOUT signal. So the microcontroller should read out the register’s values after asserting INTOUT signal.

CinXACT (X = 0 to 7)

0: Touch OFF judgment. (Initial value)

1: Touch ON judgement.

- Control 3 Register

Address 0x2B	Bit	7	6	5	4	3	2	1	0
	Name	MedMode1	MedMode0	AmpMode	CdacSel	Rsvd3	Rsvd2	Rsvd1	Rsvd0
	Reset	1	0	0	0	0	0	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

This register is used to set a target channel to read and write a digital offset level, a CDAC Plus level, a CDAC Minus level, and to set the amplifier connection composition during a measurement operation.

MedMode1, MedMode0

These are the bits to set the measurement filter operation mode to filter noise.

Initial values are MedMode1 = “1”, MedMode0 = “0”. Normally application should operate under this status.

AmpMode

This is the control bit to set the amplifier’s connection method in the measurement.

0: Measurement with a differential mode. (Initial value)

1: Measurement with a single mode.

CdacSel

This is the bit to set the target channel of Cin0−Cin3 or Cin4−Cin7 to read and write the data to the registers such as the CinX Digital Offset Register [Address=0x06 to 0x09] and the CinX CDAC Plus Register and the CinX CDAC Minus Register [Address=0x22 to 0x29].

0: Application can read and write the CDAC Plus values of Cin0−Cin3, the CDAC Minus values of Cin0−Cin3 and the digital offset values of Cin0−Cin3. (Initial value)

1: Application can read and write the CDAC Plus values of Cin4−Cin7, the CDAC Minus values of Cin4−Cin7 and the digital offset values of Cin4−Cin7.

Rsvd3 to Rsvd0

These bits are fixed to “0”. Don’t set to “1”.

- Error Status Register

Address 0x2C	Bit	7	6	5	4	3	2	1	0
	Name	SYSERR	Readd6	Readd5	Readd4	Readd3	DALM1	DALM0	CALERR
	Reset	0	0	0	0	0	0	0	0
	R/W	R	R	R	R	R	R	R	R

This register is used to notify of errors and non-errors.

SYSERR

0: No system error. (Initial value)

1: System error occurred.

In the case that the SYSERR bit sets to “1”. In order to reset the SYSERR bit to “0”, perform either the software-reset, the power on reset, or the reset of the nRST pin. The software-reset is performed by setting the SoftRst bit in the Control 2 Register [Address=0x40] to “1”.

Readd6 to Readd3

These bits output all “0”.

DALM1, DALM0

These bits are the alarm flag to notify the microcontroller of determining that an AD level might largely slip off by interference of the frequency, based on the result of the static offset calibration operation and dynamic offset calibration operation. In addition, the flag of DALM1 bit and DALM0 bit is updated at the end of next measurement after static offset calibration operation and dynamic offset calibration operation.

If an abnormality alarm level of AD level is “Level 0”, the LSI doesn’t receive most of the influence of the external noise. If an abnormality alarm level of AD level is “Level 3”, the LSI might receive the much influence of the external noise. So the AD level of measurement data and the result of touch ON/OFF detection might be abnormality.

DALM1	DALM0	Abnormality Alarm Level of AD Level
0	0	Level 0 (Initial value)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (The LSI might receive the much influence of the external noise)

CALERR

0: No calibration error. (Initial value)

1: Calibration error occurred.

In the case that the CALERR bit sets to “1”. In order to reset the CALERR bit to “0”, perform the parameter update processing. The parameter update processing is performed by setting the both ParaCh bit and WriteReq bit in the Control 1 Register [Address=0x2F] to “1”.

- Error Channel Status Register

Address 0x2D	Bit	7	6	5	4	3	2	1	0
	Name	Cin7ERR	Cin6ERR	Cin5ERR	Cin4ERR	Cin3ERR	Cin2ERR	Cin1ERR	Cin0ERR
	Reset	0	0	0	0	0	0	0	0
	R/W	R	R	R	R	R	R	R	R

This register is used to output the system error code “00h” in case of occurring system error by SYSERR = “1” or the calibration error channels in case of occurring calibration error by CALERR = “1”. The error channel status of Cin0 corresponds to Cin0ERR(Bit0). The error channel status of Cin7 corresponds to Cin7ERR(Bit7).

If the system error is occurred, all these bits are set to “0”. If the calibration error in Cin0 to Cin7 is occurred, the bit corresponding to channel with error is to “1”. In order to reset all the bits to “0”, perform the parameter update processing. The parameter update processing is performed by setting the both ParaCh bit and WriteReq bit in the Control 1 Register [Address=0x2F] to “1”.

CinXERR (X=0 to 7)

0: Channel CinX without calibration error. (Initial value)

1: Channel CinX with calibration error.

- Control 1 Register

Address 0x2F	Bit	7	6	5	4	3	2	1	0
	Name	WriteReq	Rsvd6	Rsvd5	MDtHold	IntMode	ParaCh	StaCal	Measure
	Reset	0	0	0	0	1	0	1	1
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

This register is used to set the each progressing operation for this LSI.

When at least one bit of the WriteReq bit, the ParaCh bit and the StaCal bit is not “0”, the microcontroller must not write to the Control 1 Register. (In other word, only when all of the WriteReq bit, the ParaCh bit and the StaCal bit are “0”, the microcontroller is able to write to the Control 1 Register)

As an exception, between the time when the LSI asserts the INTOUT to notify of completing the LSI internal initialization after the release of reset and the time when static offset calibration which is automatically performed based on default parameters is completed, the microcontroller might write 80h or 88h to the Control 1 Register even if the read value of the StaCal bit is “1”. By doing this, the execution of the static offset calibration and/or measurement based on LSI’s default parameters can be cancelled. For more information, refer to “Control Examples for the Microcontroller to Control the LC717A30” in this document.

WriteReq

This bit is used to reflect the setting of each control bit (The MDtHold bit, the IntMode bit, the ParaCh bit, the StaCal bit and the Measure bit in this register) to this LSI operation.

When the WriteReq bit is set to “1”, all the settings of the MDtHold bit, the IntMode bit, the ParaCh bit, the StaCal bit and the Measure bit are reflected to the LSI operation. When the WriteReq bit is set to “0”, all the settings of the MDtHold bit, the IntMode bit, the ParaCh bit, the StaCal bit and the Measure bit are not reflected to the LSI operation. Setting reflection processing is carried out when sleep state or interval state leave. After reflecting the settings to the LSI operation, the WriteReq bit returns to “0” automatically.

0: Not reflect all the settings of the IntMode bit, the MDtHold bit, the ParaCh bit, the StaCal bit and the Measure bit. (Initial value)

1: Reflect all the settings of the MDtHold bit, the IntMode bit, the ParaCh bit, the StaCal bit and the Measure bit.

Rsvd6, Rsvd5

These bits are fixed to“0”. Don’t set “1”.

MDtHold

This bit is used to set the preservation mode to keep measurement data.

In the case of Measure bit = “0”, when the MDtHold bit is “0”, the contents of the Cin0 to Cin7 Data Register [Address=0x1A to 0x21] and the Result Data Register [Address=0x2A] are cleared to “0”. When the MDtHold bit is “1”, the contents of the Cin0 to Cin7 Data Register [Address=0x1A to 0x21] and the Result Data Register [Address=0x2A] are kept, regardless of the content of Measure bit.

If application uses LSI of more than two, the microcontroller can read out the Cin0 to Cin7 Data and the Result Data with this MDtHold bit. About detail description, refer to “Control Examples for the Microcontroller to Control the LC717A30”.

0: When Measure bit is “0”, the measurement data such as the Cin0 to Cin7 Data and Result Data is cleared. (Initial value)
1: When Measure bit is “0”, the measurement data such as the Cin0 to Cin7 Data and Result Data isn’t cleared.

IntMode

This bit is used to set the measurement operation mode. For the further details of each mode, refer to “Description of Functions”.

0: Operate in sleep mode.
1: Operate in interval mode. (Initial value)

ParaCh

This bit is used to request this LSI to change settings (in other words, this bit is used to request this LSI to reflect register settings to the LSI operation).

If application need to change the parameter, it sets the ParaCh bit to “1” and reflects the settings of individual registers [Address=0x00 to 0x19, 0x22 to 0x29, 0x2B, and 0x30 to 0x3D] to the LSI operation.

When completing reflecting the settings to the LSI operation, the contents of the Result Data Register [Address=0x2A], the Error Status Register [Address=0x2C], the Error Channel Status Register [Address=0x2D] are all cleared to “0”, and INTOUT is negated. Counters inside this LSI which are used for the processing of the dynamic offset calibration and the processing of debounce, are all cleared. And then, the ParaCh bit returns to “0” automatically.

0: No request for changing parameters. (Initial value)
1: Changing parameters is requested.

StaCal

The bit is used to request this LSI to perform static offset calibration.

If the StaCal bit is set to “1”, the static offset calibration is performed. After static offset calibration has completed, the StaCal bit returns to “0” automatically. The static offset calibration performs offset adjustment of the capacity Digital to Analog converter for parasitism capacitance of each input channel (Cin0 to Cin7) and decides the most suitable offset level (the offset level of CDAC Plus, the offset level of CDAC Minus, and digital offset level) corresponding to each channel.

When the microcontroller writes the data in which the WriteReq bit is set to “1” and the StaCal bit is set to “0” (for example, 88h, 80h) into the Control 1 Register through the I^2C/SPI interface while this LSI is performing the static offset calibration, this LSI doesn’t cancel the execution of the static offset calibration immediately. It runs the current the static offset calibration processing to the end.

0: No request for static offset calibration.
1: Static offset calibration is requested. (Initial value)

Measure

This bit is used to set the operation and unoperation of measurement.

It is normally fixed to “1” unless you have specific reasons.

0: No measurement.
1: Measurement. (Initial value)

NOTE: Note: Processing order (The processing order when all of the WriteReq bit, the ParaCh bit, the StaCal bit and the Measure bit are set to “1” at a time is as follows)
(1) Control bit reflection processing (the WriteReq bit). After reflecting to this LSI, the WriteReq bit returns to “0”.
(2) Changing parameters processing (the ParaCh bit). After the processing, the ParaCh bit returns to “0”.
(3) Static offset calibration processing (the StaCal bit). After the processing, the StaCal bit returns to “0”.
(4) Measurement processing (the Measure bit). This LSI repeats the measurement processing.

- Average Count Register

Address 0x30	Bit	7	6	5	4	3	2	1	0
	Name	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
	Reset	0	1	0	0	0	0	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

This register is used to set the average counts of measurement data. In 8, 16, 32, 64, 128 times, please set one by all means. (Don't set any value other than 8, 16, 32, 64, 128 times). The initial value is "40h" showing "64 times".

AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Average Counts of the Measurement Data
0	0	0	0	1	0	0	0	8 times
0	0	0	1	0	0	0	0	16 times
0	0	1	0	0	0	0	0	32 times
0	1	0	0	0	0	0	0	64 times (Initial value)
1	0	0	0	0	0	0	0	128 times
Other than those above								Prohibited

- Filter Parameter Register

Address 0x31	Bit	7	6	5	4	3	2	1	0
	Name	FP23	FP22	FP21	FP20	FP13	FP12	FP11	FP10
	Reset	0	0	0	0	0	0	1	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

This register is used to set a measurement filter parameter for noise measures.

FP23 to FP20

These bits are used to set state of measurement filter parameter 2 for noise measures.
Usually use initial values for 0h.

FP13 to FP10

These bits are used to set state of measurement filter parameter 1 for noise measures.
Usually use initial values for 2h.

- Debounce Count 1 Register

Address 0x32	Bit	7	6	5	4	3	2	1	0
	Name	DCT17	DCT16	DCT15	DCT14	DCT13	DCT12	DCT11	DCT10
	Reset	0	0	0	0	0	0	0	1
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

This register is used to set the number of debounce count, which the parameter value is used for touch “ON/OFF” judgment by this LSI when the touch decision at each channel changes from “OFF” state to “ON” state. By setting properly the debounce count, you can prevent chattering of a switch. If application would like to set the debounce count to N1, application have to set this register to (N1−1). The initial value of debounce count is 2 counts (The initial value of the Debounce Count 1 Register is 01h).

The condition for the result of “ON/OFF” judgment to change from “OFF” state to “ON” state at each channel:

When the number of consecutive measurement points that measurement data is greater than or equal to the touch ON threshold setting with Cin0−7 ON Threshold Register [Address=0x0A to 0x11] becomes equal to the number of debounce count specified by the Debounce Count 1 Register, the result of “ON/OFF” judgment changes to the touch “ON”.

DCT17	DCT16	DCT15	DCT14	DCT13	DCT12	DCT11	DCT10	Debounce Count (from Touch OFF to Touch ON)
0	0	0	0	0	0	0	0	1 count
0	0	0	0	0	0	0	1	2 counts (Initial value)
0	0	0	0	0	0	1	0	3 counts
0	0	0	0	0	0	1	1	4 counts
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	1	1	1	0	1	254 counts
1	1	1	1	1	1	1	0	255 counts
1	1	1	1	1	1	1	1	Prohibited

- Debounce Count 2 Register

Address 0x33	Bit	7	6	5	4	3	2	1	0
	Name	DCT27	DCT26	DCT25	DCT24	DCT23	DCT22	DCT21	DCT20
	Reset	0	0	0	0	0	0	0	1
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

This register is used to set the number of debounce count, which the parameter value is used for “ON/OFF” judgment by this LSI when the touch decision at each channel changes from “ON” state to “OFF” state. By setting properly the debounce count, you can prevent chattering of a switch. If application would like to set the debounce count to N2, application has to set this register to (N2−1). The initial value of debounce count is 2 counts. (The initial value of the Debounce Count 1 Register is 01h) This value should be specified greater than or equal to the value specified by Debounce Count 1 Register [Address=0x32].

The condition for the result of “ON/OFF” judgment to change from “ON” state to “OFF” state at each channel:

When the number of consecutive measurement points that measurement data is less than the touch OFF threshold setting with Cin0−7 OFF Threshold Register [Address=0x12 to 0x19] becomes equal to the number of debounce count specified by the Debounce Count 2 Register, the result of “ON/OFF” judgment changes to be “OFF”.

DCT27	DCT26	DCT25	DCT24	DCT23	DCT22	DCT21	DCT20	Debounce Count (from Touch ON to Touch OFF)
0	0	0	0	0	0	0	0	1 count
0	0	0	0	0	0	0	1	2 counts (Initial value)
0	0	0	0	0	0	1	0	3 counts
0	0	0	0	0	0	1	1	4 counts
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	1	1	1	0	1	254 counts
1	1	1	1	1	1	1	0	255 counts
1	1	1	1	1	1	1	1	Prohibited

- Short Interval Time Register

Address 0x34	Bit	7	6	5	4	3	2	1	0
	Name	SIVAL7	SIVAL6	SIVAL5	SIVAL4	SIVAL3	SIVAL2	SIVAL1	SIVAL0
	Reset	0	0	0	0	0	1	0	1
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

This register is used to set the short interval time during interval mode. “Short interval time” is the interval between the end time of one measurement and the start time of the next measurement when the touch ON may be detected. The value of long interval time can be specified from 0 ms to 255 ms in units of 1ms (Typ). The initial value is 5 ms (Typ) (05h).

If this register is set to 00h, both long interval time and short interval time are set to 0 ms. For more information about the Short Interval Mode, refer to “Description of Functions”.

When sleep mode is selected, it operates with the short interval time of 0 ms regardless of the setting contents of this register.

SIVAL7	SIVAL6	SIVAL5	SIVAL4	SIVAL3	SIVAL2	SIVAL1	SIVAL0	Short Interval Time
0	0	0	0	0	0	0	0	0 ms
0	0	0	0	0	0	0	1	1 ms
0	0	0	0	0	0	1	0	2 ms
0	0	0	0	0	0	1	1	3 ms
0	0	0	0	0	1	0	0	4 ms
0	0	0	0	0	1	0	1	5 ms (Initial value)
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	1	1	1	1	0	254 ms
1	1	1	1	1	1	1	1	255 ms

- Long Interval Time Register

Address 0x35	Bit	7	6	5	4	3	2	1	0
	Name	LIVAL7	LIVAL6	LIVAL5	LIVAL4	LIVAL3	LIVAL2	LIVAL1	LIVAL0
	Reset	0	0	0	0	0	0	0	1
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

This register is used to set the long interval time during interval mode. “Long interval time” is the interval between the end time of one measurement and the start time of the next measurement when the touch ON is not detected at all. The value of long interval time can be specified from 0 ms to 355 ms in units of 1 ms (Typ). The long interval time is set with the long interval base time and the value of this register. The long interval base time can be selected from either 100 ms (Initial value) or 0 ms by specifying the LIVALB bit in the Measurement Mode 1 Register [Address=0x3A]. The initial value is 100 ms + 1 ms (01h) = 101 ms (Typ).

If this register is set to 00h, both long interval time and short interval time are set to 0 ms. For more information about the Long Interval Mode, refer to “Description of Functions”.

When sleep mode is selected, it operates with the long interval time of 0 ms regardless of this setting contents of this register.

LIVAL7	LIVAL6	LIVAL5	LIVAL4	LIVAL3	LIVAL2	LIVAL1	LIVAL0	Long Interval Time	
								LIVALB = “0”	LIVALB = “1”
0	0	0	0	0	0	0	0	No interval (0 ms)	No interval (0 ms)
0	0	0	0	0	0	0	1	101 ms (Initial value)	1 ms
0	0	0	0	0	0	1	0	102 ms	2 ms
0	0	0	0	0	0	1	1	103 ms	3 ms
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	1	1	1	1	0	354 ms	254 ms
1	1	1	1	1	1	1	1	355 ms	255 ms

- Short Interval Dynamic OffCal Cycle Register

Address 0x36	Bit	7	6	5	4	3	2	1	0
	Name	DCYC7	DCYC6	DCYC5	DCYC4	DCYC3	DCYC2	DCYC1	DCYC0
	Reset	0	0	0	0	0	0	1	1
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

This register is used to set an enforcement cycle judging whether the dynamic offset calibration is carried out or not when this LSI operates with the short interval mode. The initial value is “03h”. It makes the judgment of one in every 3 measurements.

A value of “Short interval time” usually differs from that of “Long interval time”. So the measurement to measurement interval in short interval mode usually differs from that in long interval mode. Therefore, it is necessary for the microcontroller to write an appropriate value to this register so that a value of interval to perform the processing of the dynamic offset calibration in short interval mode may be as equal as possible to that in long interval mode.

When this LSI operates with the long interval mode, the judgment is made at every measurement regardless of this register setting.

When sleep mode is selected, be sure to set this register to 01h.

When this register is set to 00h, dynamic offset calibration is not performed at all regardless of other register settings.

For more information about dynamic offset calibration, refer to “Explanation of the Dynamic Offset Calibration”.

DCYC7	DCYC6	DCYC5	DCYC4	DCYC3	DCYC2	DCYC1	DCYC0	The Number of Execution Cycles for the Judgment of the Dynamic Offset Calibration Operation		
								Short Interval Mode	Long Interval Mode	Sleep Mode
0	0	0	0	0	0	0	0	The dynamic offset calibration isn’t performed		
0	0	0	0	0	0	0	1	Once every 1 measurement	Once every 1 measurement	Once every 1 measurement
0	0	0	0	0	0	1	0	Once every 2 measurements		
0	0	0	0	0	0	1	1	Once every 3 measurements (Initial value)		
0	0	0	0	0	1	0	0	Once every 4 measurements		
0	0	0	0	0	1	0	1	Once every 5 measurements		
0	0	0	0	0	1	1	0	Once every 6 measurements		
0	0	0	0	0	1	1	1	Once every 7 measurements		
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .		
1	1	1	1	1	1	1	0	Once every 254 measurements		
1	1	1	1	1	1	1	1	Once every 255 measurements		

- Dynamic OffCal Count Plus Register

Address 0x37	Bit	7	6	5	4	3	2	1	0
	Name	DCALP7	DCALP6	DCALP5	DCALP4	DCALP3	DCALP2	DCALP1	DCALP0
	Reset	0	0	0	0	0	0	1	1
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

This register is used to set the dynamic offset calibration enforcement count number of plus level side. The initial value is 03h. This means that the number of consecutive measurement points is 24 points, which is equal to 8 times of the register setting value 03h. This LSI performs judgment processing of the dynamic offset calibration enforcement in the following cases by the PDCLP bit in the Measurement Mode Register [Address=0x3A] is set.

Case1: When the PDCLP bit is set to “0” and all channels are touch OFF states (OFF detection of all channels), this LSI carries out judgment processing.

Case2: When the PDCLP bit is set to “1”, this LSI carries out judgment processing for a channel of touch OFF state because dynamic offset calibration is determined and performed at each individual enabled channel.

When the long interval mode, the LSI judges enforcement of the dynamic offset calibration at every measurement. When the measurement data of the judgment processing (Judgment points) under the constant number of times specified by the Dynamic OffCal Count Plus Register [Address=0x37] continues in the dynamic offset calibration operating range (from the lower limit AD level of plus level side to the touch ON threshold), this LSI enforces the dynamic offset calibration.

When the short interval mode, the LSI judges enforcement of the dynamic offset calibration by a measurement count of the number of times that the LSI specified in the Short Interval Dynamic OffCal Cycle Register [Address=0x36]. When the measurement data of the judgment processing (Judgment points) under the constant number of times specified by the Dynamic OffCal Count Plus Register [Address=0x37] continues in the dynamic offset calibration operating range (from the lower limit AD level of plus level side to the touch ON threshold), this LSI enforces the dynamic offset calibration.

When this register is set to 00h, dynamic offset calibration is not performed at all regardless of other register settings.

For more information about dynamic offset calibration, refer to “Explanation of the Dynamic Offset Calibration”.

DCALP7	DCALP6	DCALP5	DCALP4	DCALP3	DCALP2	DCALP1	DCALP0	Number of Consecutive Measurements Points for the Dynamic Offset Calibration Operation (Positive Range)	
								Short Interval Mode	Long Interval Mode
0	0	0	0	0	0	0	0	The dynamic offset calibration isn’t performed	The dynamic offset calibration isn’t performed
0	0	0	0	0	0	0	1	(8 × Enforcement cycle) points	8 points
0	0	0	0	0	0	1	0	(16 × Enforcement cycle) points	16 points
0	0	0	0	0	0	1	1	(24 × Enforcement cycle) points	24 points (Initial value)
0	0	0	0	0	1	0	0	(32 × Enforcement cycle) points	32 points
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	1	1	1	1	0	(2032 × Enforcement cycle) points	2032 points
1	1	1	1	1	1	1	1	(2040 × Enforcement cycle) points	2040 points

NOTE: The “Enforcement cycle” is an enforcement cycle judging whether the dynamic offset calibration is carried out or not to be set in the Short Interval Dynamic OffCal Cycle Register [Address=0x36].

- Dynamic OffCal Count Minus Register

Address 0x38	Bit	7	6	5	4	3	2	1	0
	Name	DCALM7	DCALM6	DCALM5	DCALM4	DCALM3	DCALM2	DCALM1	DCALM0
	Reset	0	0	0	0	0	0	1	1
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

This register is used to set the dynamic offset calibration enforcement count number of minus level side. The initial value is 03h.

When the long interval mode, the LSI judges enforcement of the dynamic offset calibration at every measurement. When the measurement data of the judgment processing (Judgment points) under the constant number of times specified by the Dynamic OffCal Count Minus Register [Address=0x38] continues in the dynamic offset calibration operating range (from −128 to upper limit AD level of minus level side), this LSI enforces the dynamic offset calibration.

When the short interval mode, the LSI judges enforcement of the dynamic offset calibration by a measurement count of the number of times that the LSI specified in the Short Interval Dynamic OffCal Cycle Register [Address=0x36]. When the measurement data of the judgment processing (Judgment points) under the constant number of times specified by the Dynamic OffCal Count Minus Register [Address=0x38] continues in the dynamic offset calibration operating range (from −128 to upper limit AD level of minus level side), this LSI enforces the dynamic offset calibration.

When this register is set to 00h, dynamic offset calibration is not performed at all regardless of other register settings.

For more information about dynamic offset calibration, refer to "Explanation of the Dynamic Offset Calibration".

DCALM7	DCALM6	DCALM5	DCALM4	DCALM3	DCALM2	DCALM1	DCALM0	Number of Consecutive Measurements Points for the Dynamic Offset Calibration Operation (Negative Range)	
								Short Interval Mode	Long Interval Mode
0	0	0	0	0	0	0	0	The dynamic offset calibration isn't performed.	The dynamic offset calibration isn't performed.
0	0	0	0	0	0	0	1	(1 × Enforcement cycle) points	1 point
0	0	0	0	0	0	1	0	(2 × Enforcement cycle) points	2 points
0	0	0	0	0	0	1	1	(3 × Enforcement cycle) points	3 points (Initial value)
0	0	0	0	0	1	0	0	(4 × Enforcement cycle) points	4 points
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	1	1	1	1	0	(254 × Enforcement cycle) points	254 points
1	1	1	1	1	1	1	1	(255 × Enforcement cycle) points	255 points

NOTE: The "Enforcement cycle" is an enforcement cycle judging whether the dynamic offset calibration is carried out or not to be set in the Short Interval Dynamic OffCal Cycle Register [Address=0x36].

- Static OffCal CDAC Base Register

Address 0x39	Bit	7	6	5	4	3	2	1	0
	Name	DACB7	DACB6	DACB5	DACB4	DACB3	DACB2	DACB1	DACB0
	Reset	1	0	0	0	0	0	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

This register is used to set the reference capacitance when static offset calibration is performed.

If the reference value (In other words, the measurement data when the touch ON is not detected at all) might not coincide with the vicinity of the center of measurement range (that is, almost 0) after static offset calibration, this problem may be resolved by changing the value of reference capacitance.

Don't set any value but 20h, 40h, 80h. The initial value is 80h. It shows 4 pF.

DACB7	DACB6	DACB5	DACB4	DACB3	DACB2	DACB1	DACB0	The Reference Capacitance Used when Static Offset Calibration is Executed
0	0	1	0	0	0	0	0	1 pF
0	1	0	0	0	0	0	0	2 pF
1	0	0	0	0	0	0	0	4 pF
Other than those above								Prohibited setting

- Measurement Mode 1 Register

Address 0x3A	Bit	7	6	5	4	3	2	1	0
	Name	INTMD1	INTMD2	PDCLP	DmCyc	LIVALB	MCIN1	MCIN0	Rsvd0
	Reset	0	0	0	0	0	0	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

This register is used to set the measurement mode.

INTMD1

This bit is used to specify the output mode of INTOUT at the end of each measurement. By specifying the INTMD1 bit, the microcontroller can select how to assert the INTOUT signal. (The meaning that INTOUT is asserted is that INTOUT signal outputs high level).

0: Whenever the measurement was completed, INTOUT is asserted. (Initial value)
1: Only when the measurement was completed, and at least one channel is the touch ON judgment state, INTOUT is asserted. For more information about the touch ON judgment state, refer to "Explanation of the Touch Judgment".

INTMD2

This bit is used to specify the output mode of INTOUT either at the end of interval processing (In the case of interval mode) or at the wake-up of this LSI (In the case of sleep mode). By specifying the INTMD2 bit, the microcontroller can select how to negate the INTOUT signal. (The meaning that INTOUT is negated is that INTOUT signal outputs low level).

0: INTOUT is not negated automatically. (Initial value)
1: In the case of interval mode, this LSI automatically negates INTOUT immediately after the end of interval processing. In the case of sleep mode, this LSI automatically negates INTOUT immediately after the microcontroller wakes up this LSI.

INTOUT output mode when measurement has finished.

INTMD1	INTMD2	INTOUT Output Mode when Measurement Has Finished
0	0	Whenever the measurement was completed, INTOUT is asserted. To clear (Low level) INTOUT signal, set the IntOut bit in the Control 2 Register [Address=0x40] to “0”.
0	1	Whenever the measurement was completed, INTOUT is asserted. After that, this LSI automatically negates (Low level) INTOUT signal either at the end of interval processing (In the case of interval mode) or at the wake-up of this LSI (In the case of sleep mode).
1	0	Only when the measurement was completed, and at least one channel is the touch ON judgment state, INTOUT is asserted. To clear (Low level) INTOUT signal, set the IntOut bit in the Control 2 Register [Address=0x40] to “0”.
1	1	Only when the measurement was completed, and at least one channel is the touch ON judgment state, INTOUT is asserted. After that, the LSI automatically negates (Low level) INTOUT signal either at the end of interval processing (In the case of interval mode) or at the wake-up of this LSI (In the case of sleep mode).

PDCLP

This bit is used to select the method of the dynamic offset calibration for the positive range of measurement data.

0: Dynamic offset calibration for the positive range is determined and performed, only when measurement data of all touches are less than or equal to the touch ON threshold value. (Initial value)
1: Dynamic offset calibration for the positive range is determined and performed at each individual enabled channel.

For example, only if measurement data corresponding to a switch doesn’t vary at all when another switch is touched (In other words, if each switch is sufficiently far from each other), this PDCLP bit can be set to “1”.

DmCyc

This bit is used to set the number of dummy cycles at time of measurement start.

0: 4 cycles. (Initial value)
1: 7 cycles.

LIVALB

This bit is used for selecting the long interval base time.
For more information about the Long Interval Mode, refer to “Description of Functions”.

0: The long interval base time is 100 ms (Typ). (Initial value)
1: The long interval base time is 0 ms.

MCIN1, MCIN0

These bits are used to specify the output states of non-measurement channel during measurement operation.

The non-measurement channel means channels other than a measurement channel, in the enabled channels which the CinXEN bit is set to “1” with Use Channel Register [Address=0x00]. The disabled channels which the CinXEN bit is set to “0” with Use Channel Register [Address=0x00] are set to low level.

In the condition other than measurement operation, each pins such as Cin0 to Cin7, CMAdd0, CMAdd4, Cref, CrefAdd, CdrvBar are set to low level.

MCIN1	MCIN0	The State of Non-measurement Channel during Measurement Operation
0	0	Low level (Initial value)
0	1	Prohibited setting
1	0	High impedance (Hi−Z)
1	1	Cdrv signal output

Rsvd0

This bit is fixed to “0”. Don’t set “1”.

- Measurement Mode 2 Register

Address 0x3B	Bit	7	6	5	4	3	2	1	0
	Name	CDRVB	CADD4EN	CADD0EN	CIN4CINP2	CIN0CINP2	CIN4CINP	CIN0CINP	Rsvd0
	Reset	0	0	0	0	0	0	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

This register is used to set the operating status of each pin during measurement operation.

CDRVB

This bit is used to output the inversion signal of Cdrv to the CdrvBar pin.

If this LSI drives the sensor Cin of large capacitance, it can detect the capacitance change with connecting an appropriate capacitor between the Cin0−Cin7 pins and the CdrvBar pin. In this case, set this bit to “1”.

0: The CdrvBar pin is set to high impedance state. (Initial value)
1: The CdrvBar pin outputs the inversion signal of Cdrv.

CADD4EN

This bit enables the CMAdd4 pin for adding the offset capacitor to the capacitance sensor input’s Cin4−Cin7.

If this LSI drives the sensor Cin4−Cin7 of large capacitance, it can detect the capacitance change with connecting an appropriate capacitor between the CMAdd4 pin and the CdrvBar pin. In this case, set this bit to “1”.

0: The CMAdd4 isn’t used during the measurement of Cin4−Cin7. (Initial value)
1: The CMAdd4 is used during the measurement of Cin4−Cin7.

CADD0EN

This bit enables the CMAdd0 pin for adding the offset capacitor to the capacitance sensor input’s Cin0−Cin3.

If this LSI drives the sensor Cin0−Cin3 of large capacitance, it can detect the capacitance change with connecting an appropriate capacitor between the CMAdd0 pin and the CdrvBar pin. In this case, set this bit to “1”.

0: The CMAdd0 isn’t used during the measurement of Cin0−Cin3. (Initial value)
1: The CMAdd0 is used during the measurement of Cin0−Cin3.

CIN4CINP2

This bit is used to select a pin which connects to the input of 1st amplifier (+) side when Cin4 to Cin7 are measured.

Basically, set this bit to “1” and the reference capacitance pin uses the Cref pin when the measurement from Cin4 to Cin7.

0: The Cref can be used during the measurement of Cin4−Cin7. (Initial value)
1: The Cref and CrefAdd can be used during the measurement of Cin4−Cin7.

CIN0CINP2

This bit is used to select a pin which connects to the input of 1st amplifier (+) side when Cin0 to Cin3 are measured.

Basically, set this bit to “1” and the reference capacitance pin uses the Cref pin when the measurement from Cin0 to Cin3.

0: The Cref can be used during the measurement of Cin0−Cin3. (Initial value)
1: The Cref and CrefAdd can be used during the measurement of Cin0−Cin3.

CIN4CINP

This bit is fixed to “0”. Don’t set “1”.

CIN0CINP

This bit is fixed to “0”. Don’t set “1”.

Operation setting of each pin when during measurement.

CADD4EN	CADD0EN	CIN4CINP2	CIN0CINP2	An Application and Setting Contents Explanation
0	0	0	0	Applicable to configuration of small capacitive sensors (8 pF or less). The CMAdd4 pin and CMAdd0 for adding the offset capacitor to the capacitance sensor input's from Cin0 to Cin7 are not used. In addition, the reference capacitance pin uses Cref pin when measurement from Cin0 to Cin7. (For more information about the connection constitution example, refer to Figure 56)
1	1	0	0	Applicable to configuration of large capacitive sensors (More than 8 pF). The CMAdd4 pin and CMAdd0 for adding the offset capacitor to the capacitance sensor input's from Cin0 to Cin7 are used. In addition, the reference capacitance pin uses Cref pin when measurement from Cin0 to Cin7. (For more information about the connection constitution example, refer to Figure 59)
0	1	0	1	Applicable to configuration that large capacitive sensors (in the Cin0 to Cin3) and small capacitive sensors (in the Cin4 to Cin7) are mixed. The CMAdd0 for adding the offset capacitor to the capacitance sensor input's from Cin0 to Cin3 is used. And the CMAdd4 for adding the offset capacitor to the capacitance sensor input's from Cin4 to Cin7 is not used. In addition, the reference capacitance pin uses both Cref pin and CrefAdd pin when measurement from Cin0 to Cin3. And the reference capacitance pin uses only Cref pin when measurement from Cin4 to Cin7. (For more information about the connection constitution example, refer to Figure 62)
1	0	1	0	Applicable to configuration that small capacitive sensors (in the Cin0 to Cin3) and large capacitive sensors (in the Cin4 to Cin7) are mixed. The CMAdd0 for adding the offset capacitor to the capacitance sensor input's from Cin0 to Cin3 is not used. And the CMAdd4 for adding the offset capacitor to the capacitance sensor input's from Cin4 to Cin7 is used. In addition, the reference capacitance pin uses only Cref pin when measurement from Cin0 to Cin3. And the reference capacitance pin uses both Cref pin and CrefAdd pin when measurement from Cin4 to Cin7.
Combination except the above				We do not recommend the setting using an unused pin because it may influence the fall of detection sensitivity.

Rsvd0

This bit is fixed to "0". Don't set "1".

- Long Interval Mode Start Count Register

Address 0x3C	Bit	7	6	5	4	3	2	1	0
	Name	LIMSC7	LIMSC6	LIMSC5	LIMSC4	LIMSC3	LIMSC2	LIMSC1	LIMSC0
	Reset	0	0	0	0	0	1	0	1
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

This resister is used to set the number of measurement count from the time when all enabled channels have been judged to be touch OFF to the time when this LSI moves to Long Interval Mode. The initial value is 05h. The measurement counts are 20 points. (It is expressed with the value that multiplied 4 by value 5 to be set in this register.).

By writing an appropriate value to this register, application can provide the period which this LSI operates in short interval mode for a while after all enabled channels have been judged to be touch OFF.

LIMSC7	LIMSC6	LIMSC5	LIMSC4	LIMSC3	LIMSC2	LIMSC1	LIMSC0	Measurement Number of Times Setting until a Long Interval Mode Start
0	0	0	0	0	0	0	0	0 point
0	0	0	0	0	0	0	1	4 points
0	0	0	0	0	0	1	0	8 points
0	0	0	0	0	0	1	1	12 points
0	0	0	0	0	1	0	0	16 points
0	0	0	0	0	1	0	1	20 points (Initial value)
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	1	1	1	1	0	1016 points
1	1	1	1	1	1	1	1	1020 points

- Cin 1st Gain Adjust Register

Address 0x3D	Bit	7	6	5	4	3	2	1	0
	Name	Gain4F3	Gain4F2	Gain4F1	Gain4F0	Gain0F3	Gain0F2	Gain0F1	Gain0F0
	Reset	0	0	0	0	0	0	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

In this LSI, there are two steps of amplifiers (1st-amplifier and 2nd-amplifier) which detect changes in the capacitance and output an analog signal corresponding to the changes. This register sets the gain of the 1st-amplifier and adjusts the sensitivity of the channel. The gain of the 1st-amplifier of Cin0−Cin3 is specified with lower 4 bits, and the gain of the 1st-amplifier of Cin4−Cin7 is specified with upper 4 bits. Gain setting of Cin0−Cin7 is only common setting, and the individual Cin channels setting is not possible. The gain of 2nd-amplifier is set by the Cin 2nd Gain Adjust Register [Address=0x02 to 0x05]. Use the gain of the 1st-amplifier with a minimum basically.

Gain4F0 to 3: The gain of the 1st-amplifier of Cin4−Cin7 is specified with upper 4 bits.
(Initial value is 0h showing 1600 fF)

Gain0F0 to 3: The gain of the 1st-amplifier of Cin0−Cin3 is specified with lower 4 bits.
(Initial value is 0h showing 1600 fF)

The 1st-amplifier gain setting

Gain0F3 Gain4F3	Gain0F2 Gain4F2	Gain0F1 Gain4F1	Gain0F0 Gain4F0	1st-amplifier Gain Cf [fF] (Typ)
0	0	0	0	1600 (Minimum gain setting) (Initial value)
0	0	0	1	1500
0	0	1	0	1400
0	0	1	1	1300
0	1	0	0	1200
0	1	0	1	1100
0	1	1	0	1000
0	1	1	1	900
1	0	0	0	800
1	0	0	1	700
1	0	1	0	600
1	0	1	1	500
1	1	0	0	400
1	1	0	1	300
1	1	1	0	200
1	1	1	1	100 (Maximum gain setting)

<Approximate Calculation Formula of the Amplifier Output Voltage>

Output voltage of 1st and 2nd in the two-stage amplifier

Output voltage of the 1st-amplifier: $\Delta V_1 = (\Delta C/Cf) \times V_{CDRV}$ $\Delta V_1 < 0.8 \times V_{DD}$

Output voltage of the 2nd-amplifier: $\Delta V_2 = \Delta V_1 \times ga2$ $\Delta V_2 < 0.8 \times V_{DD}$

ΔC : Change in input capacitance (Capacitance change when touch)

Cf : The 1st-amplifier gain setting (Feedback capacitance in the LSI)

V_{CDRV} : High output voltage of Cdrv (=V_{DD})

ga2 : The 2nd-amplifier gain setting (times)

- Control 2 Register

Address 0x40	Bit	7	6	5	4	3	2	1	0
	Name	SoftRst	Rsvd6	Rsvd5	Rsvd4	Rsvd3	DyCalAck	IntOut	WakeUp
	Reset	0	0	0	0	0	0	0	0
	R/W	RW	RW	RW	RW	RW	RW	RW	RW

This register is used to set the each progressing operation for this LSI or to notify the progressing operation to the microcontroller.

When writing a certain value to this register either to clear INTOUT output or to wake up this LSI that is sleeping, do it during interval processing (In the case of interval mode) or during sleep period (In the case of sleep mode). If it can't be guaranteed that the microcontroller writes during interval processing, select the Interval Mode and select the mode that INTOUT is negated automatically (In other words, set the IntMode bit in Control 1 Register [Address=0x2F] to "1", and set the INTMD2 bit in Measurement Mode 1 Register [Address=0x3A] to "1").

SoftRst

Software-reset bit. When this bit is set to "1", software-reset is performed in the LSI. After software-reset is performed, it is returned to "0" automatically. For more information about software-reset, refer to "The Operating Sequence Example at the time of Software-reset".

0: Normal operation. (Initial value)
1: Software-reset.

When the software reset is performed, this bit returns to "0" automatically by the initialization processing.

Rsvd6 to Rsvd3

These bits are fixed to "0". Don't set "1".

DyCalAck

The flag bit shows the dynamic offset calibration operation.

0: The dynamic offset calibration isn't performed. (Initial value)
1: The dynamic offset calibration is performed.

When the dynamic offset calibration is performed, the IntOut bit is set to "1" and the INTOUT signal is asserted. (High level)

IntOut

This bit is the control bit for INTOUT signal. When clearing INTOUT output (that is, when setting the output of INTOUT pin to "Low"), set this bit to "0".

When the microcontroller clears the INTOUT output to "Low" in interval mode operation, set this bit to "0" while this LSI is in interval processing. When the microcontroller clears the INTOUT output to "Low" in sleep mode operation, set this bit to "0" while this LSI is sleeping.

0: INTOUT signal is negated. INTOUT pin is set to "Low". (Initial value).
1: INTOUT signal is asserted. INTOUT pin is set to "High".

WakeUp

This bit is used to cancel the sleep mode. It is used to wake up this LSI that is sleeping.

When the microcontroller sets this bit to "1", it can wake up this LSI which is sleeping. Immediately after this LSI has been woken up, this bit returns to "0" automatically.

0: Normal operation. (Initial value)
1: Wake up the LSI which is sleeping.

- SLAVE Address Register

Address 0x7F	Bit	7	6	5	4	3	2	1	0
	Name	Rsvd7	Slave6	Slave5	Slave4	Slave3	Slave2	Slave1	SA0
	Reset	0	0	0	1	0	1	1	X
	R/W	R	R	R	R	R	R	R	R

This register is used to output the I^2C slave address (7bit).

The SA0 bit is set by the state of SA0/SO pin. When the input to the SA0/SO pin is “High”, the SA0/SO bit is “1”. When the input to the SA0/SO pin is “Low”, the bit is “0”. As the input to the SA0/SO pin is reflected to the SA0 bit, the SA0 bit value can be changed at any time. However, basically the bit always has to be fixed to either “0” or “1”.

Rsvd7

This bit is fixed to “0”. Don’t set “1”.

I^2C compatible bus slave address

The Input of SA0/SO Pin	7bit Slave Address (Slave6 to Slave1 + SA0)	Binary Notation	8bit Stave Address
Low	16h	00101100b (Write)	2Ch
		00101101b (Read)	2Dh
High	17h	00101110b (Write)	2Eh
		00101111b (Read)	2Fh

Description about the communication format of I^2C compatible bus.

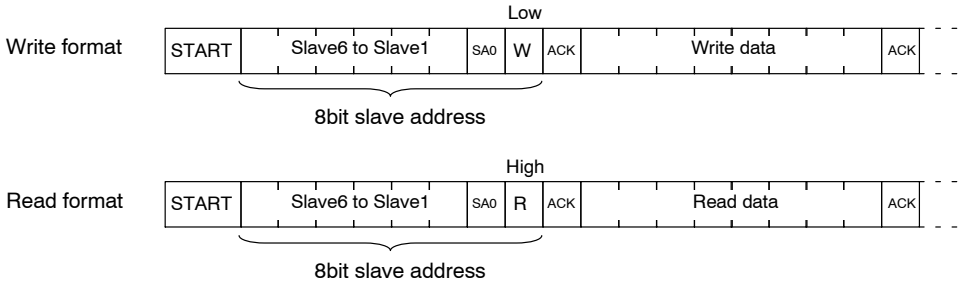


Figure 1.

FUNCTIONS

Description of Functions

Interval Mode and Sleep Mode

1. Interval Mode (Recommended)
   This is the mode that the LSI performs interval processing with either short interval or long interval after measurement processing. It is possible to select this mode by the IntMode bit in the Control 1 Register [Address=0x2F] to “1”.

2. Sleep Mode
   This is the mode that the LSI performs sleep processing after measurement processing. (In the LSI which is sleeping, main clock and logic circuit are both suspended). And then, the LSI operation is resumed by wake-up from the microcontroller. It is possible to select this mode by the IntMode bit in the Control 1 Register [Address=0x2F] to “0”.

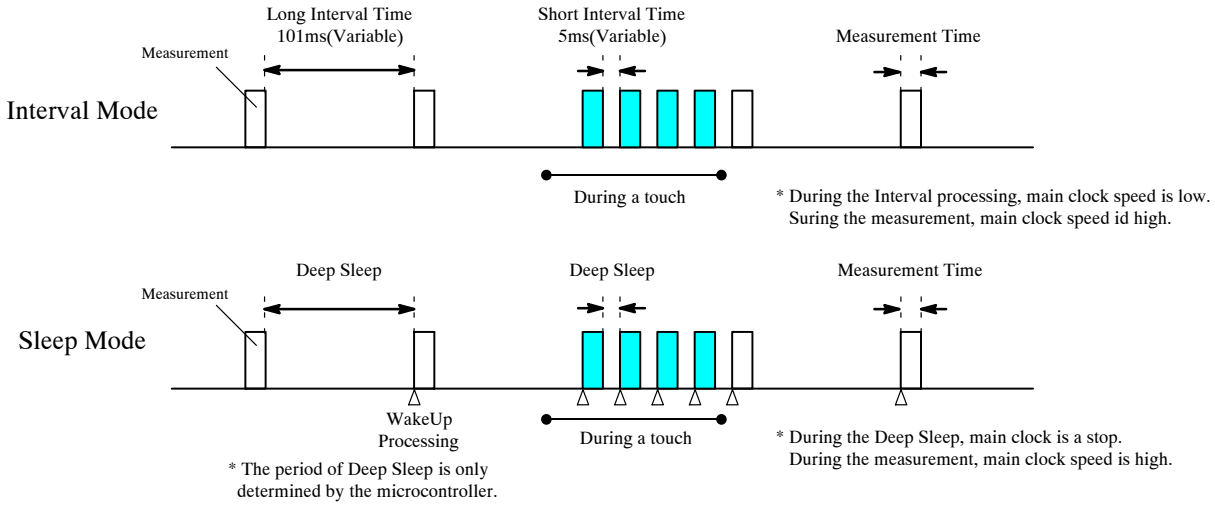


Figure 2. Interval Mode and Sleep Mode

Short Interval Mode and Long Interval Mode

1. Short Interval Mode
   This is the mode that the period of interval processing at Interval Mode is decided by the Short Interval Time Register [Address=0x34] (Short interval time). When the touch ON detected, the mode changes into Short Interval Mode immediately. Furthermore, when this LSI operates with this mode and the touch ON has not been detected only for a little while, the mode doesn’t change.
   Condition for change to “Short Interval Mode”:
   Regardless of whether the previous state is Short Interval Mode or Long Interval Mode, if the measurement data of at least one channel is greater than or equal to the touch ON threshold, the mode changes into “Short Interval Mode” immediately.

2. Long Interval Mode
   This is the mode that the period of interval processing at Interval Mode is decided by the Long Interval Time Register [Address=0x35] and the LIVALB bit in the Measurement Mode 1 Register [Address=0x3A] (Long interval time). When the touch ON is not detected at all, the mode changes into Long Interval mode.
   Condition for change to “Long Interval Mode”:
   During the “Short Interval Mode” operation, if the number of consecutive measurement points that measurement data is less than the touch OFF threshold for all the enabled channels becomes equal to the debounce counts (ON → OFF) that is specified by the Debounce Count 2 Register [Address=0x33], and subsequently the number of consecutive measurement points that data is less than the touch OFF threshold for all the enabled channels becomes equal to the number of points which is specified by Long Interval Mode Start Count Register [Address=0x3C], the mode changes into “Long Interval Mode”. (In short, after “all the enabled channels have been in no touch state for a while, the mode changes into Long Interval Mode)

Touch-ON Interrupt Function (INTOUT)

The Touch-ON interrupt function is a function to notify the microcontroller that the touch judgment result is set to “ON”. It is possible to change the state of the microcontroller by interrupt. When the touch judgment result has been “OFF” for a long time, the state of the microcontroller can be changed to sleep mode. When the touch judgment result changes to “ON”, the microcontroller

can be waked up by the Touch-ON Interrupt by carrying out such control, power consumption of your products may be lower.

Interrupt signal (INTOUT) has the function to notify the microcontroller of operating conditions of the LSI elsewhere of the Touch-ON interrupt function. When interrupt input of the microcontroller side is used, not the level detection, please use the edge detection.

The output mode of interrupt signal (INTOUT) at the time of the measurement processing sets to the INTMD1−INTMD2 bits in the Measurement 1 Mode Register [Address=0x3A].

The conditions that interrupt signal (INTOUT) does assert (“High”) are as follows.

- When this LSI completes the initialization processing.
- When the IntOut bit in the Control 2 Register [Address=0x40] is set to “1”.
- When the INTMD1 bit in the Measurement Mode 1 Register [Address=0x3A] is set to “0”, whenever the measurement was completed, INTOUT is asserted.
- When the INTMD1 bit in the Measurement Mode Register [Address=0x3A] is set to “1”, INTOUT signal is asserted as follows: Only when the measurement was completed, and at least one channel is the touch ON judgment state, INTOUT is asserted.
- When the dynamic offset calibration was carried out. At this time, the DyCalAck bit in the Control 2 Register [Address=0x40] becomes “1”. Therefore, the microcontroller can confirm normal measurement operation or dynamic offset calibration was carried out by reading Control 2 Register [Address=0x40].
- In addition, when static offset calibration has been completed, INTOUT is not asserted.

The conditions that interrupt signal (INTOUT) does negate (“Low”) are as follows.

- When reset of this LSI was canceled.
- When the microcontroller sets the IntOut bit in the Control 2 Register [Address=0x40] to “0” during interval processing (In the case of interval mode) or during sleep period (In the case of sleep mode).
- When the INTMD2 bit in the Measurement Mode 1 Register [Address=0x3A] is set to “1” in the case of interval mode, this LSI automatically negates INTOUT immediately after the end of interval processing. When the INTMD2 bit in the Measurement Mode 1 Register [Address=0x3A] is set to “1” in the case of sleep mode, this LSI automatically negates INTOUT immediately after the microcontroller wakes up this LSI.
- When LSI completed changing parameters processing after the WriteReq bit and ParaCh bit in the Control 1 Register [Address=0x2F] were set to “1”.

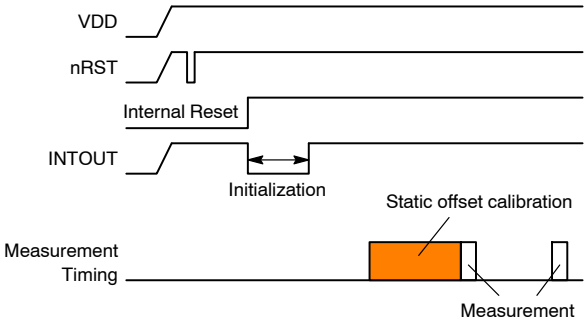


Figure 3. INTOUT Signal Timing at the Time of the Initialization

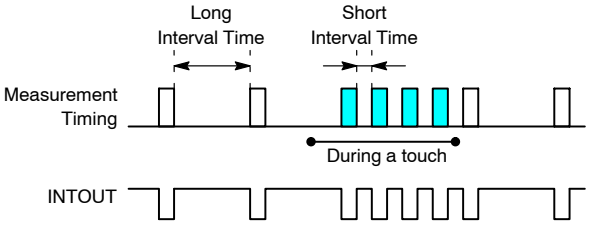


Figure 4. INTOUT Signal Timing at the Time of the Measurement (INTMD1 = “0”, INTMD2 = “1”)

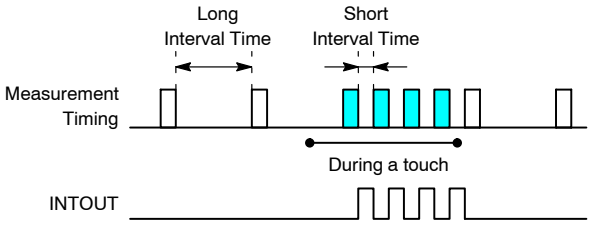


Figure 5. INTOUT Signal Timing at the Time of the Measurement (INTMD1 = “1”, INTMD2 = “1”)

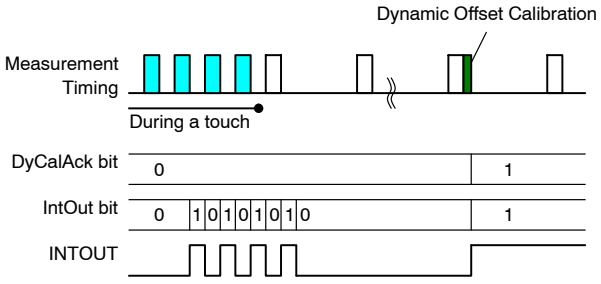


Figure 6. INTOUT Signal Timing at the Time of the Dynamic Offset Calibration Operation (INTMD1 = “1”, INTMD2 = “1”)

Reset Function (nRST)

In order to use POR(power on reset) function built into the LC717A30, you need to fix nRST pin to V_{DD}. Don't set nRST to open. However, the characteristics of power-on waveform has to follow as defined in specification. If supply to V_{DD} is unstable or waveform at power supply cannot meet specification, you can either control nRST pin from GPIO in the microcontroller or use external power-on reset circuit (Capacitor + Resistor + Diode). If high reliability is required, we do not recommend using POR function.

Moreover, in order to prevent malfunction by a noise, we recommend attaching the capacitor for noise rejection between nRST and V_{SS}. During reset, each pin of this LSI becomes High impedance (Hi−Z). For this reason, due to external effects: such as noise, if intermediate electric potential across input, the current will flow. If this is a normal reset period and is only temporary, it will cause no problem. However, do not set the reset pin (nRST) to low for a longer period then it takes to energize V_{DD}.

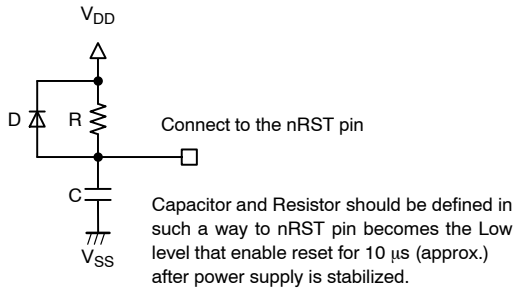


Figure 7. External Power-on Reset Circuit

How to Suppress the Influence of a Noise

1. Filter Processing
   The LC717A30 removes a noise by filter processing to increase foreign noise immunity. The LSI carries out this function inside automatically.
   This LSI has a Digital Offset Abnormality Alarm Flag Function. When this LSI carried out the static offset calibration, and an AD level became big by interference of frequency of the foreign noise and the filter processing, the DALM1 and DALM0 bits in the Error Status Register [Address=0x2C] are set by this function. Thus, this LSI notifies the microcontroller that a normal measurement result may not be provided.
2. Noise (In-phase Noise) Immunity
   Error detection likely occurs as the noise level increases due to external cause when without touch. Our LSI incorporates differential-input CV amplifier in electrostatic capacitance detection circuit. When external noise gets into two differential input pins (CinX(=Cin0 to Cin7), Cref), the noise is suppressed by in-phase noise rejection function of the CV AMP (in-phase noise rejection ratio: CMRR). As a result, output noise is reduced. The control of the amplifier connection configuration at the time of measurement sets to the AmpMode bit in the Control 3 Register [Address=0x2B]. When the AmpMode bit is set to "0" becomes the differential mode.

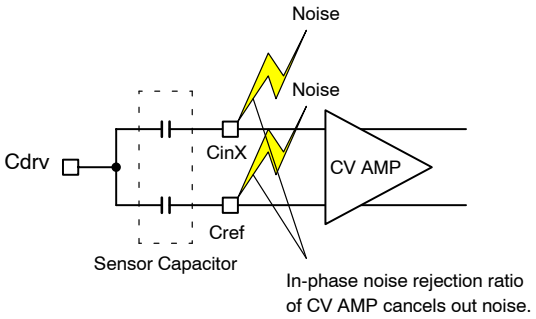


Figure 8. Noise Immunity by the Differential Mode

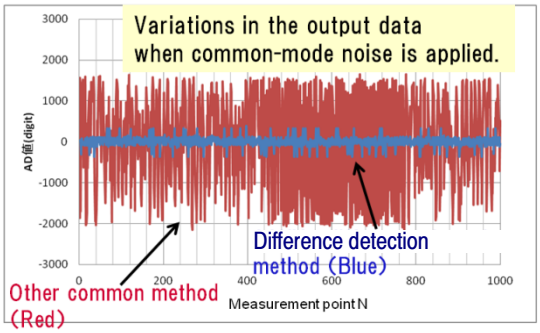


Figure 9. Variations in the Output Data When Common-mode Noise is Applied

3. Influence of the Switching Noise
   In the case of the application that reading or writing may be carried out from the microcontroller with serial interface (I^2C bus or SPI) in measurement time, we recommend the connection of the dumping resistor (about 10 Ω to 1 kΩ) in the interface signal line to reduce the influence of the switching noise of the interface signal (nCS, SCL/SCK, SDA/SI and SA0/SO). Please evaluate an actual circuit, and decide a value of the dumping resistance to meet input specifications of the LSI.

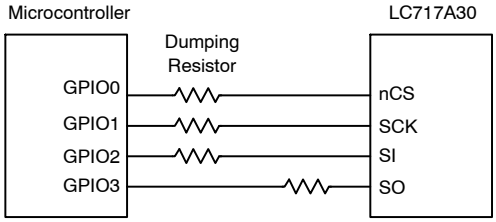


Figure 10. Connection Example with the Microcontroller (SPI)

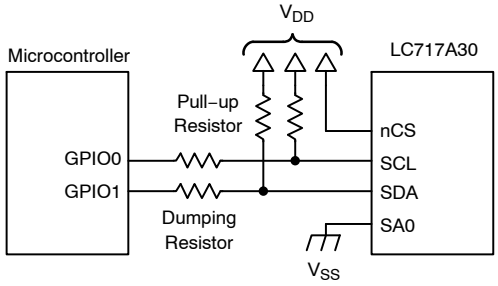


Figure 11. Connection Example with the Microcontroller (I^2C)

4. Communication With I^2C Bus or SPI
   We recommend verification of data (Reading or writing from the microcontroller with serial interface (I^2C bus or SPI)) for communication fault detection. (However, since Control 1 Register [Address=0x2F] and Control 2 Register [Address= 0x40] change a value automatically, it cannot verify) Moreover, if the communication fault by a noise is anxious, we recommend using SPI interface. (The IFSEL pin is fixed to Low(V_{SS}) level)
   When the I^2C bus is used, the SCL and SDA signal lines need a pull-up resistor. The pull-up resistor is not contained in LC717A30. Please be sure to connect the pull-up resistor of SCL and SDA to VDD and use neither nodes other than VDD. In addition, please don't use the pull-up resistor built into the microcontroller.
5. ESD (**E**lectro-**S**tatic **D**ischarge)
   The touch sensor is completely insulated from the human body. Therefore, this LSI has the ESD tolerance that is higher than a general machine switch. Moreover, when ESD tolerance becomes a problem, arranging the resistance for the following surge current restrictions in series on Cin0 to Cin7, Cref, Cdrv and CdrvBar lines will help improve ESD tolerance. Please attach current-limiting resistors of 1 kΩ near the LC717A30.

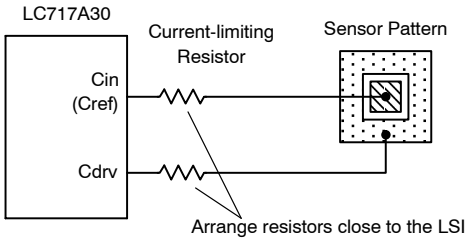


Figure 12. Connection Example of the Current-limiting Resistors

6. EMI (**E**lectro **M**agnetic **I**nterference)
   If the antenna of radio is brought close to a switch pattern, noise sound can be heard from radio. This is caused by a 121 kHz (Typ) rectangular wave that are outputted from the Cdrv and CdrvBar pins. The rectangular waves of Cdrv and CdrvBar contains 121 kHz fundamental waves and many harmonics which is an odd multiple of 121 kHz.
   When the above-mentioned harmonics become a problem as EMI, it is possible to reduce harmonics by adding a CR low pass filter to Cdrv and CdrvBar.

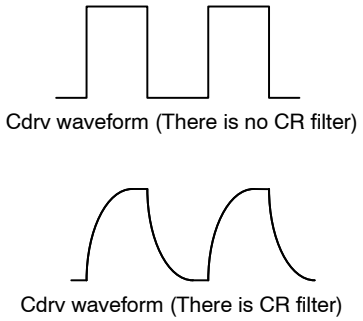


Figure 13. Cdrv Waveform by the LPF Addition

Recommended values of CR low pass filter: Resistance (R) = 1 kΩ, Capacitance (C) = 500 pF or less. However, the parasitic capacitance value between Cdrv and GND of a sensor pattern is also included in 500 pF of Capacitance (C).

The parasitic capacitance value between Cdrv and GND of a sensor pattern can be calculated by the same method as calculating parallel monotonous capacitor capacity.

For example,

- thickness of the two-layer board: d = 1.6 mm,
- Gross area of Cdrv (of a sensor pattern): S = 25 cm^2,
- Non-dielectric constant of a substrate: $\varepsilon_r = 4.3$,
- Dielectric constant under a vacuum:
  $\varepsilon_0 = 8.854 \times 10^{-12}$ Fm^{-1}

$$C_{Cdrv-GND} = \epsilon \cdot \epsilon_0(S/d)$$
$$= 4.3 \times (8.854 \times 10^{-12}) \times (0.0025/0.0016)$$
$$= 60\ pF$$

From the above-mentioned calculation, capacity to be added becomes less than 440 pF (= 500 pF − 60 pF) between Cdrv and GND.

In case there is already R (1 kΩ) of current-limiting resistor for ESD, R (1 kΩ) of CR low pass filter for EMI is unnecessary. In the case of quadratic filter, recommended values are R = 500 Ω and C = 330 pF or less.

Detection Sensitivity

1. Setting Method of Sensitivity
   The sensitivity adjustment is very important for noise tolerance. Sensitivity changes with the size of a finger. We recommend carrying out sensitivity adjustment using various fingers with varied age and gender. In order to prevent malfunction of the dynamic offset calibration, when switch is not being touched, the noise level needs to be always below a value of the lower limit AD level of the plus level

side, or the noise level needs to be always above a value of the upper limit AD level of the minus level side of the dynamic offset calibration operating range of the Dynamic OffCal Threshold Register [Address=0x01].

For more information about the control example with the microcontroller, refer to "In the case of the sensitivity adjustment", and please enforce the sensitivity adjustment by all means.

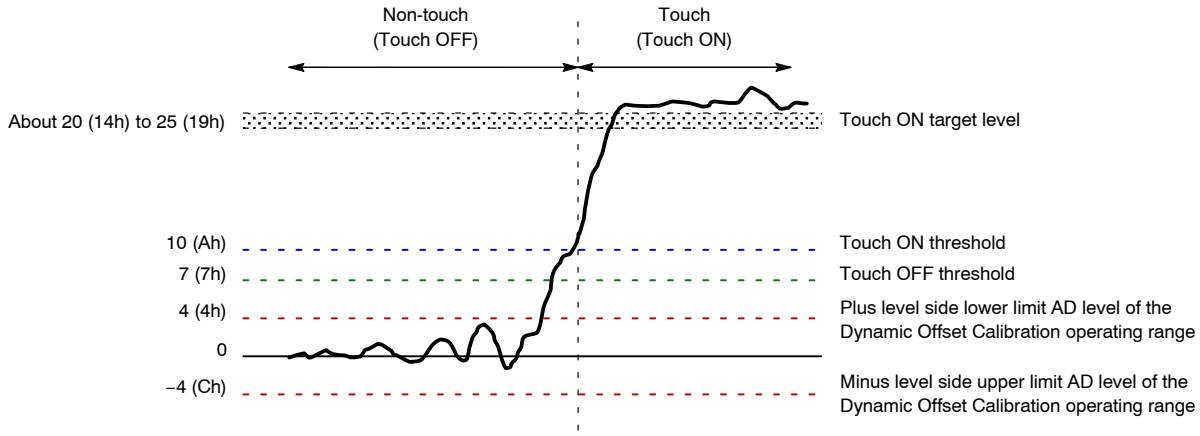


Figure 14. Setting Example of the Sensitivity Adjustment (1)

2. Mobile Devices Which Use a Battery
   The touch sensitivity that uses a battery falls compared to those that use an AC power supply. While a battery is being used the mobile device becomes a floating field to GND. For this reason, adjust sensitivity accordingly.
3. Influence of Parasitic Capacitance
   The sensitivity of a sensor falls as the parasitic capacitance between Cin and GND (or between Cin and Cin) increases. The following measure is mentioned in order to prevent the fall of sensitivity.
   a. Distance between Cin and GND (or between Cin and Cin) is lengthened.
   b. Wiring distance of Cin is shortened.

   When the MCIN1 and MCIN0 bit in the Measurement Mode 1 Register [Address=0x3A] were set to "0" and those register values are reflected inside the LC717A30 by changing parameters, a Cin is being fixed to GND (V_{SS}) except the time of measurement. Therefore, the capacity between Cin and GND and the capacity between Cin and Cin become the same meaning.
   When the above-mentioned measures are difficult, respond by setting up a higher gain. In this case, S/N of a sensor gets worse. In the case where touch switch is placed in a severe noise environment, cautions are required.
   When wiring of Cin is long, please prevent a drop of the sensitivity by extending distance between Cin and GND (Distance between Cin and Cin is included) as much as possible.
4. Influences When Backside of the Switch Pattern is all GND
   When GND is placed on the backside of Cin, a part of electrical flux lines between Cin and Cdrv are terminated to the backside of all GND. Therefore, if the distance of Cin and backside of all GND is small, touch detection sensitivity falls. However, we recommend back side all GND. This reason is for suppressing the influence of an exogenous noise.

Reference Capacitance (Cref/CrefAdd)

1. How to Design of the Reference Capacitance (Cref) Pattern
   The LC717A30 needs sensor pattern connected to Cin and also reference pattern connected to Cref. With Cref pattern, you can use the same tile as used with Cin.
   If you arrange Cref on the top layer of the board, the electrical flux line between Cref and Cdrv may be intercepted when a surface panel is touched, and the reference capacity may be altered.
   A solution to the above-mentioned problem, Cref pattern is arranged on the bottom layer, and top layer except over Cref is covered with GND. In such a case, there is no electrical flux lines between Cref and Cdrv(in others words, on the front side of the board). Since the capacitance does not change when Cref is touched, the value of measured data does not change.
   In addition, since Cref pattern is not covered with GND on top layer, Cref receives the same amount of noise as Cin from front side. So, it is possible for the internal circuit of LSI to cancel these noises as common mode noise. However, please don't arrange noise source such as a switching power supply near Cref pattern because Cref is influenced by the noise from the backside of the board. In case that you can't

arrange Cref pattern without influence from noise source, or in case that you use single layer board, please connect the chip capacitor, which has almost the same capacity value as that of the tile between Cref and Cdrv, near the LSI. To learn more about chip capacitor, please refer to Figure 15 and Figure 16.

We recommend preparing PCB land pattern which attaches a chip capacitor together, even when using Cref pattern. In addition, we recommend preparing CrefAdd's PCB land pattern for a chip capacitor. When a chip capacitor between CrefAdd and Cdrv is connected and the CIN4CINP2 or CIN0CINP2 bit in the Measurement Mode 2 Register [Address=0x3B] was set to "1" and those register values are reflected inside the LC717A30 by changing parameters, the measurement processing using both Cref and CrefAdd is carried out. If Cref pattern catches a lot of noise, cut Cref line and attach a chip capacitor between Cref and Cdrv (or between CrefAdd and Cdrv).

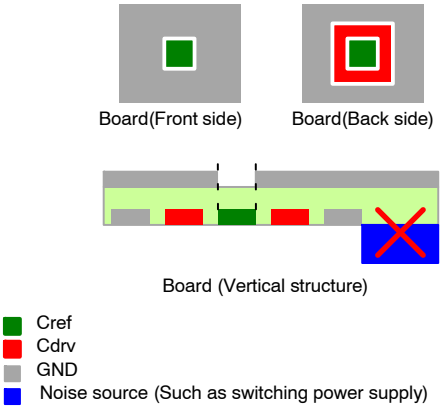


Figure 15. Design Example of the Cref Pattern (1)

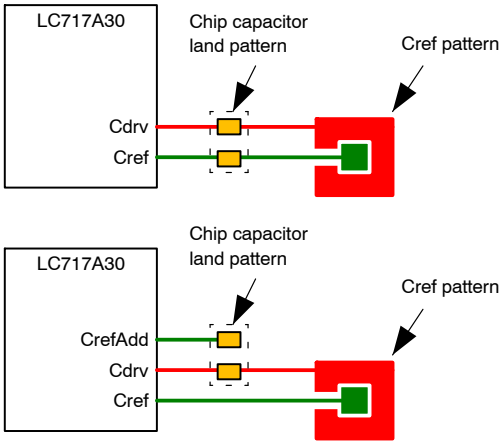


Figure 16. Design Example of the Cref Pattern (2)

2. Explanation of the Static OffCal CDAC Base Register

The value set up by the Static OffCal CDAC Base Register [Address=0x39], it is a value of reference capacity when carrying out the static offset calibration, this reference capacity value is compared with the capacity value between Cin and Cdrv (or between Cref and Cdrv) of a sensor pattern, and the measurement condition used as the standard of touch detection measurement is determined. When determining the above-mentioned measurement condition, the dynamic range of OP-Amp inside LSI is determined, and OP-Amp of the dynamic range becomes wider so that reference capacity and a capacity value between Cin and Cdrv of the sensor pattern are nearer. Since the characteristic of touch detection will improve if the dynamic range of OPAmp becomes large, it recommends that the Static OffCal CDAC Base Register [Address=0x39] carries out the optimal setup to the capacity value between Cin and Cdrv.

Even though static offset calibration is performed, when reference value (The origin of the measurement) does not correspond with the middle of measurement range, change this value. The optimal preset value of the Static OffCal CDAC Base Register [Address=0x39] changes with capacity (when two or more sensor patterns are connected to one Cin, it is total capacity value) between Cin and Cdrv. Don't set any value but 20h, 40h, 80h. The initial value is 80h. It shows 4 pF.

Please set the following as reference.

- When a capacity value between Cin (Cref) and Cdrv is larger than 2 pF, this 0x39 register is set to 80h (4 pF).
- When a capacity value between Cin(Cref) and Cdrv is larger than 1 pF and is less than 2 pF, this 0x39 register is set to 40h (2 pF).
- When a capacity value between Cin(Cref) and Cdrv is less than 1 pF, this 0x39 register is set to 20h (1 pF).

However, when the sensor pattern with which a size is different for every Cin is being used, please consider the above to the capacity value between largest Cin and Cdrv.

For example, when a 1.5 pF sensor pattern and a 5 pF sensor pattern are being used, please set up 80h.

Measurement Function

Explanation of the Touch Judgment

1. The State That a Touch is Detected (Touch State)
   Even if all Cin0ACT to Cin7ACT bits in the Result Data Register [Address=0x2A] become “0” (All channels are touch OFF judgment), this state means “the measurement data of one or more enabled channels are greater than or equal to the touch ON threshold set in the Cin0 to Cin7 ON Threshold Register [Address=0x0A to 0x11]”.
   When “The state that a touch was detected (Touch state)” is judged once, all use channels continue “The state that a touch was detected (Touch state)” until it is judged to be touch OFF.
   This state refers to the “All Channels No Touch Status = AllChNoTch (LSI Internal Signal)” to “0 (Touch)” in the measurement timing of Figure 18 to Figure 24. About detail description, refer to Figure 18 to Figure 24.
2. Touch ON Judgment State
   When the number of consecutive measurement points that measurement data is greater than or equal to the touch ON threshold setting with Cin0 to Cin7 ON Threshold Register [Address=0x0A to 0x11] becomes equal to the number of debounce count (OFF → ON) specified by the Debounce Count 1 Register [Address=0x32], the result of “ON/OFF” judgment changes to the “Touch ON”. When touch ON is judged, the Cin0ACT to Cin7ACT bits corresponding to each channel of Result Data Register [Address=0x2A] becomes “1”.
3. Touch OFF Judgment State
   When the number of consecutive measurement points that measurement data is less than the touch OFF threshold setting with the Cin0 to Cin7 OFF Threshold Register [Address=0x12 to 0x19] becomes equal to the number of debounce count (ON → OFF) specified by the Debounce Count 2 Register [Address=0x33], the result of “ON/OFF” judgment changes to be “Touch OFF”. When touch OFF is judged, the Cin0ACT to Cin7ACT bits corresponding to each channel of Result Data Register [Address=0x2A] becomes “0”.
4. The State That a Touch is not Detected (Non-touch State)
   This state means “all use channels (The Cin0EN to Cin7EN bits in the Use Channel Register [Address= 0x00] were set to “1”) become the touch OFF judgment”. However, it changes into “The state that a touch is not detected (Non-touch state)” immediately if measurement data more than the touch ON threshold set in the Cin0 to Cin7 ON Threshold Register [Address=0x0A to 0x11] are once even if it is touch OFF.
   This state refers to the “All Channels No Touch Status = AllChNoTch (LSI Internal Signal)” to “1 (Non-touch)” in the measurement timing of Figure 18 to Figure 24. About detail description, refer to Figure 18 to Figure 24.

Explanation of the Threshold Setting

The LC717A30 can set the touch ON threshold, the touch OFF threshold, the dynamic offset calibration enforcement count number of plus level side and the dynamic offset calibration enforcement count number of minus level side.

The touch ON threshold can be set in the Cin0 to Cin7 ON Threshold Register [Address=0x0A to 0x11], and the touch OFF threshold can be set in the Cin0 to Cin7 OFF Threshold Register [Address=0x12 to 0x19], and the dynamic offset calibration enforcement count number of plus level side can be set to the DCalTHP0 to DCalTHP3 bits in the Dynamic OffCal Threshold Register [Address=0x01], and the dynamic offset calibration enforcement count number of minus level side can be set to the DCalTHM0 to DCalTHM3 bits in the Dynamic OffCal Threshold Register [Address= 0x01].

When register values written with the microcontroller at this time, reflected inside the LC717A30 by changing parameters, the following processing changes. When register values written with the microcontroller at this time, reflected inside the LC717A30 by changing parameters (by the ParaCh bit in the Control 1 Register [Address=0x2F] is set to “1”), the following processing changes.

The setting relation of these thresholds are as follows.

Touch ON Threshold	>	Touch OFF Threshold
Touch OFF Threshold	>	Plus Level Side Lower Limit AD Level
Plus Level Side Lower Limit AD Level	>	0
0	>	Minus Level Side Upper Limit AD Level

In addition, when the touch ON threshold of the Cin0 to Cin7 ON Threshold Register [Address=0x0A to 0x11] is smaller than the touch OFF threshold of the Cin0 to Cin7 OFF Threshold Register [Address=0x12 to 0x19], the touch OFF threshold is the same value as the touch ON threshold of the Cin0 to Cin7 ON Threshold Register [Address= 0x0A to 0x11].

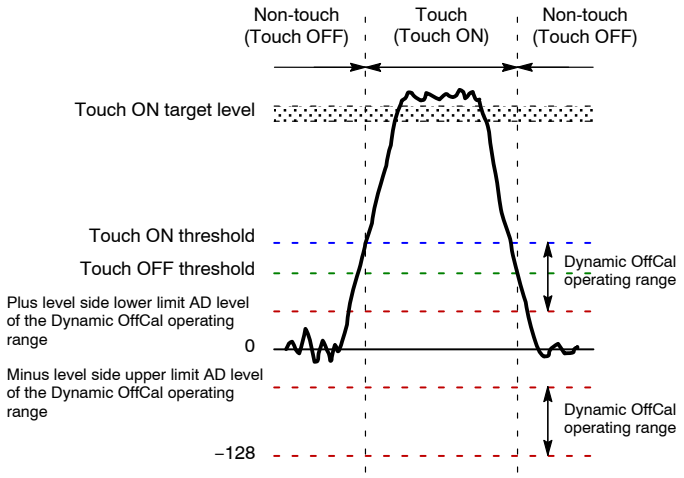


Figure 17. Relations of the Threshold Setting

Relation Between Measurement Timing and Long Interval/ Short Interval Setting

For example, the following schematic view shows the measurement timing when this LSI operates with the next settings.

In the following figures, the measurement points where the measurement data is greater than or equal to the touch ON threshold are shown as a light-blue box, the measurement points where the measurement data is less than the touch OFF threshold are shown as a white box.

The values from Cin0ACT to Cin7ACT (Touch ON/OFF Status) in the figure is reflected to the corresponding bit in the Result Data Register [Address=0x2A]. Both “AllChNoTch” (All Channels No Touch Status) and “LongItvl” (Long Interval Mode Status) in the figures are the status this LSI has inside itself.

Table 4. REGISTER SETTING IN THE SCHEMATIC VIEW OF THE MEASUREMENT TIMING

Register Name	Setting Value	Setting Contents
Use Channel Register [Address=0x00]	FFh	Use channel: 8 channels from Cin0 to Cin7
Average Count Register [Address=0x30]	40h	Initial value. One measurement time: Approximately 17 ms (Typ)
Filter Parameter Register [Address=0x31]	02h	Initial value.
DmCyc bit in the Measurement Mode 1 Register [Address=0x3A]	“0”	Initial value. Dummy cycle: 4 cycles
Debounce Count 1 Register [Address=0x32]	02h	Debounce count(OFF → ON): 3 counts
Debounce Count 2 Register [Address=0x33]	02h	Debounce count(ON → OFF): 3 counts
Short Interval Time Register [Address=0x34]	07h	Short interval time: 7 ms (Typ)
Long Interval Time Register [Address=0x35]	07h	Long interval time: 107 ms (Typ)
LIVALB bit in the Measurement Mode 1 Register [Address=0x3A]	“0”	Long interval base time: 100 ms
Long Interval Mode Start Count Register [Address=0x3C]	01h	Measurement number of times setting until a long interval mode start: 4 points

1. Measurement Timing When Touch is not Detected for All the Enabled Channels
   When the state that all use channels which the Cin0EN to Cin7EN bits in the Use Channel Register [Address=0x00] were set to “1” became touch OFF, it changes into “The State That a Touch is not Detected (Non-touch State)”. When the state that a touch is not detected, the LSI operates with a mode in a long interval.

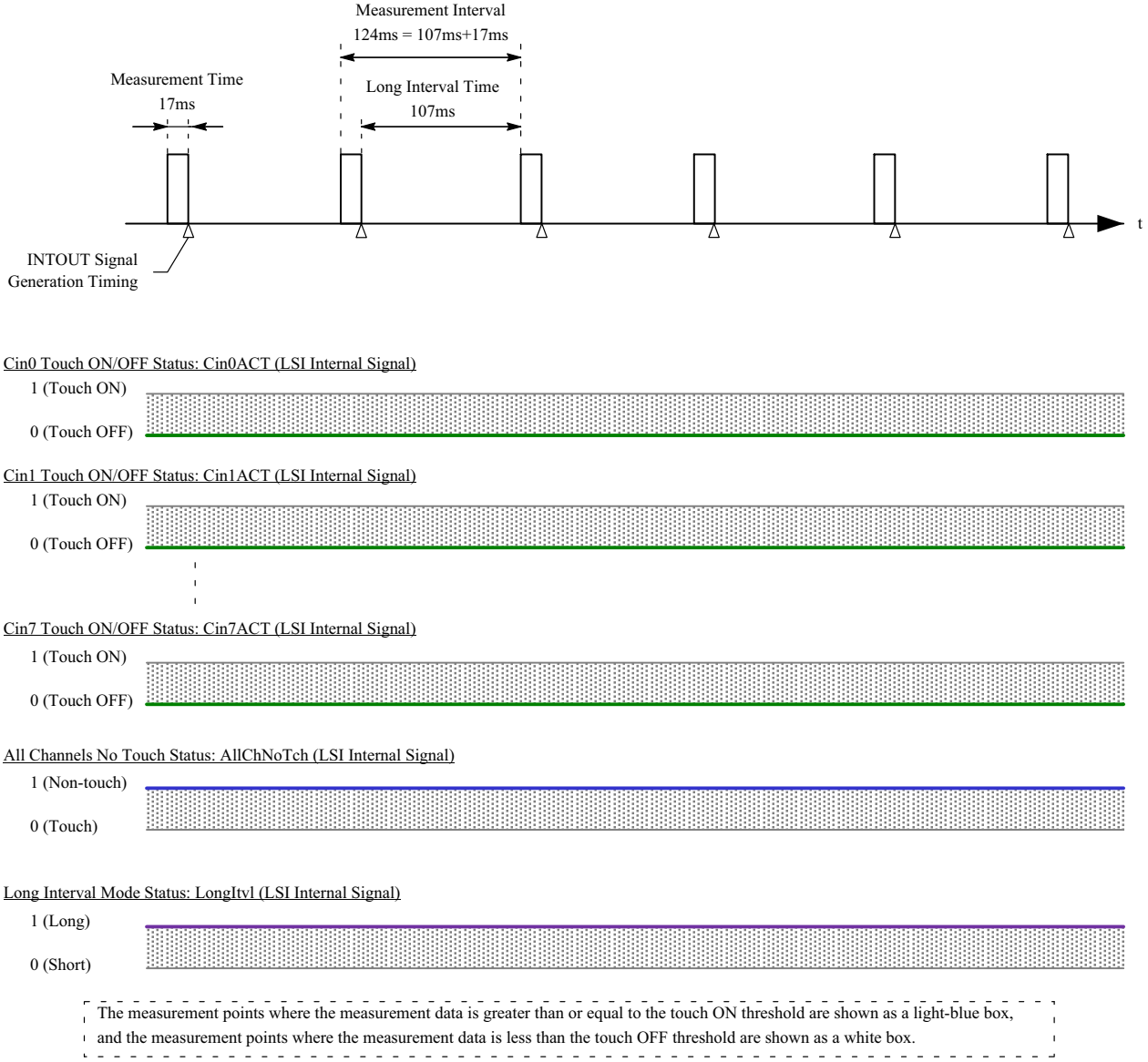


Figure 18. Measurement Timing When Touch is Not Detected for All the Enabled Channels

2. Measurement Timing Around the Time When One or more Enabled Channels Have Been Touched in the Previous State of (1.)
   If the measurement data of one or more enabled channels (The Cin0EN to Cin7EN bits in the Use Channel Register [Address=0x00] were set to “1”) are greater than or equal to the touch ON threshold, immediately it changes into “The State That a Touch is Detected (Touch State)”. At the same time, it changes into “Short Interval Mode” state.
   When the number of consecutive measurement points that measurement data is greater than or equal to the touch ON threshold setting with Cin0 to Cin7 ON Threshold Register [Address=0x0A to 0x11] becomes equal to the number of debounce count (OFF → ON) specified by the Debounce Count 1 Register [Address=0x32], its channel changes into “Touch ON Judgment State”.
   When touch ON is judged, the Cin0ACT to Cin7ACT bits corresponding to each channel of Result Data Register [Address=0x2A] becomes “1”.

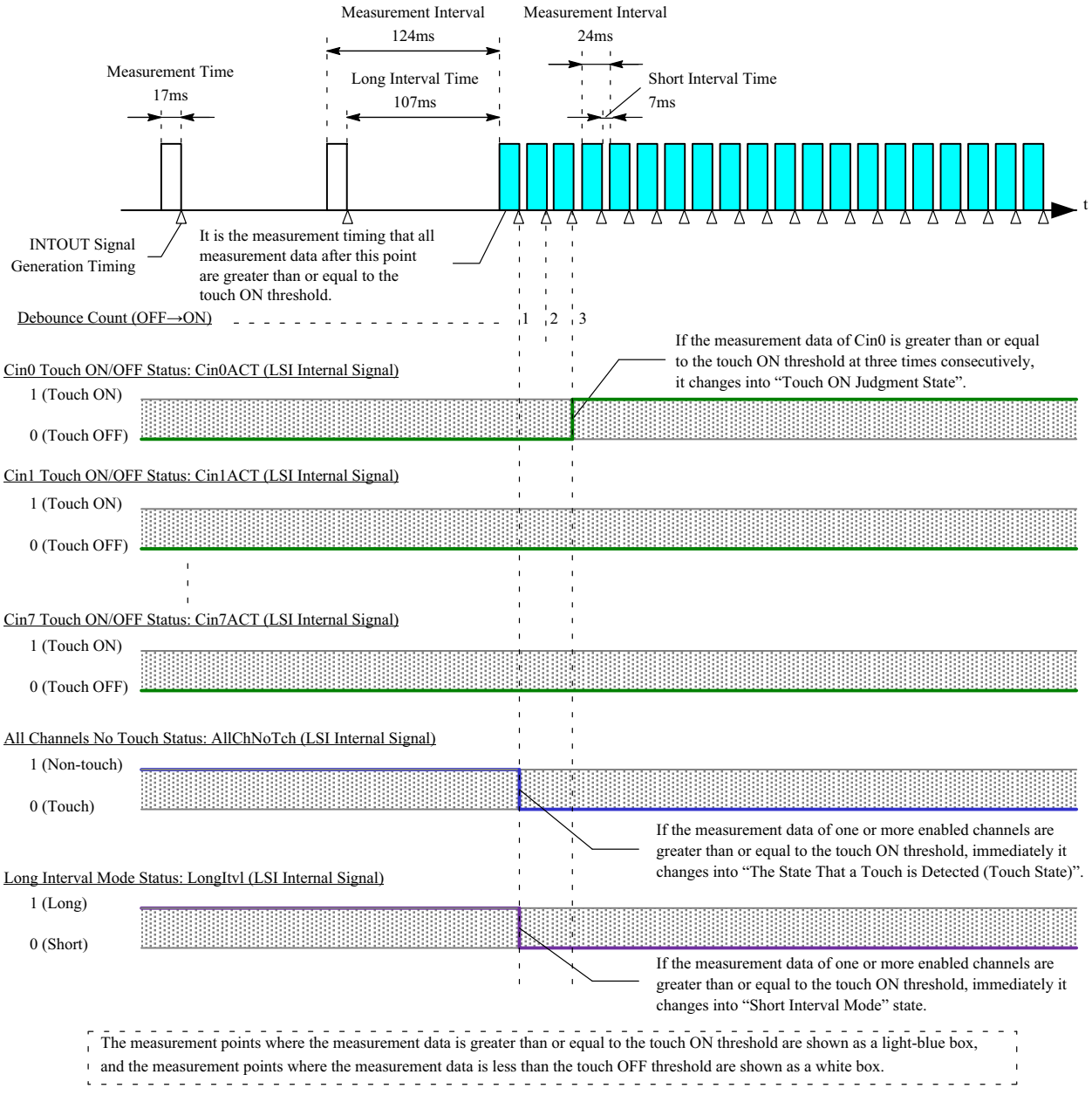


Figure 19. Measurement Timing Around the Time When One or More Enabled Channels Have Been Touched in the Previous State of (1.)

3. Measurement Timing when One or more Enabled Channels are Being Touched for a Long Time

The LSI continues operating with a mode in a short interval.

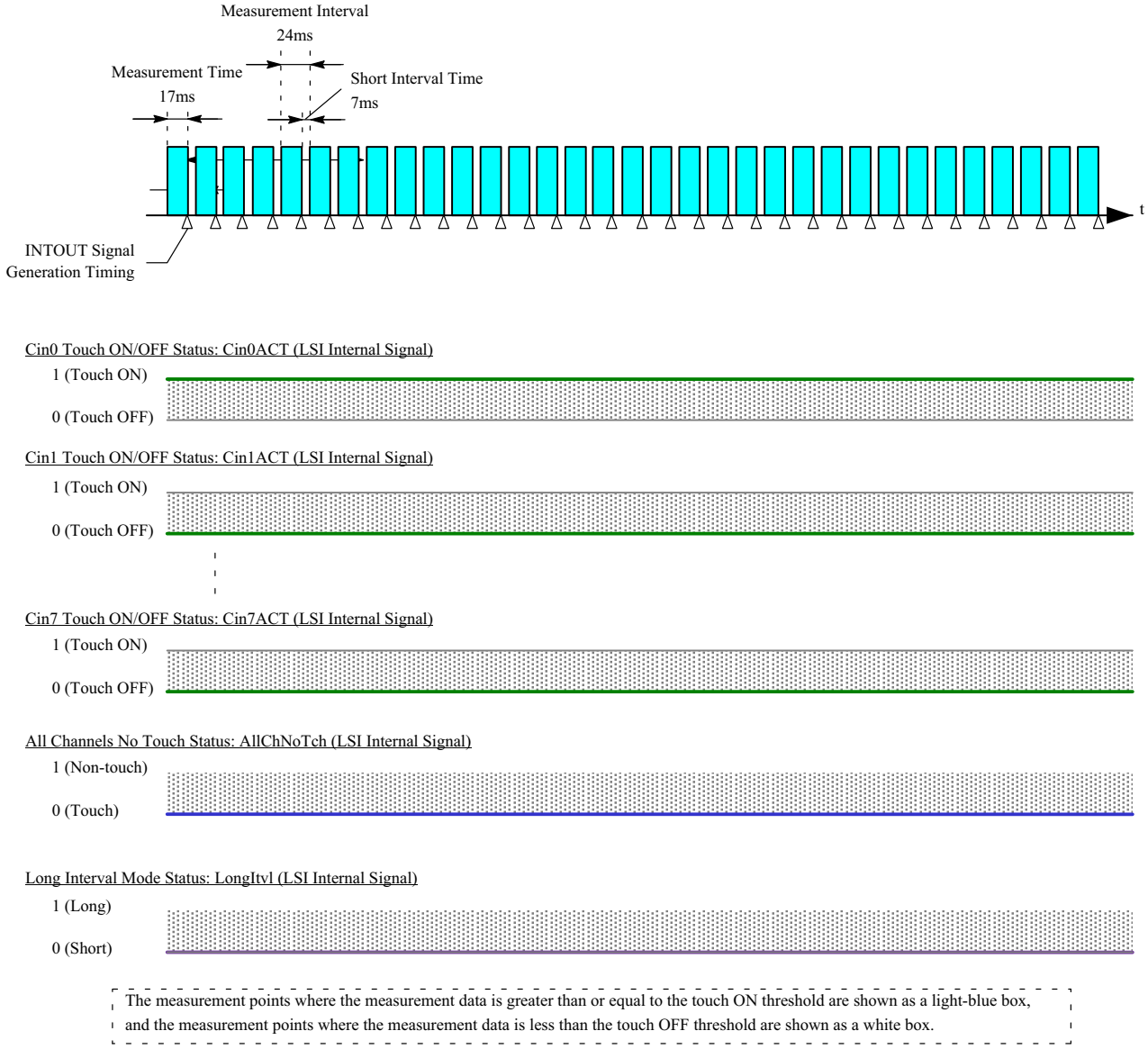


Figure 20. Measurement Timing when One or More Enabled Channels are Being Touched for a Long Time

4. Measurement Timing Around the Time when the Touch has been Released for All the Enabled Channels in the Previous State of (3.)

When the number of consecutive measurement points that measurement data is less than the touch OFF threshold setting with Cin0 to Cin7 OFF Threshold Register [Address=0x12 to 0x19] becomes equal to the number of debounce count (ON → OFF) specified by the Debounce Count 2 Register [Address=0x33], its channel changes into “Touch OFF Judgment State”. When touch OFF is judged, the Cin0ACT to Cin7ACT bits corresponding to each channel of Result Data Register [Address=0x2A] becomes “0”.

When all use channels (The Cin0EN to Cin7EN bits in the Use Channel Register [Address=0x00] were set to “1”) become the touch OFF judgment, it changes into “The State That a Touch is not Detected (Non-touch State)”.

Even if the LSI does not change into “All channels are no touch” state, immediately it does not become “Long Interval Mode”. It operates in “Short Interval Mode” to the measurement number of times until a long interval mode start set in the Long Interval Mode Start Count Register [Address= 0x3C].

If measurement data more than the touch ON threshold are once during counting the measurement number of times until a long interval mode start,

immediately it changes into “Touch ON Judgment State”. At the same time, it continue “Short Interval Mode”.

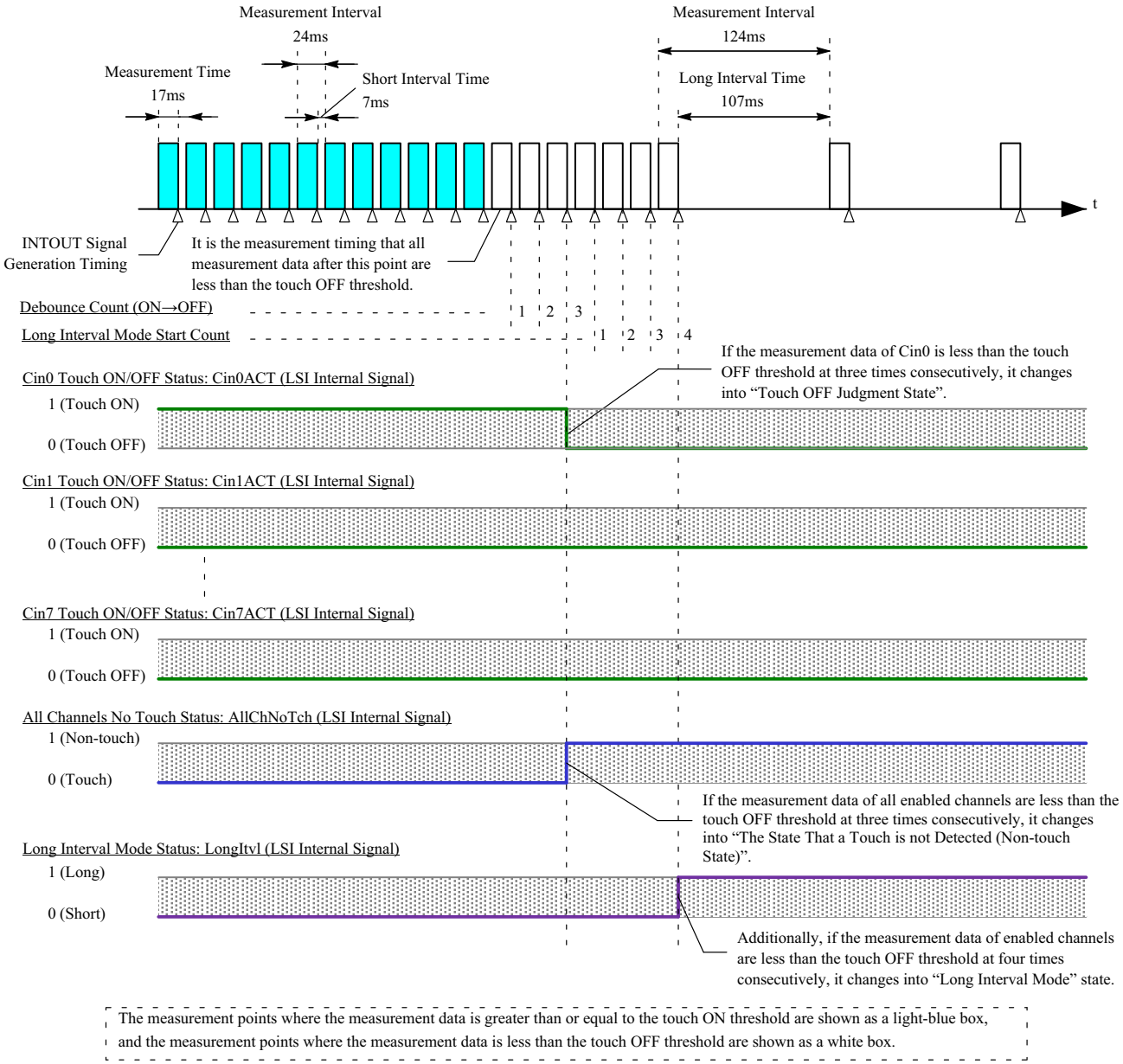


Figure 21. Measurement Timing Around the Time when the Touch has been Released for All the Enabled Channels in the Previous State of (3.)

5. Measurement Timing Around the Time When Only the Measurement Data at a Certain Measurement Point are Above the Touch ON Threshold in the Previous State of (1.).

   When only the measurement data at a certain measurement point are above the touch ON threshold, immediately it changes into “The State That a Touch is Detected (Touch State)”. At the same time, it changes into “Short Interval Mode”. At this time, it carries out a measurement in “Short Interval Mode” to points of debounce count (OFF → ON) set at least. And, when never exceed the touch ON threshold after a first measurement above the touch ON threshold, it becomes “Touch OFF Judgment State”. Furthermore, when it counts the measurement number of times until a long interval mode start, it changes into “Long Interval Mode” state.

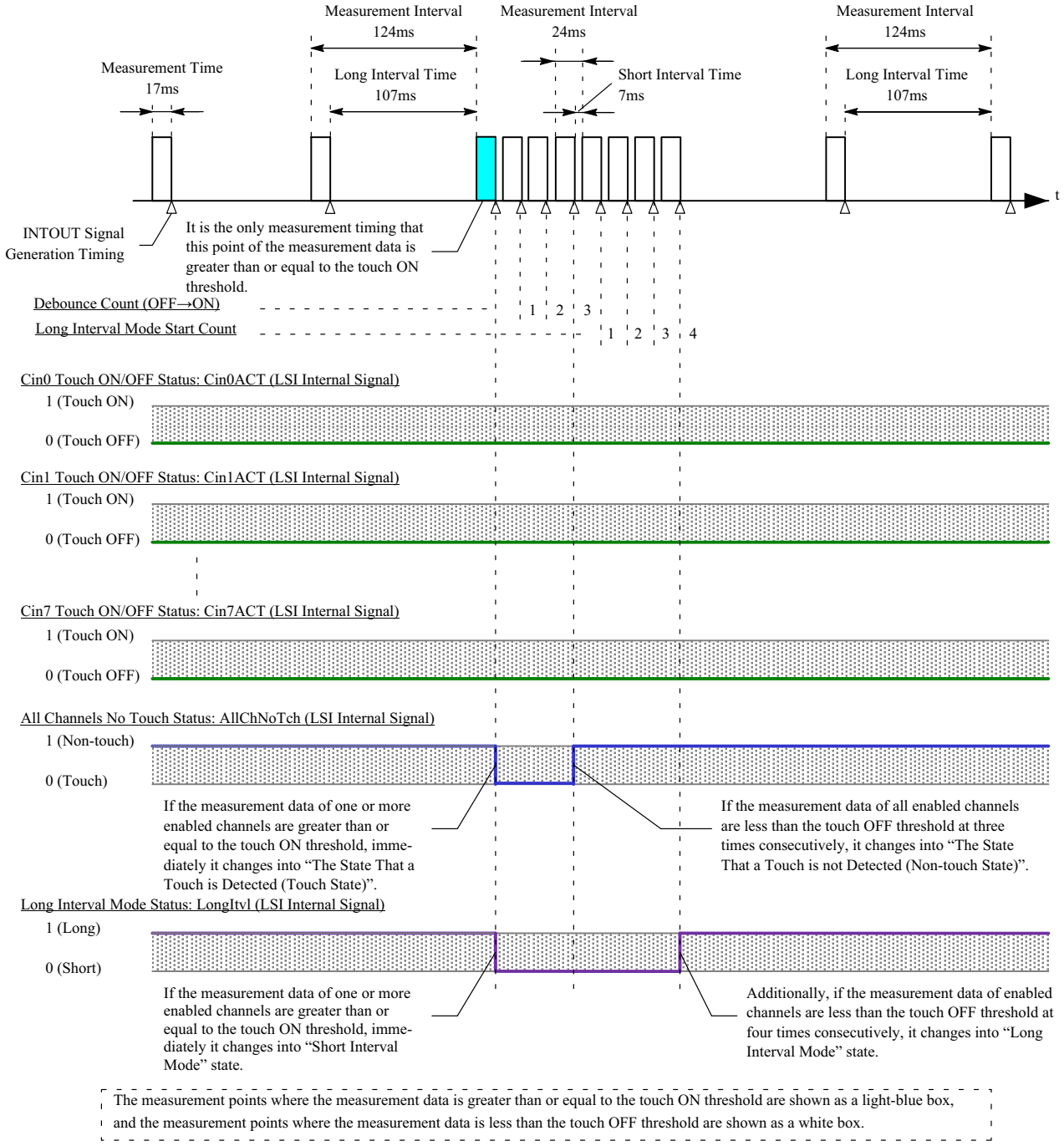


Figure 22. Measurement Timing Around the Time When Only the Measurement Data at a Certain Measurement Point are Above the Touch ON Threshold in the Previous State of (1.)

6. Measurement Timing When the Measurement Data at a Certain Channel is Affected by Chattering, etc.
The measurement timing when the measurement data at a certain measurement point exceed the touch ON threshold and the touch OFF threshold irregularly by influence of chattering, etc. is as follows. The operation explanation of the details refers to above-mentioned from (1.) to (5.).

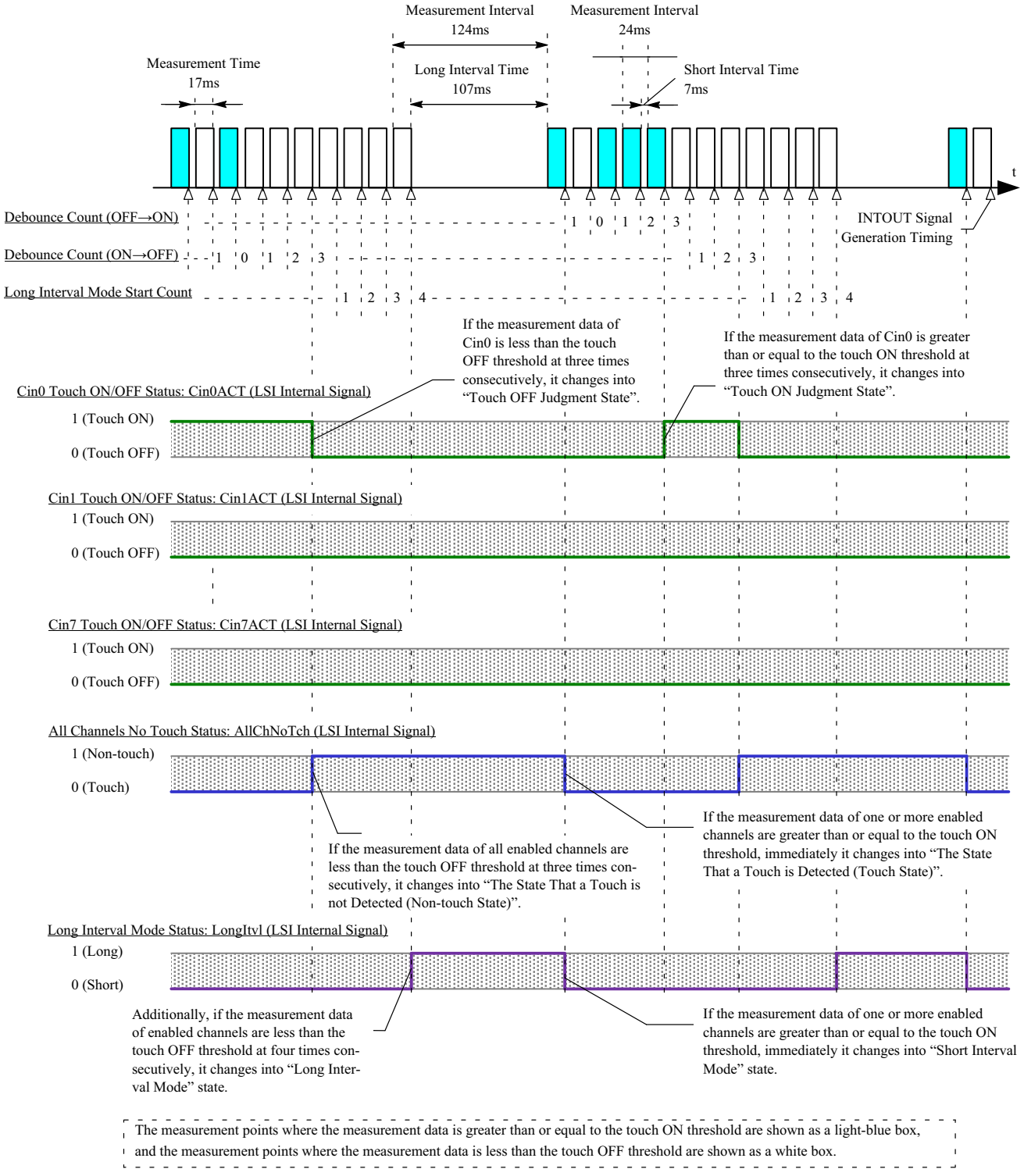


Figure 23. Measurement Timing When the Measurement Data at a Certain Channel is Affected by Chattering, etc.

7. Measurement Timing When the Measurement Number of Times Until a Long Interval Mode Start is Zero Times.
   When the measurement number of times until a long interval mode start in the Long Interval Mode Start Count Register [Address=0x3C] is set other than zero times, even if it changes into “All channels are no touch” state, immediately it does not become “Long Interval Mode”. It operates in “Short Interval Mode” to the measurement number of times until a long interval mode start set.
   However, when this setting was set to zero times and becomes “All channels are no touch” state, immediately it changes into “Long Interval Mode”. And if the measurement data more than the touch ON threshold are even once, immediately it changes into “The State That a Touch is Detected (Touch State)” state. At the same time, it changes into “Short Interval Mode” state.

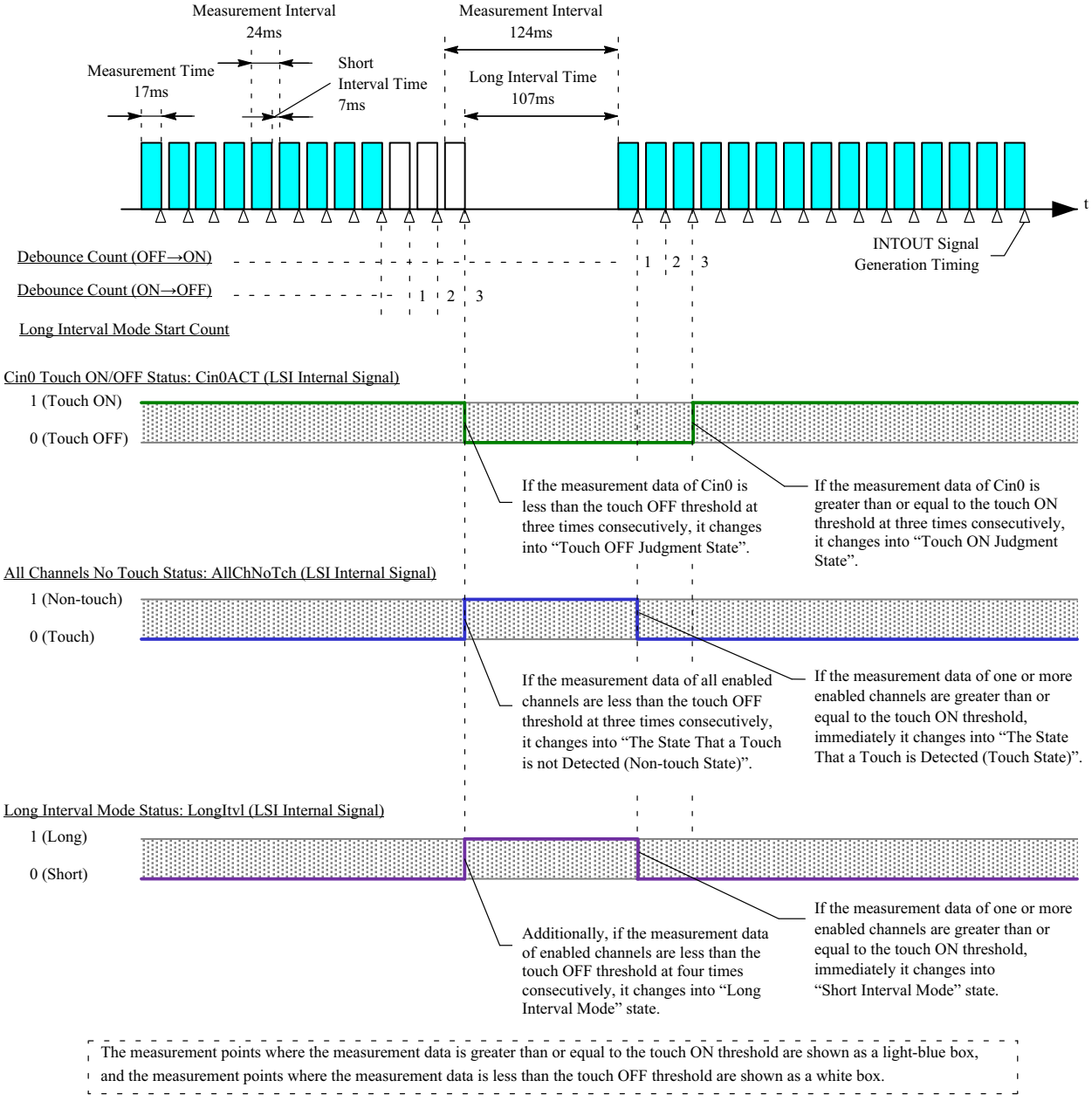


Figure 24. Measurement Timing When the Measurement Number of Times Until a Long Interval Mode Start is Zero Times

Approximate Calculation Formula of the Measurement Interval

When the register values in which a new value was set are reflected inside the LC717A30 by changing parameters, the measurement interval (Interval from a measurement to the next measurement) is changed. Measurement time is shortened by setting an unused channel to disable the channel (The Cin0EN to Cin7EN bits in the Use Channel Register [Address=0x00] were set to “0”).

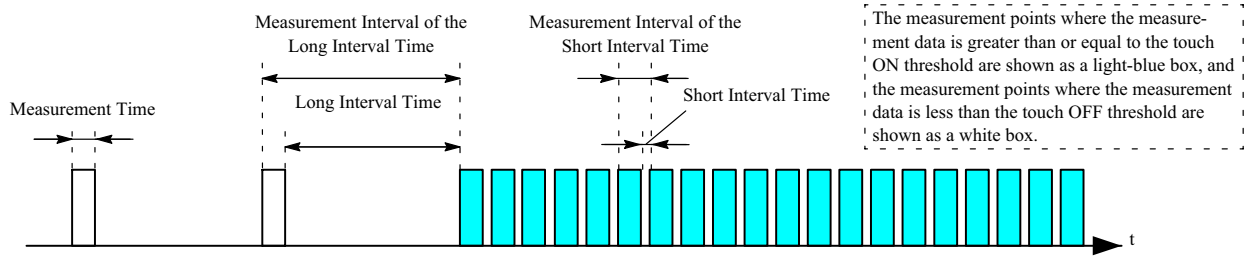


Figure 25. Measurement Interval

Approximate Calculation Formula of the Measurement Interval (Interval from a measurement to the next measurement):

Measurement Interval of the Short Interval Mode [ms](Typ)
$= \{FP1k \times (AC[7:0] + DmCyc) + 0.116 \times UseCh + 0.16\} +$ (Short interval time)

Measurement Time

Measurement Interval of the Long Interval Mode [ms](Typ)
$= \{FP1k \times (AC[7:0] + DmCyc) + 0.116 \times UseCh + 1.60\} +$ (Long interval time)

Measurement Time

AC[7:0]:	The number of measurement data average count (Average Count Register [Address=0x30])
DmCyc:	The number of dummy cycle (Measurement Mode 1 Register [Address=0x3A])
UseCh:	The number of measuring channel (Use channel in the Use Channel Register [Address=0x00])
FP1k:	Coefficient by the set value of the Filter Parameter Register [Address=0x31] In the case of FP2[3:0]=0, FP1k can be calculated by the following formula from FP1[3:0] in the Filter Parameter Register [Address=0x31]. $FP1k(Typ) = 0.02475 + (FP1[3:0] \times 0.001875)$

The measurement interval in the case of V_{DD} = 5.0 V, the number of enabling channel is 8ch and other condition is initial setting (Specifically, the number of measurement data average count is 64 times, FP2[3:0]=0h, FP1[3:0]=2h, short interval time set to 5 ms and long interval time set to 101 ms) is following. The measurement time is changed by Cdrv drive frequency f_{CDRV}.

Measurement Interval of the Short Interval Mode (Typ) = $\{(0.0285 \times (64 + 4) + 0.116) \times 8 + 0.16\} + 5.0 = 21.59$ [ms]
Measurement Interval of the Short Interval Mode (Min) = $\{16.592 \times (1/1.3)\} + 1.9 = 14.66$ [ms]
Measurement Interval of the Short Interval Mode (Max) = $\{16.592 \times (1/0.7)\} + 6.3 = 30.01$ [ms]

Measurement Interval of the Long Interval Mode (Typ) = $\{(0.0285 \times (64 + 4) + 0.116) \times 8 + 0.16\} + 101 = 117.59$ [ms]
Measurement Interval of the Long Interval Mode (Min) = $\{16.592 \times (1/1.3)\} + 40 = 52.76$ [ms]
Measurement Interval of the Long Interval Mode (Max) = $\{16.592 \times (1/0.7)\} + 125 = 148.71$ [ms]

Offset Calibration Functions

The LC717A30 is maintenance-free because the calibration function is integrated to support the aging of sensor board and the change of temperature.

Unlike tactile switch or resistor-type touch sensor, electrostatic capacitance touch sensor has no mechanical operation parts. Hence it is free of breakdown and has a long life without need of maintenance. However, if there is an air gap between surface and a board, the dust can possibly be an issue. and even if you supply V_{DD} in state which put the finger on the Touch Switch, The LC717A30 don't malfunction. That is, in other words, the touch is not detected until you release the finger from the touch switch, but you release your finger from the touch switch once, then subsequent touch detection will work correctly. That is, in other words, the touch is not detected until you release the finger from the touch switch, but you release your finger from the touch switch once, then subsequent touch detection will work correctly.

In order to prevent malfunction of the dynamic offset calibration, the Data Register (AD level) of the non-touching noise level always needs to be more than the plus level side lower limit AD level setting or less than the minus level side upper limit AD level setting in the Dynamic OffCal Threshold Register [Address=0x01]. In addition, when operating time is long (For example, it continues operating for 24 hours), we recommend initialization (The changing parameters and the static offset calibration by the Control 1 Register [Address=0x2F]) of the LC717A30 periodically for a fail-safe.

Read/Write of the CdacP/CdacM/DigitalOffset Register of all Channels

The LC717A30 can read and write from the microcontroller with the offset capacity value (CdacP/CdacM) and digital offset value of all channels which adjusts by enforcement of the static offset calibration and the dynamic offset calibration.

(The offset calibration performs offset adjustment of the capacity Digital to Analog converter for parasitism capacitance of each input channel (Cin0 to Cin7) and decides the most suitable offset level (the offset level of CDAC Plus, the offset level of CDAC Minus, and digital offset level) corresponding to each channel)

The microcontroller writes the setting corresponding to a channel targeted for Cin0 to Cin3 or Cin4 to Cin7 in the CdacSel bit of the Control 3 Register [Address=0x2B]. However, these registers are controllable with four channels at a time. When the CdacSel bit is set to "0", the microcontroller can read or write the CdacP/CdacM/DigitalOffset registers from Cin0 to Cin3. Otherwise, when the CdacSel bit is set to "1", the microcontroller can read or write the CdacP/CdacM/DigitalOffset registers from Cin4 to Cin7.

For more information about the control example with the microcontroller, refer to "In the Case of Reading and Writing of the CdacP/CdacM/DigitalOffset Registers".

Explanation of the Static Offset Calibration

The static offset calibration is processing for adjusting to a center level of the measurement range (−128 to 127) as a reference level of the each pattern and of the measured value in the non-touching state including parasitism capacitance.

When a system started, or when the StaCal bit in the Control 1 Register [Address=0x2F] was set to "1", this LSI automatically carries out dynamic offset calibration.

If it is normal use environment, the static offset calibration is completed by once processing to adjust to a center level. However, re-calibration is performed to up to three times with a worst case situation by inferior noise environment.

If a static offset calibration error occurs, the CALERR bit in the Error Status Register [Address=0x2C] is set to "1", and the bit in the Error Channel Status Register [Address=0x2D] corresponding to the channels of the error occurrence are set to "1". It is necessary to re-design a switch pattern if calibration error occurs under customer's environmental testing (with practical temperature and humidity).

Approximate Calculation Formula of the Static Offset Calibration Time

When the register values in which a new value was set are reflected inside the LC717A30 by changing parameters, the static offset calibration time is changed.

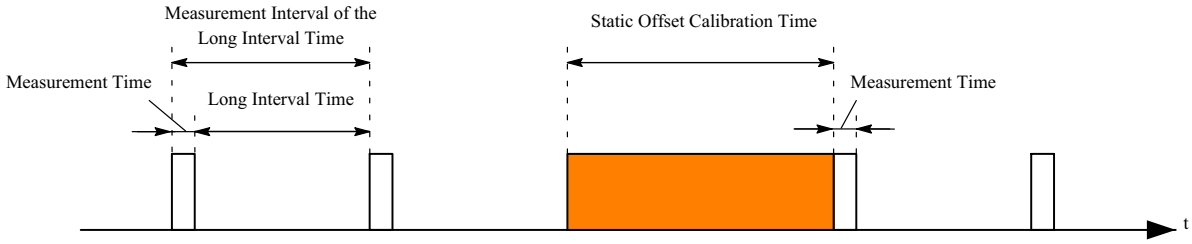


Figure 26. Static Offset Calibration Time

Approximate Calculation Formula of the Static Offset Calibration Time:

Static Offset Calibration Time of Normal Time [ms](Typ)
= ({FP1k × (AC[7:0] + DmCyc) + 0.13} × CdacBase × UseCh + 0.18

Static Offset Calibration Time When the Maximum Number of Retrying Times [ms](Typ)
= (Static Offset Calibration Time of Normal Time) × 3 + 0.6

Maximum Number of Retrying Times

Processing Time in this LSI (Except Calibration Time)

AC[7:0]:	The number of measurement data average count (Average Count Register [Address=0x30])
DmCyc:	The number of dummy cycle (Measurement Mode 1 Register [Address=0x3A])
CdacBase:	Coefficient by the set value of the Static OffCal CDAC Base Register [Address=0x39] When the reference capacity value is set to 4 pF, CdacBase is 11. When the reference capacity value is set to 2 pF, CdacBase is 10. When the reference capacity value is set to 1 pF, CdacBase is 9.
UseCh:	The number of measuring channel (Use channel in the Use Channel Register [Address=0x00])
FP1k:	Coefficient by the set value of the Filter Parameter Register [Address=0x31] In the case of FP2[3:0]=0, FP1k can be calculated by the following formula from FP1[3:0] in the Filter Parameter Register [Address=0x31]. FP1k(Typ) = 0.02475 + (FP1[3:0] × 0.001875)

The measurement interval in the case of V_{DD} = 5.0 V, the number of enabling channel is 8ch and other condition is initial setting (Specifically, the number of measurement data average count is 64 times, FP2[3:0]=0h, FP1[3:0]=2h, reference capacity is 4 pF) is following. The static offset calibration time is changed by Cdrv drive frequency f_{CDRV}.

Static Offset Calibration Time of Normal Time (Typ) = {0.0285 × (64 + 4) + 0.13} × 11 × 8 + 0.18 = 182.16 [ms]
Static Offset Calibration Time of Normal Time (Min) = 182.16 × (1 / 1.3) = 140.12 [ms]
Static Offset Calibration Time of Normal Time (Max) = 182.16 × (1 / 0.7) = 260.23 [ms]

Static Offset Calibration Time When the Maximum Number of Retrying Times (Typ) = 182.16 × 3 + 0.6 = 547.08 [ms]
Static Offset Calibration Time When the Maximum Number of Retrying Times (Min) = 140.12 × 3 + 0.6 = 420.96 [ms]
Static Offset Calibration Time When the Maximum Number of Retrying Times (Max) = 260.23 × 3 + 0.6 = 781.29 [ms]

Explanation of the Dynamic Offset Calibration

The dynamic offset calibration is the automatically processing inside the LSI to correct continuously the difference between a reference value and the median of the entire measurement data range (The difference from the median of zero), which is caused by external factors such as temperature and humidity and so on.

The microcontroller can confirm that the dynamic offset calibration was enforced by reading the Control 2 Register [Address=0x40] after having confirmed assertion (“High” level) of the INTOUT signal.

If a static offset calibration error occurs, the CALERR bit in the Error Status Register [Address=0x2C] is set to “1”, and the bit in the Error Channel Status Register [Address=0x2D] corresponding to the channels of the error occurrence are set to “1”.

The setting registers about the dynamic offset calibration are as follows.

- Dynamic OffCal Threshold Register [Address=0x01]
- Short Interval Dynamic OffCal Cycle Register [Address=0x36]
- Dynamic OffCal Count Plus Register [Address=0x37]
- Dynamic OffCal Count Minus Register [Address=0x38]
- PDCLP bit in the Measurement Mode 1 Register [Address=0x3A]
- DyCalAck bit in the Control 2 Register [Address=0x40]

The LSI can set an enforcement condition of the dynamic offset calibration by the setting combination of a register related to these dynamic offset calibrations. Enforcement condition are “Not executed”, “Executed a plus level side only”, “Executed a minus level side only” or “Executed both levels of the plus and minus”.

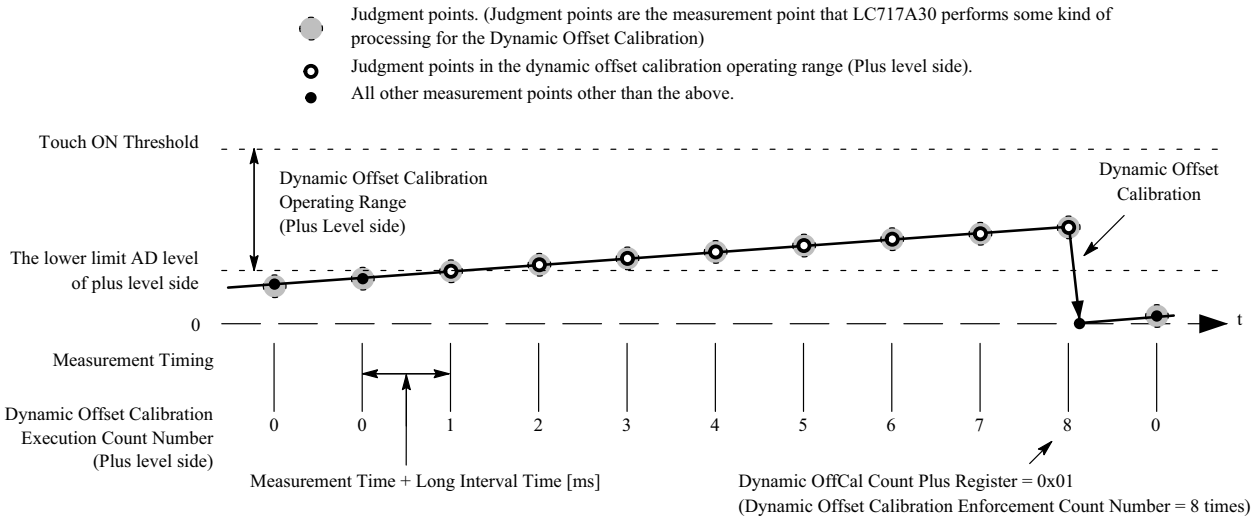
Table 5. EXECUTION CONDITIONS OF THE DYNAMIC OFFSET CALIBRATION

Register Name	Register Value			
DCalTHM0 to DCalTHM3 bits in the Dynamic OffCal Threshold Register [Address=0x01]	X	X	X	0h
DCalTHP0 to DCalTHP3 bits in the Dynamic OffCal Threshold Register [Address=0x01]	X	X	X	0h
Short Interval Dynamic OffCal Cycle Register [Address=0x36]	00h	X	X	01h to FFh
Dynamic OffCal Count Plus Register [Address=0x37]	X	00h	X	01h to FFh
Dynamic OffCal Count Minus Register [Address=0x38]	X	X	00h	01h to FFh
Execution Conditions of the Dynamic Offset Calibration	Not executed	Not executed	Not executed	Not executed

Register Name	Register Value		
DCalTHM0 to DCalTHM3 bits in the Dynamic OffCal Threshold Register [Address=0x01]	0h	1h to Fh	1h to Fh
DCalTHP0 to DCalTHP3 bits in the Dynamic OffCal Threshold Register [Address=0x01]	1h to Fh	0h	1h to Fh
Short Interval Dynamic OffCal Cycle Register [Address=0x36]	01h to FFh	01h to FFh	01h to FFh
Dynamic OffCal Count Plus Register [Address=0x37]	01h to FFh	01h to FFh	01h to FFh
Dynamic OffCal Count Minus Register [Address=0x38]	01h to FFh	01h to FFh	01h to FFh
Execution Conditions of the Dynamic Offset Calibration	Executed only the plus level side	Executed only the minus level side	Executed both levels of the plus and minus

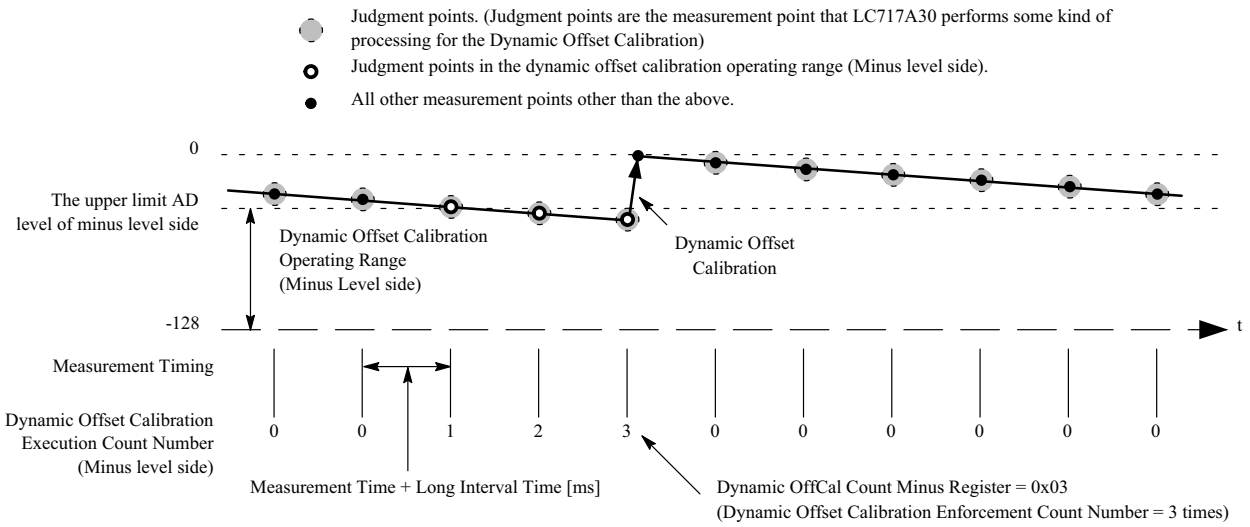
1. Dynamic Offset Calibration of the Long Interval Mode:
   When the long interval mode, the LSI judges enforcement of the dynamic offset calibration at every measurement.
   When the measurement data of the judgment processing (Judgment points) under the constant number of times specified by the Dynamic OffCal Count Plus Register [Address=0x37] continues in the dynamic offset calibration operating range (from the lower limit AD level of plus level side to the touch ON threshold), this LSI enforces the dynamic offset calibration. And when the measurement data of the judgment processing (Judgment points) under the constant number of times specified by the Dynamic OffCal Count Minus Register [Address=0x38] continues in the dynamic offset calibration operating range (from −128 to upper limit AD level of minus level side), this LSI enforces the dynamic offset calibration too.
   About the time that elapses before performing the dynamic offset calibration processing in the long interval mode is as follows.

(Measurement Time + Long Interval Time) × (Dynamic Offset Calibration Execution Counts −1) [ms]



NOTE: Either when measurement data in the judgment point is out of the dynamic offset calibration operation range or when the Dynamic Offset Calibration has been performed, the dynamic offset calibration enforcement count number of plus level side is immediately reset to “0”.

Figure 27. Example of the Dynamic Offset Calibration Processing of the Long Interval Mode (When a Measured Value Gradually Drifted From the Median in the Plus Level Direction)

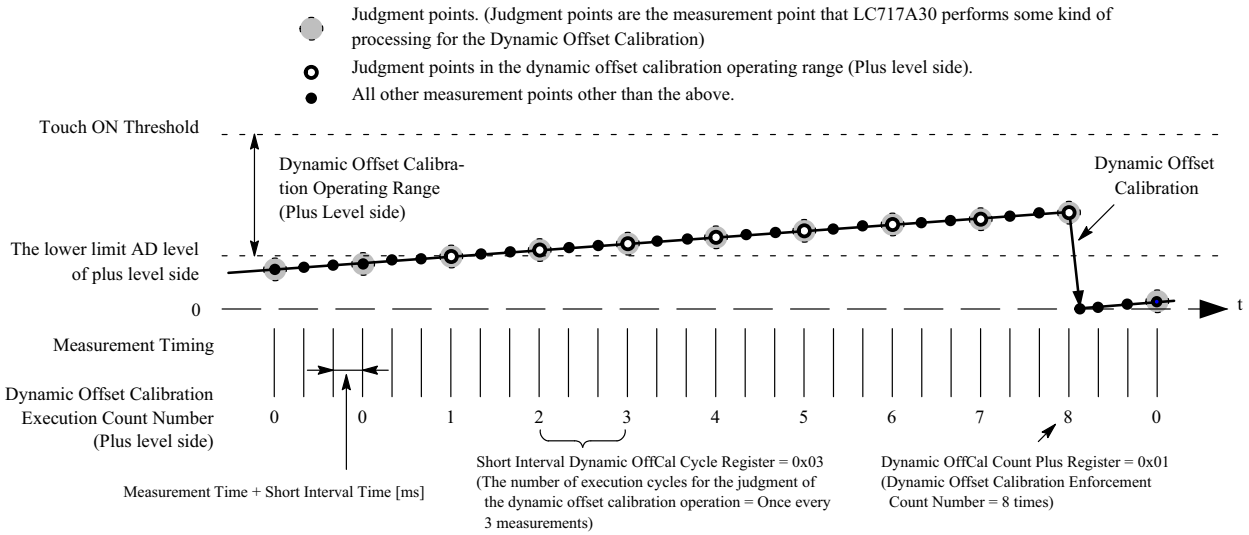


NOTE: Either when measurement data in the judgment point is out of the dynamic offset calibration operation range or when the Dynamic Offset Calibration has been performed, the dynamic offset calibration enforcement count number of minus level side is immediately reset to “0”.

Figure 28. Example of the Dynamic Offset Calibration Processing of the Long Interval Mode (When a Measured Value Gradually Drifted From the Median in the Minus Level Direction)

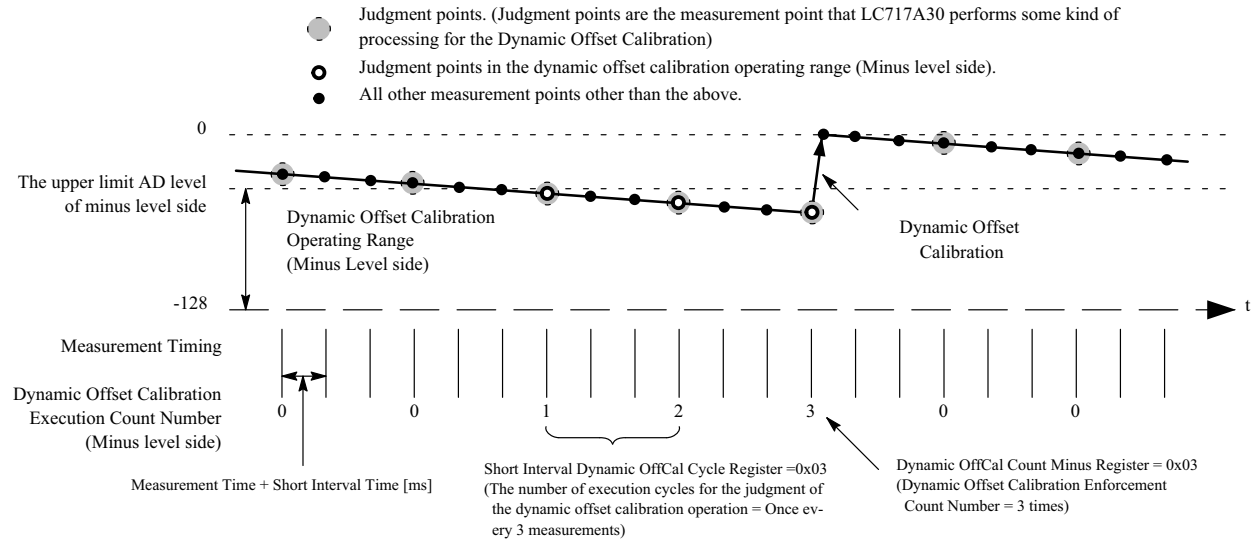
2. Dynamic Offset Calibration of the Short Interval Mode:
   When the short interval mode, the “Measurement” in the short interval time is enforced, the measurement interval shortens basically in comparison with the dynamic offset calibration at the time of the long interval mode. Therefore, the LSI judges enforcement of the dynamic offset calibration by a measurement count of the number of times that the LSI specified in the Short Interval Dynamic OffCal Cycle Register [Address=0x36].
   When the measurement data of the judgment processing (Judgment points) under the constant number of times specified by the Dynamic OffCal Count Plus Register [Address=0x37] continues in the dynamic offset calibration operating range (from the lower limit AD level of plus level side to the touch ON threshold), this LSI enforces the dynamic offset calibration. And when the measurement data of the judgment processing (Judgment points) under the constant number of times specified by the Dynamic OffCal Count Minus Register [Address=0x38] continues in the dynamic offset calibration operating range (from −128 to upper limit AD level of minus level side), this LSI enforces the dynamic offset calibration too.
   About the time that elapses before performing the dynamic offset calibration processing in the short interval mode is as follows.

(Measurement Time + Short Interval Time) × (Dynamic Offset Calibration Execution Counts −1)
× (The number of measurement points specified by Short Interval Dynamic OffCal Cycle Register) [ms]



NOTE: Either when measurement data in the judgment point is out of the dynamic offset calibration operation range or when the Dynamic Offset Calibration has been performed, the dynamic offset calibration enforcement count number of plus level side is immediately reset to “0”.

Figure 29. Example of the Dynamic Offset Calibration Processing of the Short Interval Mode (When a Measured Value Gradually Drifted From the Median in the Plus Level Direction)



NOTE: Either when measurement data in the judgment point is out of the dynamic offset calibration operation range or when the Dynamic Offset Calibration has been performed, the dynamic offset calibration enforcement count number of plus level side is immediately reset to “0”.

Figure 30. Example of the Dynamic Offset Calibration Processing of the Short Interval Mode (When a Measured Value Gradually Drifted From the Median in the Minus Level Direction)

Explanation of the Operation Flag of the Dynamic Offset Calibration

The operation flag of the dynamic offset calibration is a function to notify the microcontroller that the dynamic offset calibration was enforced When the dynamic offset calibration is enforced, the DyCalAck bit in the Control 2 Register [Address=0x40] is set to “1” at the same time IntOut bit is set to “1”, and the LC717A30 asserts (“High” level) the INTOUT signal.

The microcontroller detects the rising edge of the INTOUT, Next, reading a value of the Control 2 Register [Address=0x40]. If it was judged that the dynamic offset calibration was enforced by the DyCalAck bit in the Control 2 Register [Address=0x40] being set to “1”, the microcontroller sets the DyCalAck and IntOut bits in the Control 2 Register [Address=0x40] to “0”. In addition, the DyCalAck bit does not clear it automatically even if it becomes the mode which INTOUT signal negates automatically by the INTMD2 bit in the Measurement 1Mode Register [Address=0x3A] having been set to “1”. Please always clear DyCalAck bits by the microcontroller.

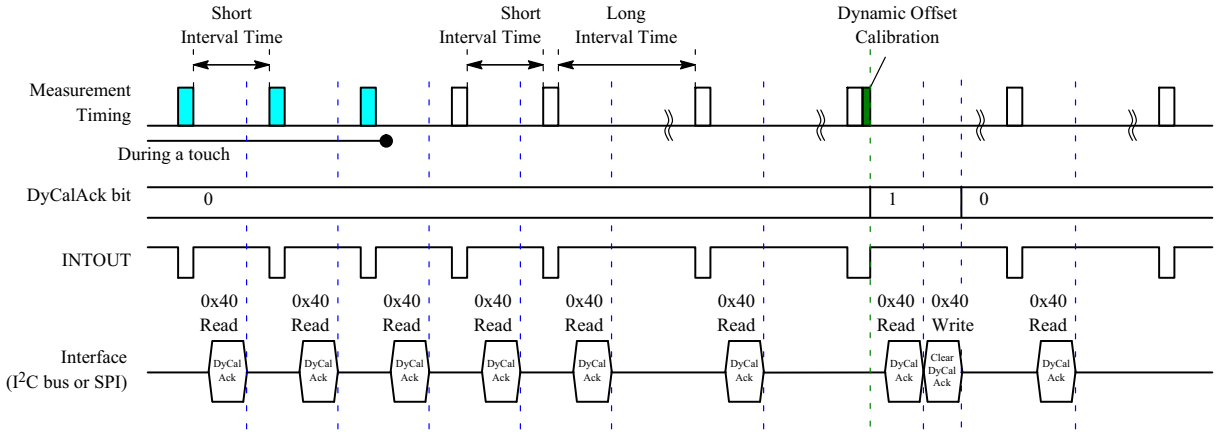
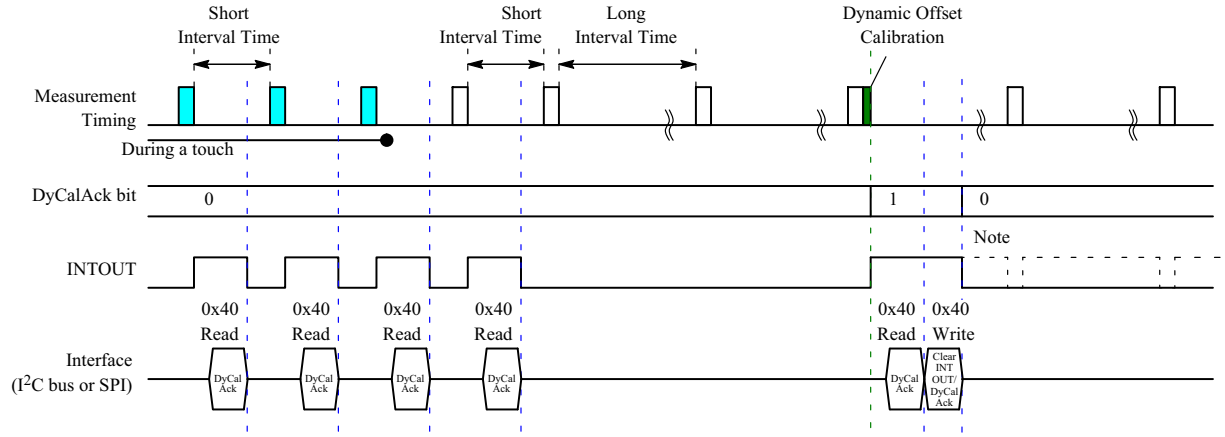


Figure 31. Timing of the Operation Flag of the Dynamic Offset Calibration (When INTMD1 = “0”, INTMD2 = “1”)



e.g., above situation is Debounce Count (ON→OFF) = 2 times, Long Interval Mode Start Count = 0 point.

NOTE: When the microcontroller does not clear DyCalAck bit and clears only IntOut bit, just after the end of the interval time or just after the end of the sleep, the LSI negates (“Low” level) INTOUT signal automatically. And when the LSI completed the measurement processing of the setting all channels , the LSI asserts (“High” level) of the INTOUT signal again.

Figure 32. Timing of the Operation Flag of the Dynamic Offset Calibration (When INTMD1 = “1”, INTMD2 = “1”)

OPERATION SEQUENCES

In this chapter, examples of operation sequence of the LC717A30 are described.

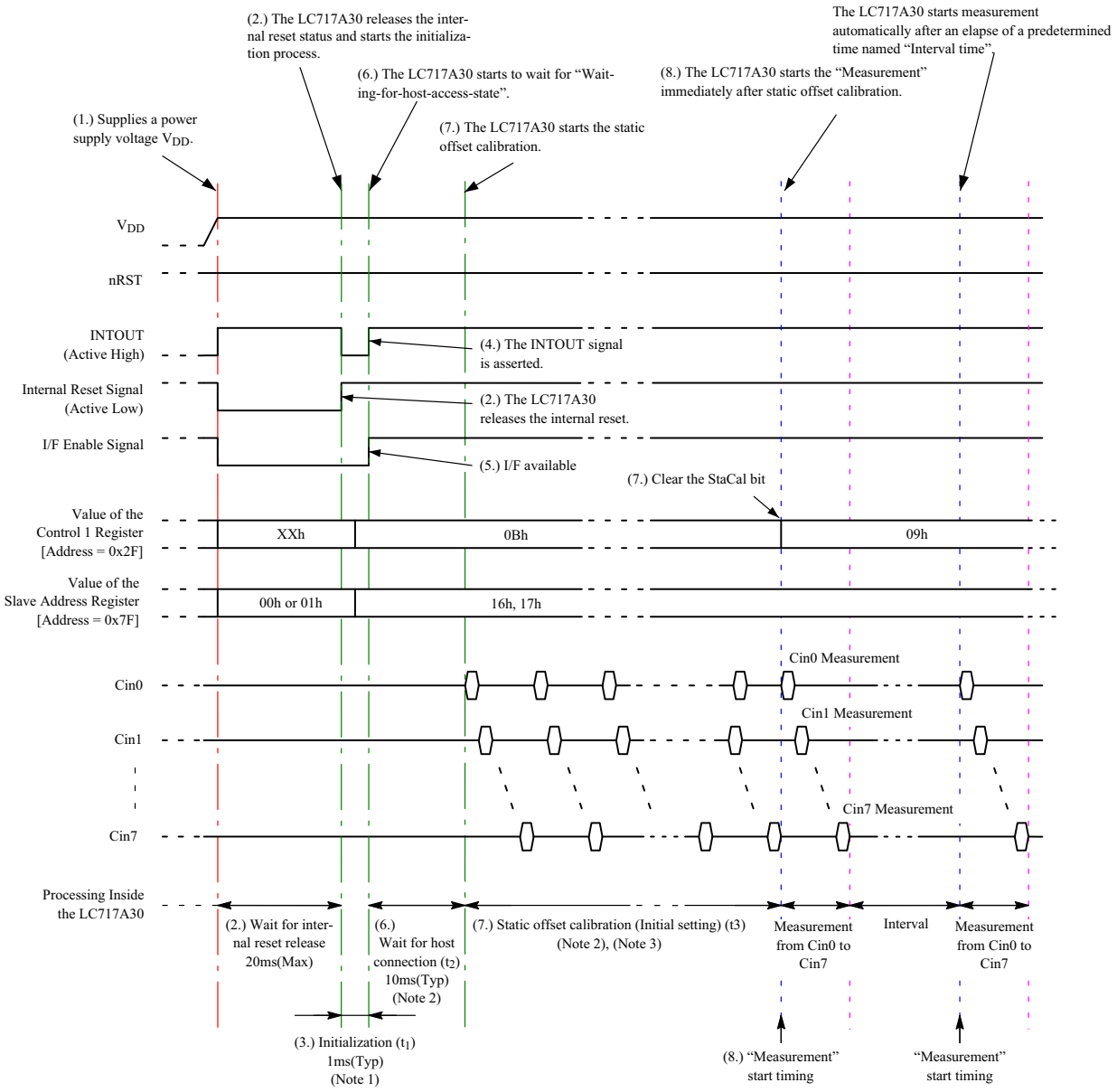
NOTE: In this chapter, the term “Measurement” means that the LC717A30 measures the amount of capacitance variation for each channel which is specified by the Use Channel Register [Address=0x00], and performs ON/OFF judgment for each channel, and reflects measurement results to registers such as the Result Data Register [Address=0x2A].

An Example of Operation Sequence After Reset

An Example of Operation Sequence Using the Power-ON Reset

The detailed explanation of the “Figure 33 – An example of Operation Sequence Using the Power-ON Reset” is following.

1. Supplies a power supply voltage V_{DD}. When the nRST pin isn’t used, please be connected to “High(V_{DD})”.
2. After reset processing time (Maximum 20 ms) of the LC717A30 was finished since the power supply voltage V_{DD} was supplied, the internal reset of the LC717A30 is released automatically. When the internal reset has been released, the LC717A30 negates (“Low” level) the INTOUT signal.
3. The LC717A30 performs initialization processing. In the initialization processing, the LC717A30 sets each register to predetermined default value.
   The initialization processing time is (t1)=2.0 ms (Max), (t1)=1.0 ms (Typ), (t1)=0.5 ms (Min).
4. After the initialization processing has completed, the LC717A30 asserts (“High” level) the INTOUT signal in order to notify the completion of internal initialization to the microcontroller.
5. After (4.), the I^2C bus or SPI interface of the LC717A30 becomes available. The microcontroller is able to read/write to the registers of the LC717A30.
6. The LC717A30 enters “Waiting-for-host-access-state” because the WriteReq bit in the Control 1 Register [Address=0x2F] is set to “0” as an initial value. (In other words, the LC717A30 starts waiting for the access from the host)
   If the application changes initial setting of the LC717A30 by the microcontroller, it promises the minimum time (t2) and completes it during a period of time (t2) awaiting host connection, and set the ParaCh bit in the Control 1 Register [Address=0x2F] to “1”. When register values written with the microcontroller at this time, reflected inside the LC717A30 by changing parameters, the following processing changes. Attention is necessary, because the LC717A30 may not be calibrated normally when application changes setting of it during static offset calibration. In addition, the timing to exit host connection wait state is when the data “1” was written into the WriteReq bit in the of Control 1 Register [Address=0x2F], or when the host connection waiting time (t2) passed after completing the initialization processing time (t1).
   The host connection waiting time is (t2)=14.3 ms (Max), (t2)=10.0 ms (Typ), (t2)=7.6 ms (Min).
7. The LC717A30 performs the static offset calibration because the StaCal bit in the Control 1 Register [Address=0x2F] is set to “1” as an initial value.
   When the static offset calibration has completed, the LC717A30 automatically sets the StaCal bit in the Control 1 Register [Address=0x2F] to “0”. In case that the LC717A30 has the first initial setting state, the static offset calibration time (t3) is as follows.
   <1> Time (t3) (Normal):
   (t3)=140.12 ms (Min), (t3)=182.16 ms (Typ), (t3)=260.23 ms (Max)
   <2> Time (t3) (That is, the time it takes for this LSI to perform the static offset calibration three times consecutively due to the error occurrence in the static offset calibration):
   (t3)=420.96 ms (Min), (t3)=547.08 ms (Typ), (t3)=781.29 ms (Max)
8. The LC717A30 repeats processing of the “Measurement” from Cin0 to Cin7 and processing of an interval. At that time, the LSI does the “Measurement” immediately without spacing of the interval time soon after the static offset calibration has completed.



Notes:

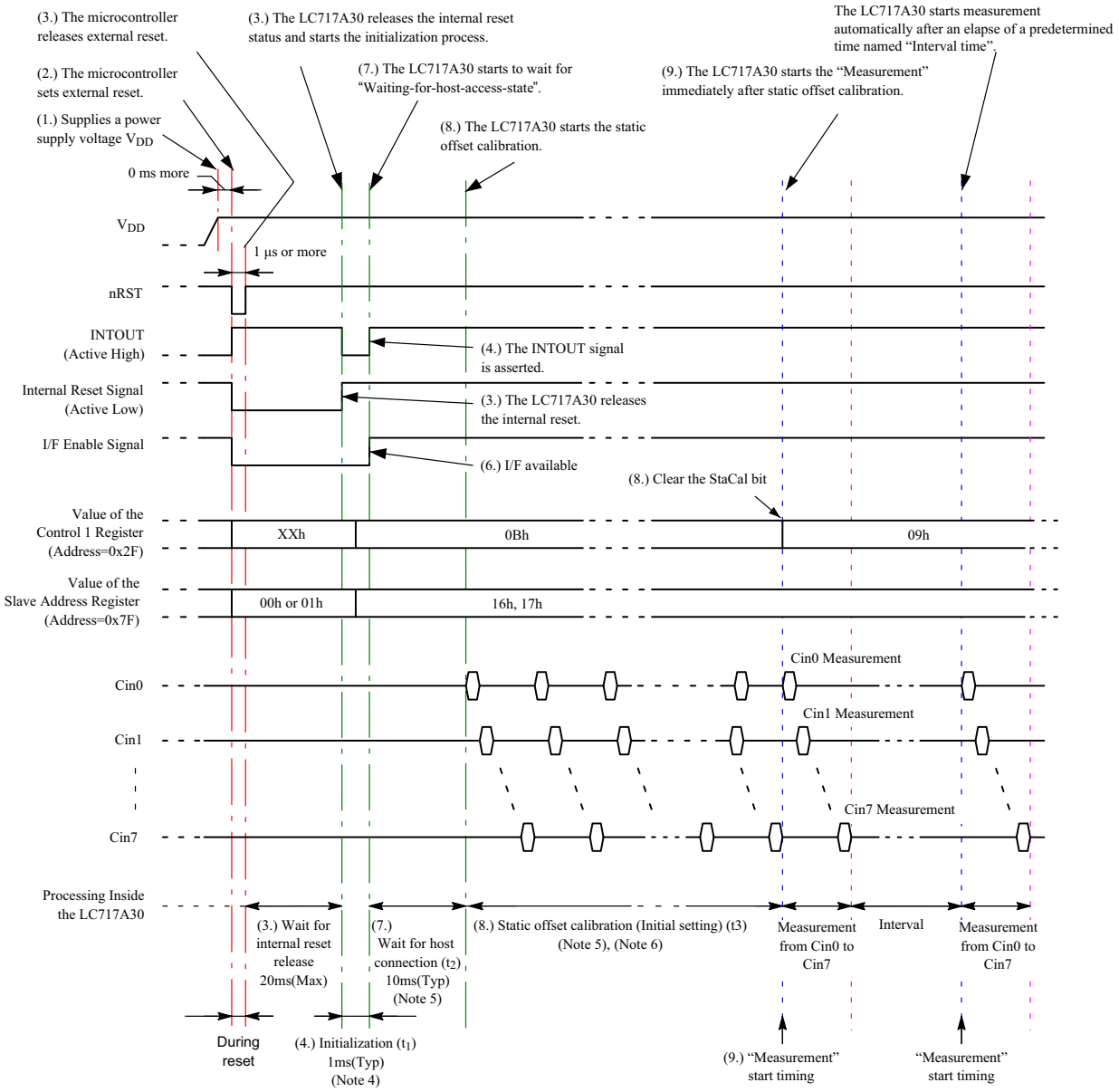
1. The initialization processing time is (t_1)=2.0 ms (Max), (t_1)=1.0 ms (Typ), (t_1)=0.5 ms (Min).
2. If the application changes initial setting of the LC717A30 by the microcontroller, it promises the minimum time (t2) and completes it during a period of time (t2) awaiting host connection, and set the ParaCh bit in the Control 1 Register [Address=0x2F] to "1". When register values written with the microcontroller at this time, reflected inside the LC717A30 by changing parameters, the following processing changes. Attention is necessary, because the LC717A30 may not be calibrated normally when application changes setting of it during static offset calibration. In addition, the timing to exit host connection wait state is when the data "1" was written into the WriteReq bit in the of Control 1 Register [Address=0x2F], or when the host connection waiting time (t2) passed after completing the initialization processing time (t1). The host connection waiting time is (t2)=14.3 ms (Max), (t2)=10.0 ms (Typ), (t2)=7.6 ms (Min).
3. In case that the LC717A30 has the first initial setting state, the static offset calibration time (t3) is as follows.
   <1> Time (t3) (Normal): (t3)=140.12 ms (Min), (t3)=182.16 ms (Typ), (t3)=260.23 ms (Max).
   <2> Time (t3) (That is, the time it takes for this LSI to perform the static offset calibration three times consecutively due to the error occurrence in the static offset calibration): (t3)=420.96 ms (Min), (t3)=547.08 ms (Typ), (t3)=781.29 ms (Max).

Figure 33. An Example of Operation Sequence Using the Power-ON Reset

An Example of Operation Sequence Using the External Reset Pin

The detailed explanation of the “Figure 34 – An example of Operation Sequence Using the External Reset Pin” is following.

1. Supplies a power supply voltage V_{DD}.
2. The microcontroller performs the external reset (nRST) of the LC717A30.
   The reset period: 1 μs or more.
3. After reset processing time (Maximum 20 ms) of the LC717A30 was finished since the external reset (nRST) has been released, the internal reset of the LC717A30 is released automatically. When the internal reset has been released, the LC717A30 negates (“Low” level) the INTOUT signal.
4. The LC717A30 performs initialization processing. In the initialization processing, the LC717A30 sets each register to predetermined default value.
   The initialization processing time is (t1)=2.0 ms (Max), (t1)=1.0 ms (Typ), (t1) = 0.5 ms (Min).
5. After the initialization processing has completed, the LC717A30 asserts (“High” level) the INTOUT signal in order to notify the completion of internal initialization to the microcontroller.
6. After (5.), the I^2C bus or SPI interface of the LC717A30 becomes available. The microcontroller is able to read/write to the registers of the LC717A30.
7. The LC717A30 enters “Waiting-for-host-access-state” because the WriteReq bit in the Control 1 Register [Address=0x2F] is set to “0” as an initial value. (In other words, the LC717A30 starts waiting for the access from the host)
   If the application changes initial setting of the LC717A30 by the microcontroller, it promises the minimum time (t2) and completes it during a period of time (t2) awaiting host connection, and set the ParaCh bit in the Control 1 Register [Address=0x2F] to “1”. When register values written with the microcontroller at this time, reflected inside the LC717A30 by changing parameters, the following processing changes. Attention is necessary, because the LC717A30 may not be calibrated normally when application changes setting of it during static offset calibration. In addition, the timing to exit host connection wait state is when the data “1” was written into the WriteReq bit in the of Control 1 Register [Address=0x2F], or when the host connection waiting time (t2) passed after completing the initialization processing time (t1).
   The host connection waiting time is (t2)=14.3 ms (Max), (t2)=10.0 ms (Typ), (t2)=7.6 ms (Min).
8. The LC717A30 performs the static offset calibration because the StaCal bit in the Control 1 Register [Address=0x2F] is set to “1” as an initial value.
   When the static offset calibration has completed, the LC717A30 automatically sets the StaCal bit in the Control 1 Register [Address=0x2F] to “0”. In case that the LC717A30 has the first initial setting state, the static offset calibration time (t3) is as follows.
   <1> Time (t3) (Normal):
   (t3)=140.12 ms (Min), (t3)=182.16 ms (Typ),
   (t3)=260.23 ms (Max)
   <2> Time (t3) (That is, the time it takes for this LSI to perform the static offset calibration three times consecutively due to the error occurrence in the static offset calibration):
   (t3)=420.96 ms(Min), (t3)=547.08 ms(Typ),
   (t3)=781.29 ms(Max)
9. The LC717A30 repeats processing of the “Measurement” from Cin0 to Cin7 and processing of an interval. At that time, the LSI does the “Measurement” immediately without spacing of the interval time soon after the static offset calibration has completed.



Notes:

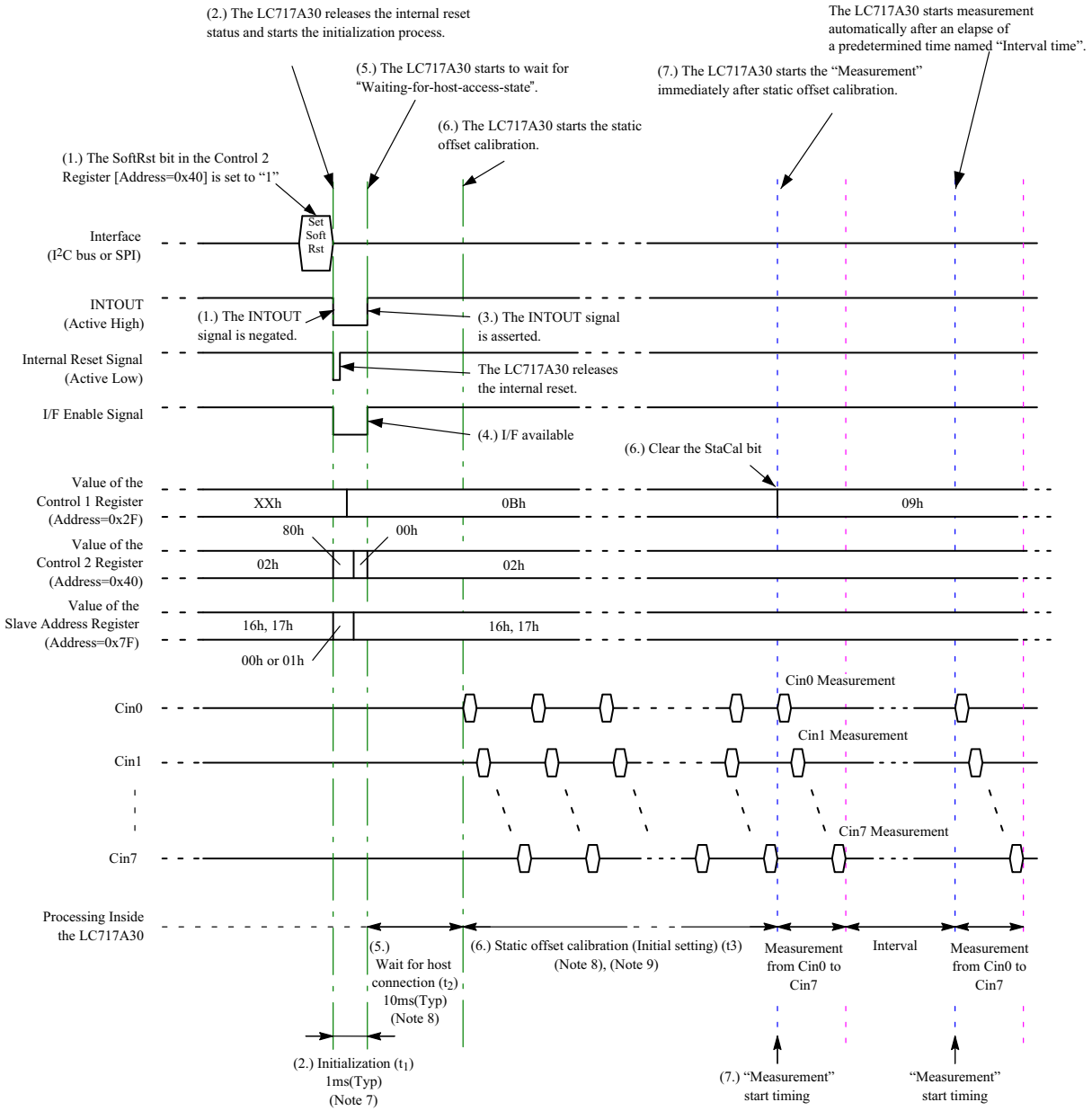
4. The initialization processing time is (t_1)=2.0 ms (Max), (t_1)=1.0 ms (Typ), (t_1)=0.5 ms (Min).
5. If the application changes initial setting of the LC717A30 by the microcontroller, it promises the minimum time (t2) and completes it during a period of time (t2) awaiting host connection, and set the ParaCh bit in the Control 1 Register [Address=0x2F] to “1”. When register values written with the microcontroller at this time, reflected inside the LC717A30 by changing parameters, the following processing changes. Attention is necessary, because the LC717A30 may not be calibrated normally when application changes setting of it during static offset calibration. In addition, the timing to exit host connection wait state is when the data “1” was written into the WriteReq bit in the of Control 1 Register [Address=0x2F], or when the host connection waiting time (t2) passed after completing the initialization processing time (t1). The host connection waiting time is (t2)=14.3 ms (Max), (t2)=10.0 ms (Typ), (t2)=7.6 ms (Min).
6. In case that the LC717A30 has the first initial setting state, the static offset calibration time (t3) is as follows.
   <1> Time (t3) (Normal): (t3)=140.12 ms (Min), (t3)=182.16 ms (Typ), (t3)=260.23 ms (Max).
   <2> Time (t3) (That is, the time it takes for this LSI to perform the static offset calibration three times consecutively due to the error occurrence in the static offset calibration): (t3)=420.96 ms (Min), (t3)=547.08 ms (Typ), (t3)=781.29 ms (Max).

Figure 34. An Example of Operation Sequence Using the External Reset Pin

An Example of Operation Sequence Using the Software Reset

The detailed explanation of the “Figure 35 – An example of Operation Sequence Using the Software Reset” is following.

1. When the SoftRst bit in the Control 2 Register [Address=0x40] is set to “1”, the LC717A30 performs initialization processing. When software reset processing is started, the LC717A30 negates (“Low” level) the INTOUT signal.
2. The LC717A30 performs initialization processing. In the initialization processing, the LC717A30 sets each register to predetermined default value.
   The initialization processing time is (t1)=2.0 ms (Max), (t1)=1.0 ms (Typ), (t1)=0.5 ms (Min).
   When software reset is completed, the SoftRst bit in the Control 2 Register [Address=0x40] is set to “0” automatically.
3. After the initialization processing has completed, the LC717A30 asserts (“High” level) the INTOUT signal in order to notify the completion of internal initialization to the microcontroller.
4. After (3.), the I^2C bus or SPI interface of the LC717A30 becomes available. The microcontroller is able to read/write to the registers of the LC717A30.
5. The LC717A30 enters “Waiting-for-host-access-state” because the WriteReq bit in the Control 1 Register [Address=0x2F] is set to “0” as an initial value. (In other words, the LC717A30 starts waiting for the access from the host)
   If the application changes initial setting of the LC717A30 by the microcontroller, it promises the minimum time (t2) and completes it during a period of time (t2) awaiting host connection, and set the ParaCh bit in the Control 1 Register [Address=0x2F] to “1”. When register values written with the microcontroller at this time, reflected inside the LC717A30 by changing parameters, the following processing changes. Attention is necessary, because the LC717A30 may not be calibrated normally when application changes setting of it during static offset calibration. In addition, the timing to exit host connection wait state is when the data “1” was written into the WriteReq bit in the of Control 1 Register [Address=0x2F], or when the host connection waiting time (t2) passed after completing the initialization processing time (t1).
   The host connection waiting time is (t2)=14.3 ms (Max), (t2)=10.0 ms (Typ), (t2)=7.6 ms (Min).
6. The LC717A30 performs the static offset calibration because the StaCal bit in the Control 1 Register [Address=0x2F] is set to “1” as an initial value.
   When the static offset calibration has completed, the LC717A30 automatically sets the StaCal bit in the Control 1 Register [Address=0x2F] to “0”. In case that the LC717A30 has the first initial setting state, the static offset calibration time (t3) is as follows.
   <1> Time (t3) (Normal):
   (t3)=140.12 ms (Min), (t3)=182.16 ms (Typ), (t3)=260.23 ms (Max)
   <2> Time (t3) (That is, the time it takes for this LSI to perform the static offset calibration three times consecutively due to the error occurrence in the static offset calibration):
   (t3)=420.96 ms (Min), (t3)=547.08 ms (Typ), (t3)=781.29 ms (Max)
7. The LC717A30 repeats processing of the “Measurement” from Cin0 to Cin7 and processing of an interval. At that time, the LSI does the “Measurement” immediately without spacing of the interval time soon after the static offset calibration has completed.



Notes:

7. The initialization processing time is (t_1)=2.0 ms (Max), (t_1)=1.0 ms (Typ), (t_1)=0.5 ms (Min).
8. If the application changes initial setting of the LC717A30 by the microcontroller, it promises the minimum time (t2) and completes it during a period of time (t2) awaiting host connection, and set the ParaCh bit in the Control 1 Register [Address=0x2F] to "1". When register values written with the microcontroller at this time, reflected inside the LC717A30 by changing parameters, the following processing changes. Attention is necessary, because the LC717A30 may not be calibrated normally when application changes setting of it during static offset calibration. In addition, the timing to exit host connection wait state is when the data "1" was written into the WriteReq bit in the of Control 1 Register [Address=0x2F], or when the host connection waiting time (t2) passed after completing the initialization processing time (t1). The host connection waiting time is (t2)=14.3 ms (Max), (t2)=10.0 ms (Typ), (t2)=7.6 ms (Min).
9. In case that the LC717A30 has the first initial setting state, the static offset calibration time (t3) is as follows.
<1> Time (t3) (Normal): (t3)=140.12 ms (Min), (t3)=182.16 ms (Typ), (t3)=260.23 ms (Max).
<2> Time (t3) (That is, the time it takes for this LSI to perform the static offset calibration three times consecutively due to the error occurrence in the static offset calibration): (t3)=420.96 ms (Min), (t3)=547.08 ms (Typ), (t3)=781.29 ms (Max).

Figure 35. An Example of Operation Sequence Using the Software Reset

An Example of Operation Sequence When the Interval Mode Operation

Generally, it is recommended for the LC717A30 to operate in the “Interval Mode” rather than in the “Sleep mode”.

An example of operation sequence in the case of eight channels are used and always set to the “Interval Mode” is shown in Figure 36 and Figure 37. In this example, both the INTMD1 bit and the INTMD2 bit in the Measurement 1 Register [Address=0x3A] are always set to “0”, so the LC717A30 always asserts (“High” level) the INTOUT immediately after the measurement has completed, and it doesn’t negate (“Low” level) the INTOUT signal automatically.

The summary of the description of the operation sequence in Figure 36 and Figure 37 are as follows:

- Assume that the LC717A30 operates in the “Interval Mode” with all eight channels enabled.
  (In concrete terms, assume that the LC717A30 repeats “Measurement” in the “Interval Mode”, and the microcontroller reads measurement results over the I^2C bus or SPI)
- After writing new settings into LC717A30’s registers, the microcontroller issues a request to the LC717A30 for reflecting new settings to the operation and performing the static offset calibration.
- After both the reflection of the new settings and the static offset calibration have completed, the microcontroller reads measurement results from the LC717A30.

The details about Figure 36 and Figure 37 are described below.

1. Assume that the LC717A30 operates in the “Interval Mode” with all eight channels enabled.
   (In concrete terms, the LC717A30 repeats measurement, and the microcontroller negates (“Low” level) the INTOUT signal and reads measurement results over the I^2C bus or SPI every time it detects the assertion (“High” level) of the INTOUT signal)
2. In order to change the settings of the LC717A30, the microcontroller writes an appropriate parameter value to each register of the LC717A30, the address range of which are 0x00 to 0x19, 0x22 to 0x29, 0x2B or 0x30 to 0x3D, over the I^2C bus or SPI. (Note: At this time, the LC717A30 doesn’t still operate according to the new settings)
3. The microcontroller writes 8Fh in the Control 1 Register [Address=0x2F]. Herewith, the microcontroller reflects new setting for LC717A30 and demands that it performs the static offset calibration based on new setting.
4. This demand for the LC717A30 is pending until the end of the interval time.
5. As soon as the period of the interval time ends, the LC717A30 accepts the request described in the above (3.). As a result, the WriteReq bit in the Control 1 Register [Address=0x2F] changes from “1” to “0”. Subsequently, the new settings are reflected to the LC717A30’s operation. (That is to say, the LC717A30 operates according to the new settings)
6. After (5.), the LC717A30 performs the static offset calibration based on the new settings.
7. The LC717A30 starts the “Measurement”. When the “Measurement” of all the enabled channels has completed, the LC717A30 asserts (“High” level) the INTOUT signal every time.
8. Every time the microcontroller detects the assertion (“High” level) of the INTOUT signal, the microcontroller negates (“Low” level) the INTOUT signal and reads measurement results over the I^2C bus or SPI.

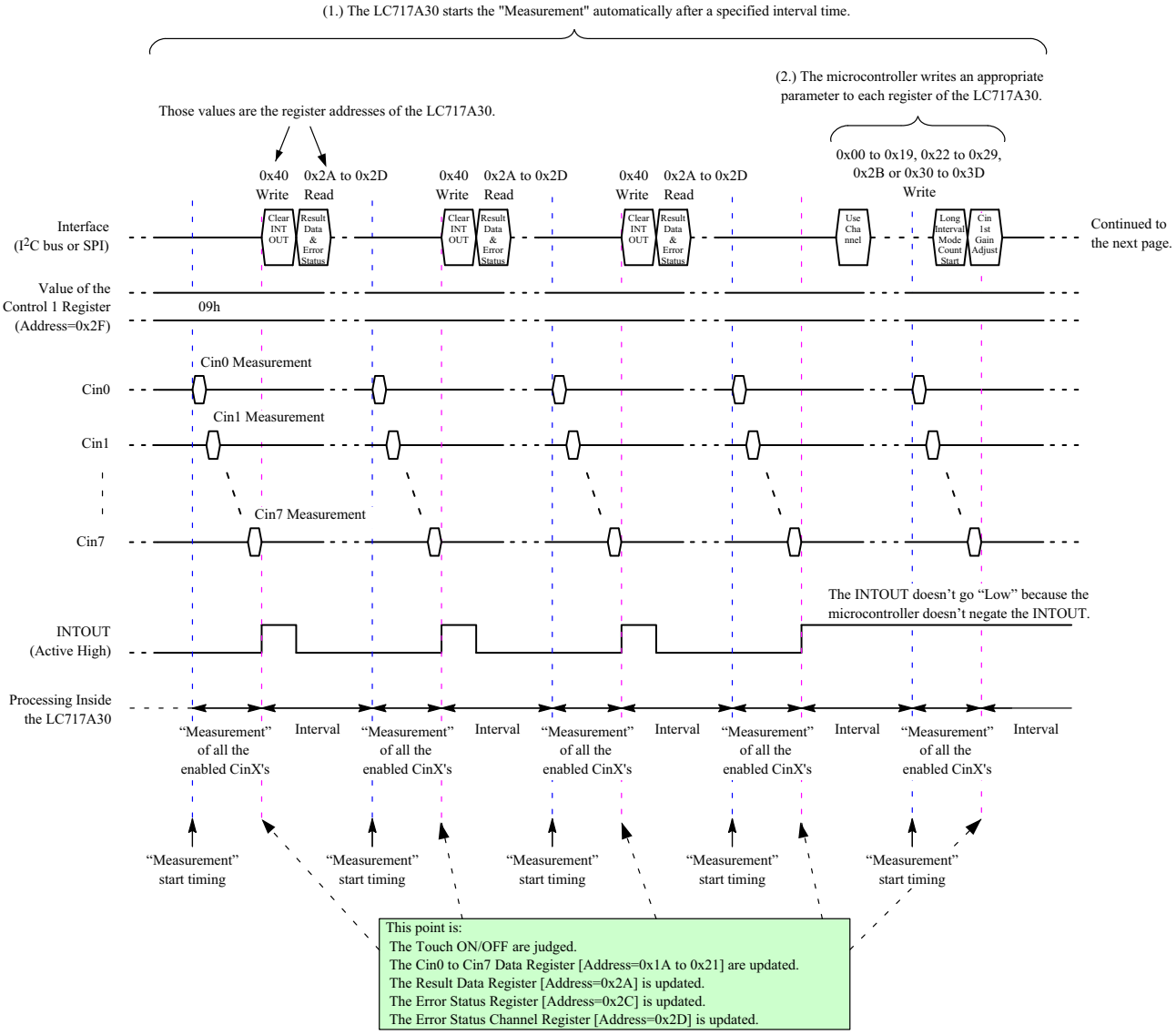


Figure 36. An Example of Operation Sequence When the Interval Mode Operation (1/2)

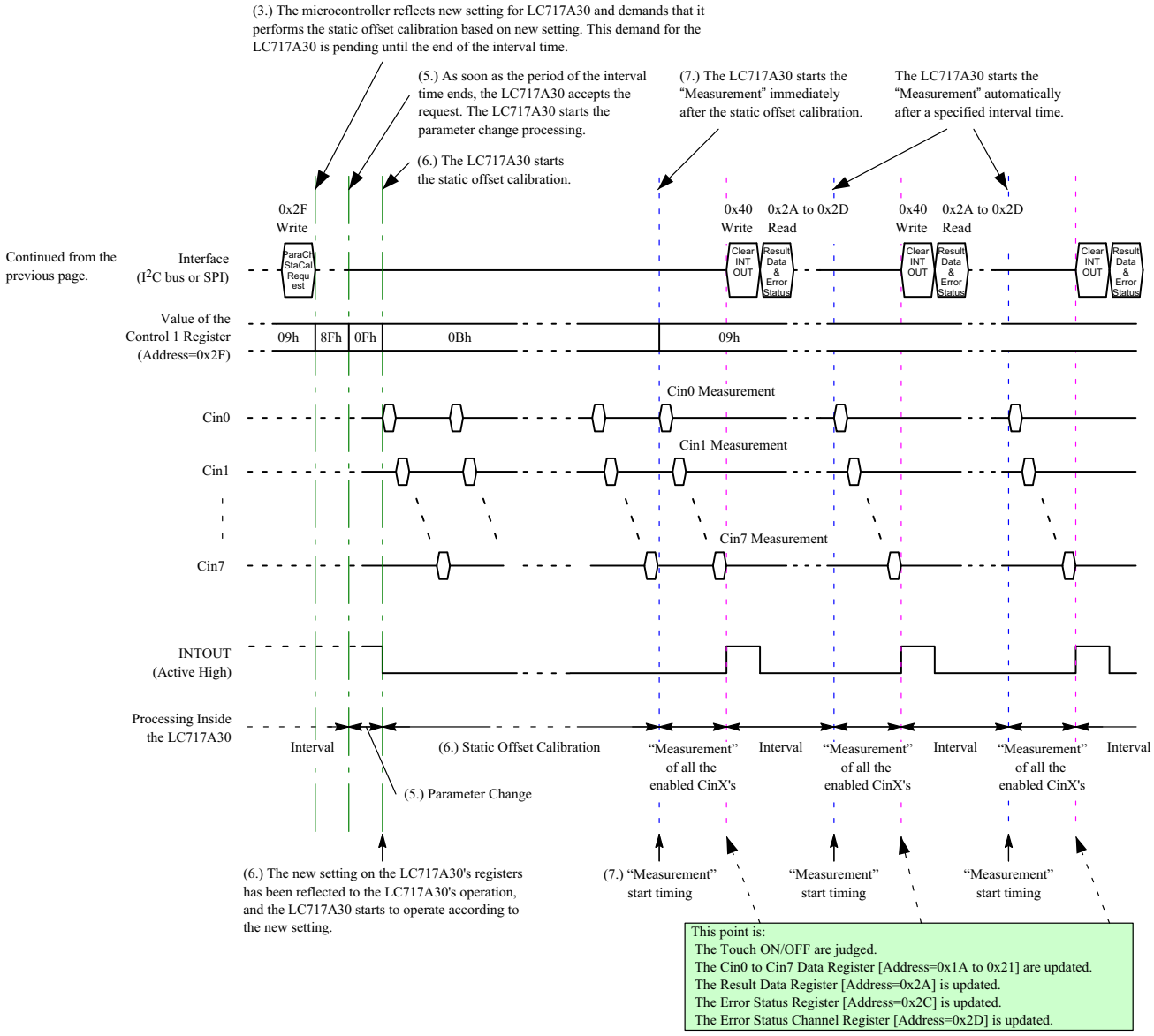


Figure 37. An Example of Operation Sequence When the Interval Mode Operation (2/2)

An Example of Operation Sequence When the Sleep Mode Operation

An example of operation sequence in the case of eight channels are used and always set to the “Sleep Mode” is shown in Figure 38 and Figure 39. In this example, both the INTMD1 bit and the INTMD2 bit in the Measurement 1 Register [Address=0x3A] are always set to “0”, so the LC717A30 always asserts (“High” level) the INTOUT immediately after the measurement has completed.

In the case of a sleep mode, when the microcontroller wakes up the LC717A30 of the sleep state, the LC717A30 does sleep after having enforced the “Measurement” of all the enabled channels only once. In addition, when the LC717A30 becomes the sleep, the INTOUT signal is asserted (“High” level).

The summary of the description of the operation sequence in Figure 38 and Figure 39 are as follows:

- Assume that the LC717A30 operates in the “Sleep Mode” with all eight channels enabled.
  (In concrete terms, assume that the LC717A30 and the microcontroller operate as follows: Every time the microcontroller detects the assertion (“High” level) of the INTOUT signal, the microcontroller reads measurement results over the I^2C bus or SPI and it wakes up the LC717A30 at a predetermined time)
- After writing new settings into the LC717A30’s registers, the microcontroller issues a request to the LC717A30 only once for reflecting new settings to the operation and performing static offset calibration, and it wakes up the LC717A30.
- After that, the LC717A30 starts to perform the “Measurement”. After the “Measurement”, the LC717A30 goes to sleep. Every time the microcontroller detects the assertion (“High” level) of the INTOUT signal, the microcontroller reads measurement results and it wakes up the LC717A30 at a predetermined time.
- Every time the microcontroller detects the LC717A30 of the sleep state, the microcontroller negates (“Low” level) the INTOUT signal and reads measurement results over the I^2C bus or SPI and it wakes up the LC717A30 at a predetermined time.

The details about Figure 38 and Figure 39 are described below.

1. Assume that the LC717A30 operates in the “Sleep Mode” with all eight channels enabled.
   (In concrete terms, the LC717A30 and the microcontroller operate as follows: Every time the microcontroller detects the assertion (“High” level) of the INTOUT signal, the microcontroller reads measurement results over the I^2C bus or SPI and it wakes up the LC717A30 at a predetermined time)
2. In order to change the settings of the LC717A30, the microcontroller writes an appropriate parameter value to each register of the LC717A30, the address range of which are 0x00 to 0x19, 0x22 to 0x29, 0x2B or 0x30 to 0x3D, over the I^2C bus or SPI. (Note: At this time, the LC717A30 doesn’t still operate according to the new settings)
3. The microcontroller writes 87h in the Control 1 Register [Address= 0x2F]. Herewith, the microcontroller reflects new setting for LC717A30 and demands that it performs the static offset calibration based on new setting.
4. The microcontroller wakes up the LC717A30 of the sleep state.
5. After the LC717A30 has been woken up, the LC717A30 accepts the request described in the above (3.). As a result, the WriteReq bit in the Control 1 Register [Address=0x2F] changes from “1” to “0”. Subsequently, the new settings are reflected to the LC717A30’s operation. (That is to say, the LC717A30 operates according to the new settings)
6. After the reflection of the new settings, the LC717A30 performs the static offset calibration based on the new settings.
7. The LC717A30 starts the “Measurement”. Every time the “Measurement” of all the enabled channels has completed, the LC717A30 asserts (“High” level) the INTOUT signal and goes to sleep.
8. Every time the microcontroller detects the assertion (“High” level) of the INTOUT signal (that is, the LC717A30 has gone to sleep), the microcontroller reads measurement results over the I^2C bus or SPI and it wakes up the LC717A30 at a predetermined time.
9. The microcontroller repeats the above (7.) to (8.).

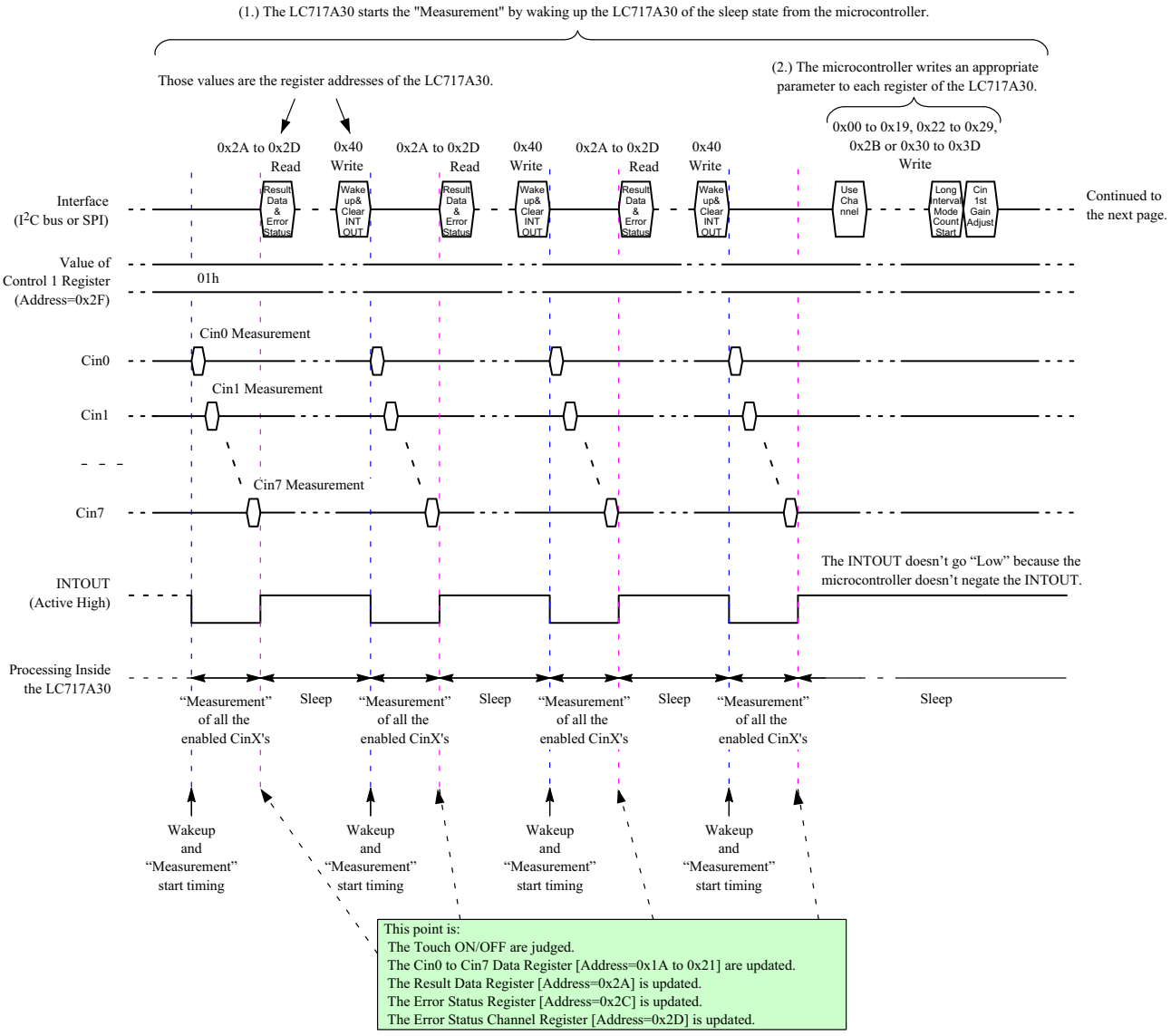


Figure 38. An Example of Operation Sequence When the Sleep Mode Operation (1/2)

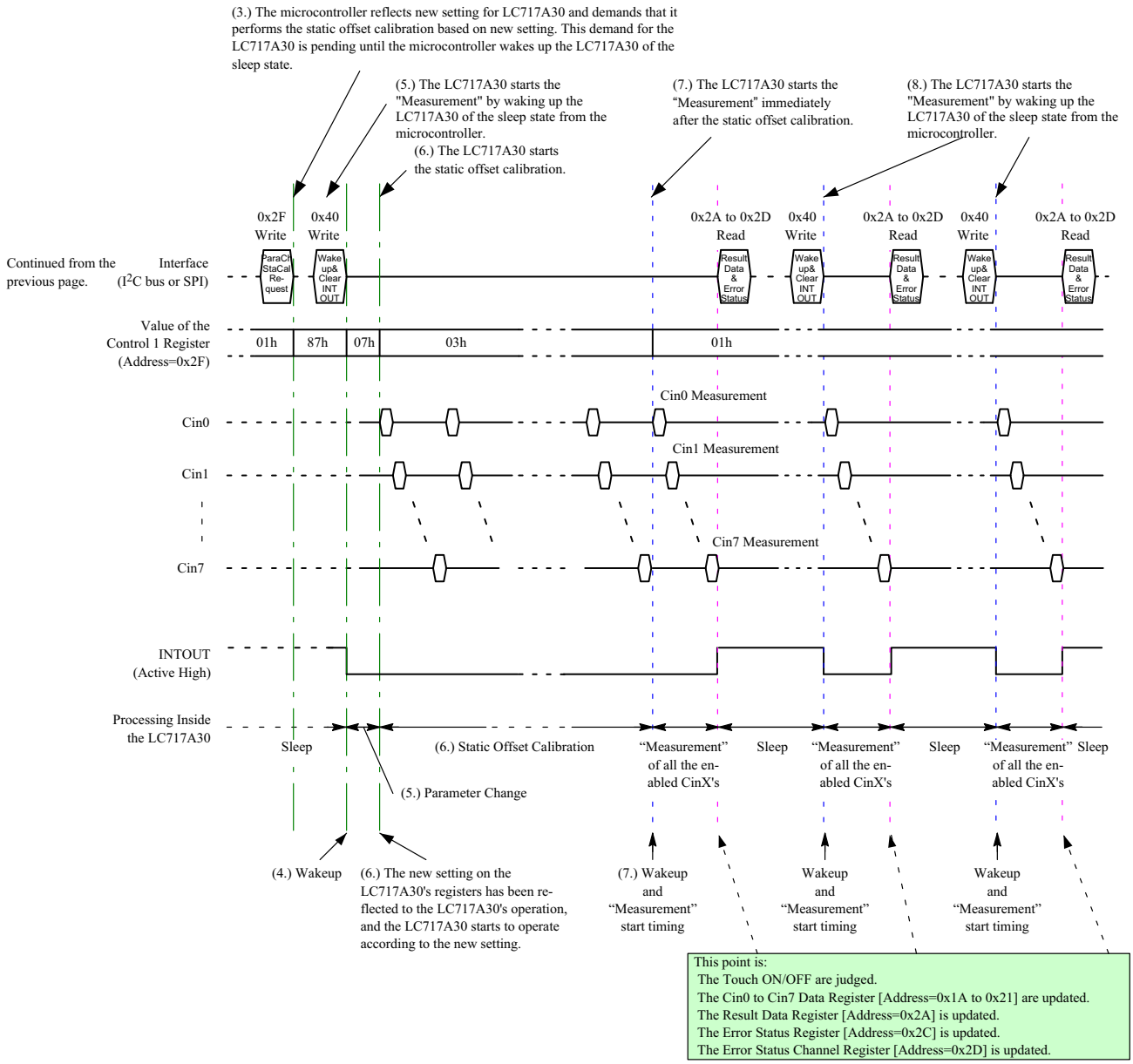


Figure 39. An Example of Operation Sequence When the Sleep Mode Operation (2/2)

CONTROL EXAMPLES FOR THE MICROCONTROLLER TO CONTROL THE LC717A30

In this chapter, six control flow examples for a microcontroller to control the LC717A30 are shown and described.

- The microcontroller reads the measurement result with the INTOUT signal at the time of the “Interval Mode”.
- The microcontroller reads the measurement result without the INTOUT signal at the time of the “Interval Mode”.
- The microcontroller reads the measurement result with the INTOUT signal at the time of the “Sleep Mode”.
- The microcontroller reads and writes the registers of the CdacP/CdacM/DigitalOffset.
- The microcontroller reads the measurement result using two LC717A30.
- The sensitivity adjustment.

NOTE: In this chapter, the term “Measurement” means that the LC717A30 measures the amount of capacitance variation for each channel which is specified by the Use Channel Register [Address=0x00], and performs ON/OFF judgment for each channel, and reflects measurement results to registers such as the Result Data Register [Address=0x2A].

NOTE: When at least one bit of the WriteReq bit, the ParaCh bit and the StaCal bit is not “0”, the microcontroller must not write to the Control 1 Register [Address=0x2F]. (In other word, only when all of the WriteReq bit, the ParaCh bit and the StaCal bit are “0”, the microcontroller is able to write to the Control 1 Register [Address=0x2F])
As an exception, between the time when the LSI asserts the INTOUT to notify of completing the LSI internal initialization after the release of reset and the time when static offset calibration which is automatically performed based on default parameters is completed, the microcontroller might write 80h or 88h to the Control 1 Register even if the read value of the StaCal bit is “1”. By doing this, the execution of the static offset calibration and/or measurement based on LSI’s default parameters can be cancelled.

NOTE: When writing a value in the Control 2 Register [Address=0x40] either to clear INTOUT output or to wake up this LSI that is sleeping, do it during interval processing (In the case of interval mode) or during sleep period (In the case of sleep mode). If it can’t be guaranteed that the microcontroller writes during interval processing, select the Interval Mode and select the mode that INTOUT is negated automatically (In other words, set the IntMode bit in Control 1 Register [Address=0x2F] to “1”, and set the INTMD2 bit in Measurement Mode 1 Register [Address=0x3A] to “1”).

Control Flow Examples

In the Case of Reading the Measurement Result with the INTOUT Signal at the "Interval Mode"

The microcontroller is connected to the LC717A30 over I^2C bus or SPI, and a GPIO port of the microcontroller is connected to the INTOUT pin of the LC717A30, and another GPIO port is connected to the nRST pin.

In such case, explains the control example when the microcontroller detects the assertion ("High" level) of the INTOUT signal and reads measurement results over the I^2C bus or SPI every time.

In this control example, the microcontroller always sets the LC717A30's operation mode to the "Interval Mode". (In concrete terms, the microcontroller always writes "1" to the IntMode bit in the Control 1 Register [Address=0x2F]) In addition, both the INTMD1 bit and the INTMD2 bit in the Measurement 1 Register [Address=0x3A] are always set to "0", so the LC717A30 always asserts ("High" level) the INTOUT immediately after the "Measurement" has completed and it doesn't negate ("Low" level) the INTOUT signal automatically.

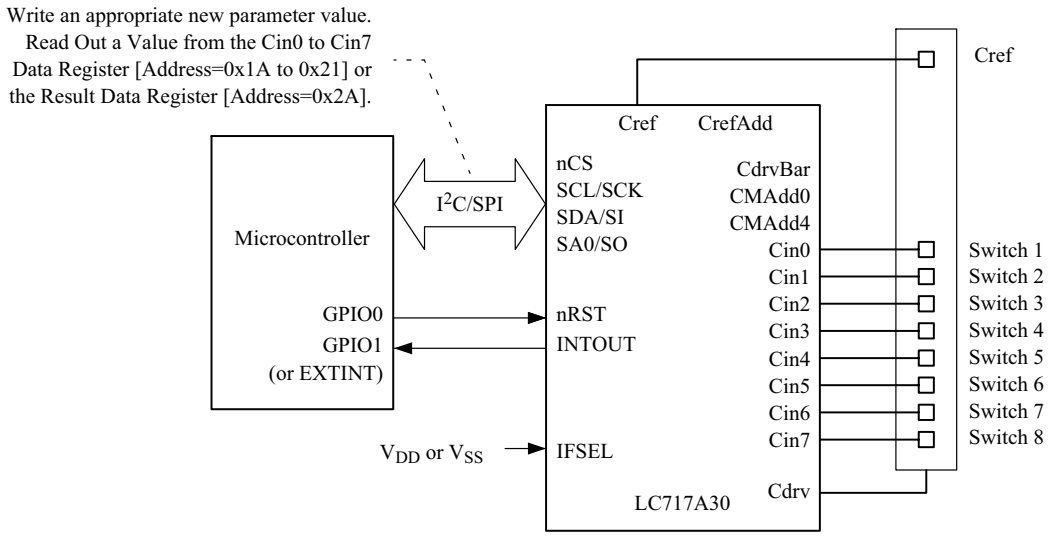


Figure 40. Connection (1) Between the Microcontroller and the LC717A30

1. The microcontroller resets the LC717A30 by controlling the nRST signal line via a GPIO port. (In concrete terms, the microcontroller outputs "Low" to nRST signal line, and then it outputs "High" to nRST signal line. The output from the GPIO port of the microcontroller, which is connected to the nRST pin, has to be kept "Low" for at least 1 microsecond)
2. After controlling the nRST signal line, the microcontroller checks the status of the INTOUT signal via another GPIO port. As soon as the microcontroller detects the rising edge of the INTOUT signal, it sets 88h to the Control 1 Register [Address=0x2F] over the I^2C bus or SPI. (To put it concretely, the microcontroller writes 88h to the Control 1 Register [Address=0x2F] within 5 milliseconds after the INTOUT signal goes "High" level)

   NOTE: By doing (2.), the execution of the static offset calibration and "Measurement", which is performed automatically after initialization in the LC717A30, can be cancelled. (Conversely, if you allow the microcontroller to perform the static offset calibration and the subsequent measurement which are performed automatically by the LC717A30 according to the default setting of the LC717A30, the microcontroller need not do the processing described above, but the microcontroller usually has to wait at least until the static offset calibration has completed)
3. The microcontroller writes an appropriate parameter value to each register of the LC717A30 over the I^2C bus or SPI. (For more information about registers the microcontroller may write a parameter to, refer to the inside of the blue dashed line box(a) on the control flow figure shown in Figure 41)

   Especially, in this example, the microcontroller writes "0" to both the INTMD1 bit and the INTMD2 bit in the Measurement 1 Register [Address=0x3A] so that the LC717A30 may not negate ("Low" level) the INTOUT signal automatically.

   NOTE: At this time, new settings on all the registers are not still reflected to the LC717A30's operation. (In other words,

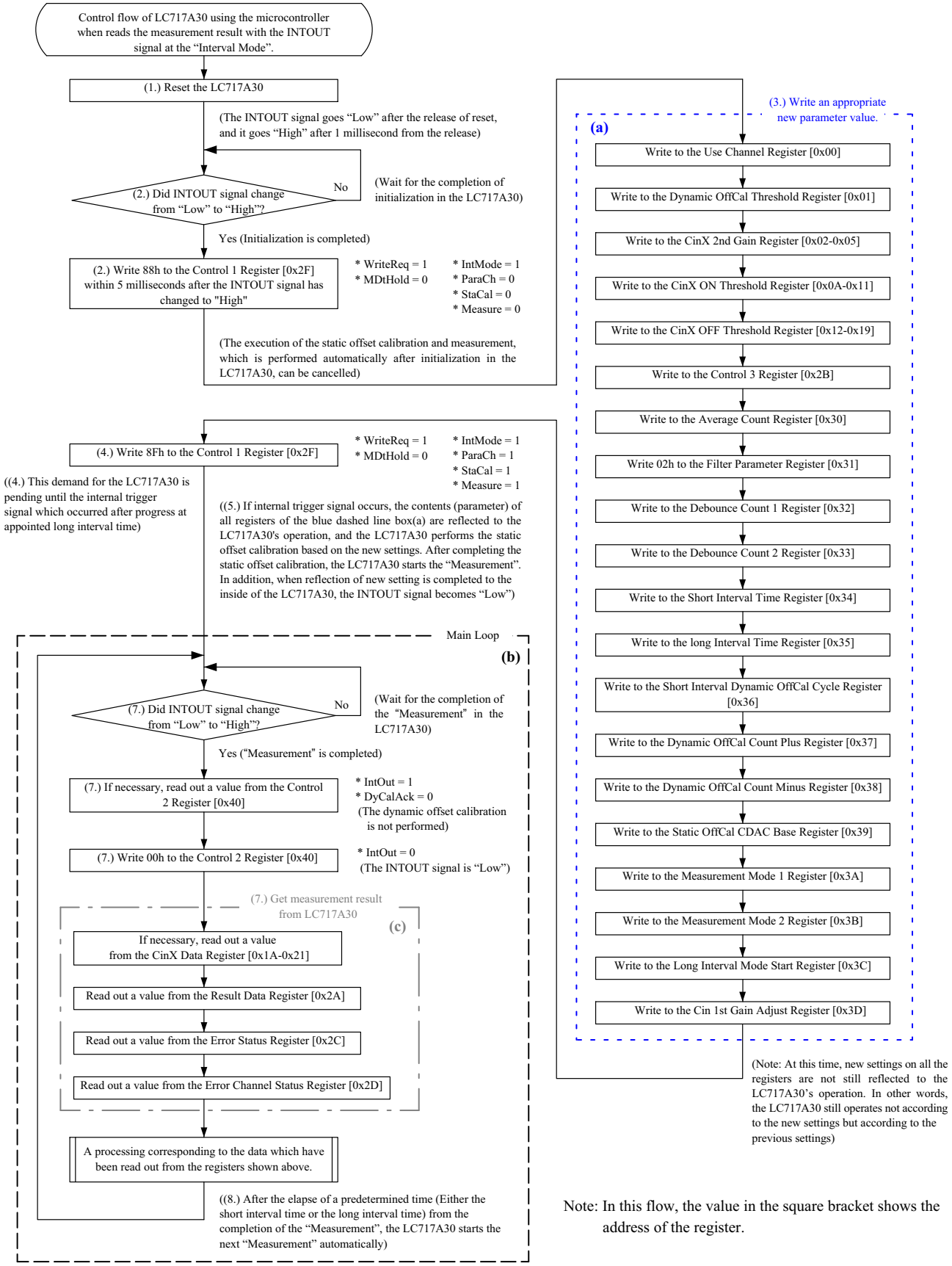
the LC717A30 still operates not according to the new settings but according to the previous settings)

4. To reflect the new settings to the LC717A30's operation and to make the LC717A30 perform the static offset calibration and the "Measurement", the microcontroller writes 8Fh to the Control 1 Register [Address=0x2F] over the I^2C bus or SPI. This demand for the LC717A30 is pending until the internal trigger signal which occurred after progress at appointed long interval time.
5. If internal trigger signal occurs, the new settings on all the registers are reflected to the LC717A30's operation. (That is to say, the LC717A30 waits for a processing start until the maximum time of appointed long interval time. And the LC717A30 operates according to the new settings)

   NOTE: In addition, when reflection of new setting is completed to the inside of the LC717A30, the INTOUT signal of the LC717A30 does negation ("Low" level) automatically. Furthermore, the Cin0 to Cin7 Data Register [Address=0x1A to 0x21], the Result Data Register [Address=0x2A], the Error Status Register [Address=0x2C] and the Error Channel Status Register [Address=0x2D] are all initialized into 00h. Particularly, please be careful about initializing the touch ON/OFF judgement result of all channels to OFF. And counters inside this LSI which are used for the processing of the dynamic offset calibration and the processing of debounce are all cleared.
6. The LC717A30 performs the static offset calibration based on the new settings. After completing the static offset calibration, the LC717A30 starts the "Measurement".
7. In order to check the completion of the measurement in the LC717A30, the microcontroller checks the assertion ("High" level) of the INTOUT signal. After detecting the assertion ("High" level) of the INTOUT signal, the microcontroller writes 00h to the Control 2 Register [Address=0x40] to negate ("Low" level) the INTOUT signal, and it reads measurement results from the Result Data Register [Address=0x2A] and so on.

   NOTE: At the time of the completion of the "Measurement", the LC717A30 outputs "High" to the INTOUT signal line. When the dynamic offset calibration is enforced, the DyCalAck bit in the Control 2 Register [Address=0x40] is set to "1" at the same time IntOut bit is set to "1", and the LC717A30 asserts ("High" level) the INTOUT signal. Therefore, the microcontroller can confirm that the dynamic offset calibration was enforced by reading the Control 2 Register [Address=0x40] after having confirmed assertion ("High" level) of the INTOUT signal.
8. After the elapse of a predetermined time (Either the short interval time or the long interval time) from the completion of the "Measurement", the LC717A30 starts the next "Measurement" automatically.
9. The microcontroller repeats the above (7.) through (8.).

The control flow figure corresponding to the control sequence described above is shown on the next page.



Note: In this flow, the value in the square bracket shows the address of the register.

Figure 41. Control Flow Example When the Microcontroller Reads the Measurement Result with the INTOUT Signal at the “Interval Mode”

In the Case of Reading the Measurement Result without the INTOUT Signal at the "Interval Mode"

The microcontroller is connected to the LC717A30 over I^2C bus or SPI, and a GPIO port of the microcontroller is connected to the nRST pin of the LC717A30. The microcontroller doesn't check the INTOUT signal of the LC717A30. Without detecting the assertion of the INTOUT signal, the microcontroller reads measurement results periodically (at 50-millisecond intervals) from the Result Data Register [Address=0x2A] and so on.

However, when a microcontroller reads and writes from serial interface (I^2C bus or SPI) during execution of the offset calibration or the "Measurement", we do not recommend the application to read the measurement result without using INTOUT, because to have possibilities to affect the measurement result by a switching noise of interface signals (nCS, SCL/SCK, SDA/SI, SA0/SO).

In this control example, the microcontroller always sets the LC717A30's operation mode to "Interval Mode". (In concrete terms, the microcontroller always writes "1" to the IntMode bit in the Control 1 Register [Address=0x2F])

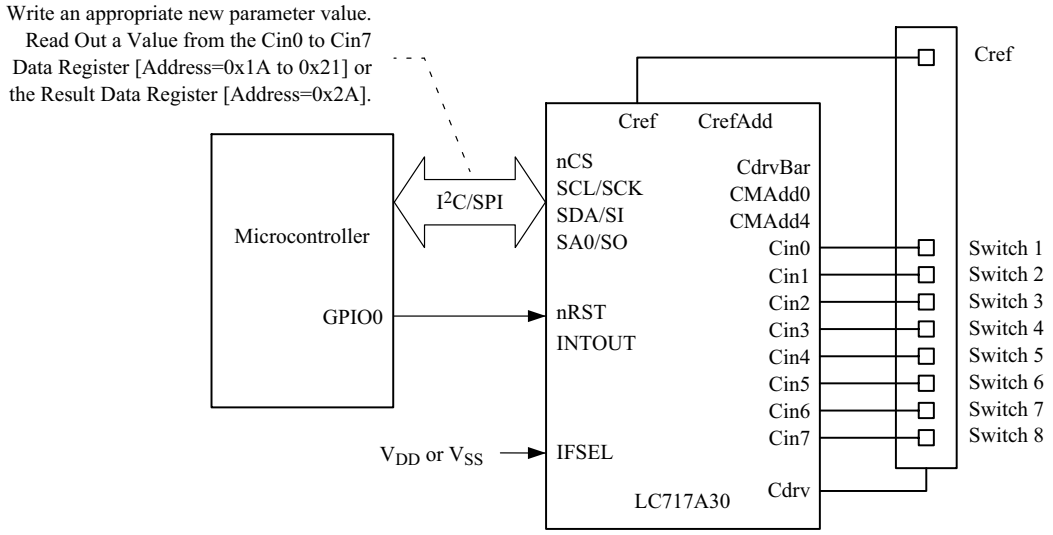


Figure 42. Connection (2) Between the Microcontroller and the LC717A30

1. The microcontroller resets the LC717A30 by controlling the nRST signal line via a GPIO port.
   (In concrete terms, the microcontroller outputs "Low" to nRST signal line, and then it outputs "High" to nRST signal line. The output from the GPIO port of the microcontroller, which is connected to the nRST pin, has to be kept "Low" for at least 1 microsecond)
2. After controlling the nRST signal line, the microcontroller waits until a reasonable amount of time passes since the LC717A30 has gone into the static offset calibration. For example, the microcontroller waits for 100 milliseconds from the release of reset. Afterwards, the microcontroller reads the Control 1 Register [Address=0x2F] and waits until the StaCal bit becomes "0".
3. The microcontroller writes an appropriate parameter value to each register of the LC717A30 over the I^2C bus or SPI. (For more information about registers the microcontroller may write a parameter to, refer to the inside of the blue dashed line box(a) on the control flow figure shown in Figure 43)
   Especially, in this example, the microcontroller writes "0" to both the INTMD1 bit and the INTMD2 bit in the Measurement 1 Register [Address=0x3A] so that the LC717A30 may not negate ("Low" level) the INTOUT signal automatically.

   NOTE: At this time, new settings on all the registers are not still reflected to the LC717A30's operation. (In other words, the LC717A30 still operates not according to the new settings but according to the previous settings)
4. To reflect the new settings to the LC717A30's operation and to make the LC717A30 perform the static offset calibration and the "Measurement", the microcontroller writes 8Fh to the Control 1 Register [Address=0x2F] over the I^2C bus or SPI. This demand for the LC717A30 is pending until the internal trigger signal which occurred after progress at appointed long interval time.
5. If internal trigger signal occurs, the new settings on all the registers are reflected to the LC717A30's operation. (That is to say, the LC717A30 waits for a processing start until the maximum time of

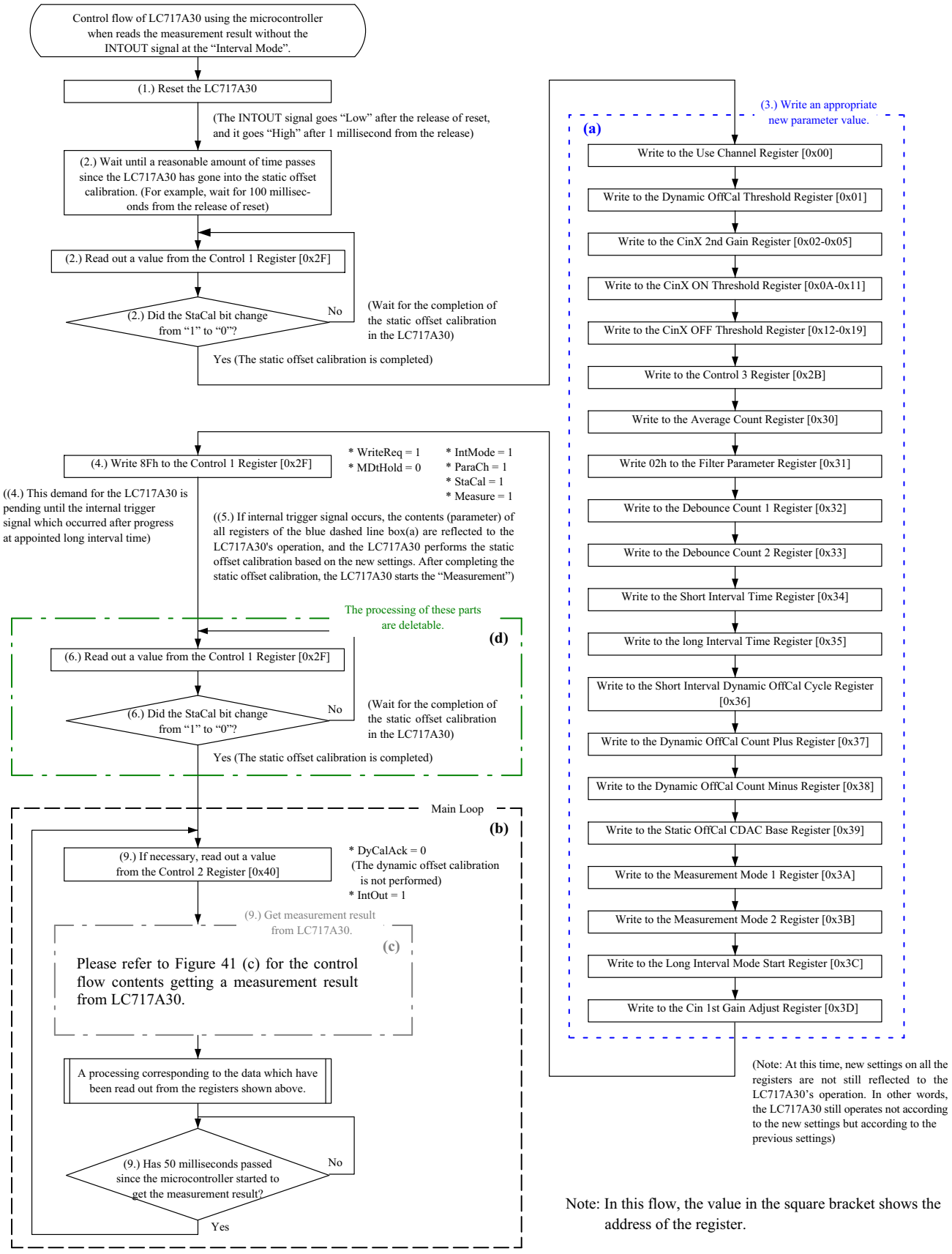
appointed long interval time. And the LC717A30 operates according to the new settings)

NOTE: In addition, when reflection of new setting is completed to the inside of the LC717A30, the INTOUT signal of the LC717A30 does negation (“Low” level) automatically. Furthermore, the Cin0 to Cin7 Data Register [Address=0x1A to 0x21], the Result Data Register [Address=0x2A], the Error Status Register [Address=0x2C] and the Error Channel Status Register [Address=0x2D] are all initialized into 00h. Particularly, please be careful about initializing the touch ON/OFF judgement result of all channels to OFF. And counters inside this LSI which are used for the processing of the dynamic offset calibration and the processing of debounce are all cleared.

6. The LC717A30 performs the static offset calibration based on the new settings. The microcontroller checks that the static offset calibration processing of LC717A30 has completed. (Specifically, the microcontroller reads the Control 1 Register [Address=0x2F] and waits until the StaCal bit becomes “0”)
7. After completing the static offset calibration, the LC717A30 starts the “Measurement”.
8. The LC717A30 completes the “Measurement”. After the time which is named the “Interval time” passed since the completion of the “Measurement”, the LC717A30 restarts next “Measurement” automatically.
9. The microcontroller retrieves a measurement result from registers such as Result Data Register [Address=0x2A] repeatedly without considering the timing (For example, at 50-millisecond intervals) when the “Measurement” of the LC717A30 has completed.

   NOTE: When the dynamic offset calibration is enforced, the DyCalAck bit in the Control 2 Register [Address=0x40] is set to “1”. Therefore, the microcontroller can confirm that the dynamic offset calibration was enforced by reading the Control 2 Register [Address=0x40].
10. The microcontroller repeats the above (9.).

The control flow figure corresponding to the control sequence described above is shown on the next page.



Note: In this flow, the value in the square bracket shows the address of the register.

Figure 43. Control Flow Example When the Microcontroller Reads the Measurement Result without the INTOUT Signal at the “Interval Mode”

In the case of Reading the Measurement Result with the INTOUT Signal at the "Sleep Mode"

The microcontroller is connected to the LC717A30 over I^2C bus or SPI, and a GPIO port of the microcontroller is connected to the INTOUT pin of the LC717A30, and another GPIO port is connected to the nRST pin. In such case, explains the control example when the microcontroller detects the assertion ("High" level) of the INTOUT signal and reads measurement results over the I^2C bus or SPI every time.

In this control example, the microcontroller always sets the LC717A30's operation mode to "Sleep Mode". (In concrete terms, the microcontroller always writes "0" to the IntMode bit in the Control 1 Register [Address=0x2F]) In addition, both the INTMD1 bit and the INTMD2 bit in the Measurement 1 Register [Address=0x3A] are always set to "0", so the LC717A30 always asserts ("High" level) the INTOUT immediately after the "Measurement" has completed and it doesn't negate ("Low" level) the INTOUT signal automatically.

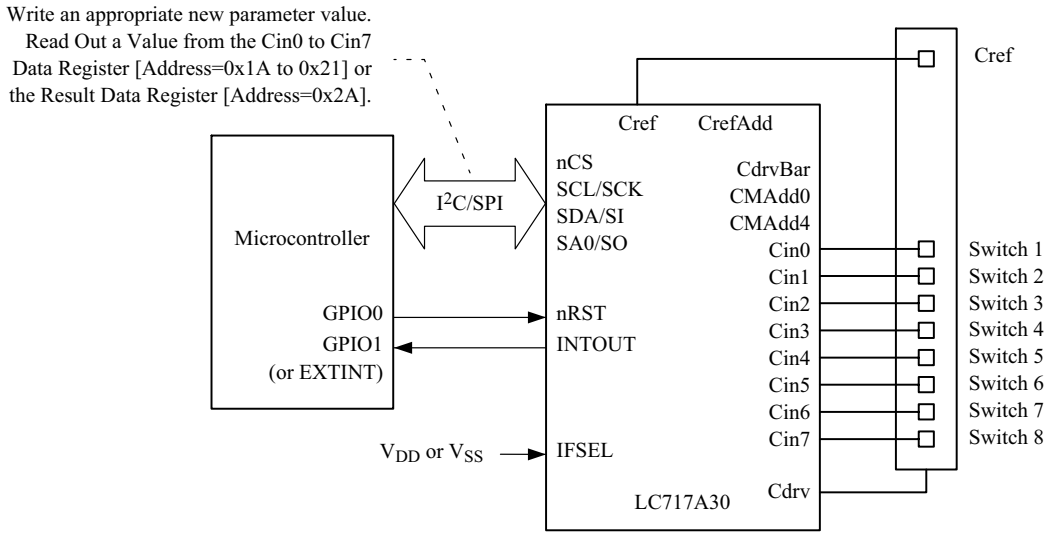


Figure 44. Connection (3) Between the Microcontroller and the LC717A30

1. The microcontroller resets the LC717A30 by controlling the nRST signal line via a GPIO port. (In concrete terms, the microcontroller outputs "Low" to nRST signal line, and then it outputs "High" to nRST signal line. The output from the GPIO port of the microcontroller, which is connected to the nRST pin, has to be kept "Low" for at least 1 microsecond)
2. After controlling the nRST signal line, the microcontroller checks the status of the INTOUT signal via another GPIO port. As soon as the microcontroller detects the rising edge of the INTOUT signal, it sets 80h to the Control 1 Register [Address=0x2F] over the I^2C bus or SPI. (To put it concretely, the microcontroller writes 80h to the Control 1 Register [Address=0x2F] within 5 milliseconds after the INTOUT signal goes "High" level)

   NOTE: By doing (2.), the execution of the static offset calibration and the "Measurement", which is performed automatically after initialization in the LC717A30, can be cancelled. (Conversely, if you allow the microcontroller to perform the static offset calibration and the subsequent measurement which are performed automatically by the LC717A30 according to the default setting of the LC717A30, the microcontroller need not do the processing described above, but the microcontroller usually has to wait at least until the static offset calibration has completed)
3. The LC717A30 goes to sleep shortly (Operation stop). The microcontroller writes an appropriate parameter value to each register of the LC717A30 over the I^2C bus or SPI. (For more information about registers the microcontroller may write a parameter to, refer to the inside of the blue dashed line box(a) on the control flow figure shown in Figure 45) Especially, In this example, the microcontroller writes "0" to both the INTMD1 bit and the INTMD2 bit in the Measurement 1 Register [Address=0x3A] so that the LC717A30 may not negate ("Low" level) the INTOUT signal automatically.

   NOTE: At this time, new settings on all the registers are not still reflected to the LC717A30's operation. (In other words, the LC717A30 still operates not according to the new settings but according to the previous settings)

4. The microcontroller writes 87h to the Control 1 Register [Address=0x2F] over the I^2C bus or SPI. And then, in order to negate (“Low” level) the INTOUT signal and wake up the LC717A30, the microcontroller writes 01h to the Control 2 Register [Address=0x40]. After wake up, the LC717A30 restarts operation.
5. After (4.), the new settings on all the registers are reflected to the LC717A30’s operation. (That is to say, the LC717A30 operates according to the new settings)

   NOTE: In addition, when reflection of new setting is completed to the inside of the LC717A30, the INTOUT signal of the LC717A30 does negation (“Low” level) automatically. Furthermore, the Cin0 to Cin7 Data Register [Address=0x1A to 0x21], the Result Data Register [Address=0x2A], the Error Status Register [Address=0x2C] and the Error Channel Status Register [Address=0x2D] are all initialized into 00h. Particularly, please be careful about initializing the touch ON/OFF judgement result of all channels to OFF. And counters inside this LSI which are used for the processing of the dynamic offset calibration and the processing of debounce are all cleared.
6. The LC717A30 performs the static offset calibration based on the new settings. After completing the static offset calibration, the LC717A30 starts the “Measurement”.
7. After the completion of the “Measurement”, the LC717A30 asserts (“High” level) the INTOUT signal. And then it goes to sleep. The microcontroller checks the assertion (“High” level) of the INTOUT signal in order to check that the LC717A30 has gone to sleep. After detecting the assertion (“High” level) of the INTOUT signal, the microcontroller reads measurement results from the Result Data Register [Address=0x2A] and so on.

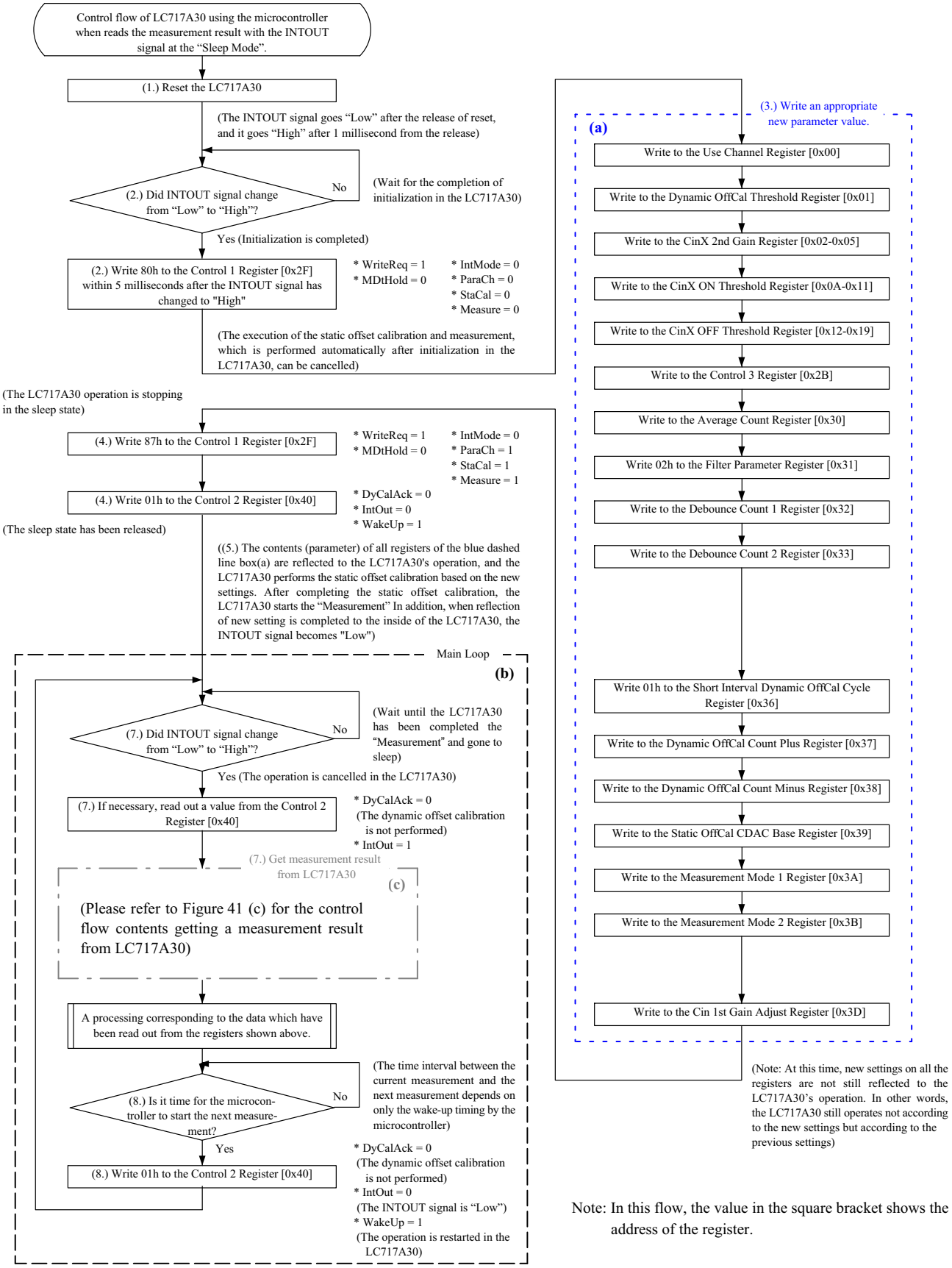
   NOTE: At the time of the completion of the “Measurement”, the LC717A30 outputs “High” to the INTOUT signal line. When the dynamic offset calibration is enforced, the DyCalAck bit in the Control 2 Register [Address=0x40] is set to “1” at the same time IntOut bit is set to “1”, and the LC717A30 asserts (“High” level) the INTOUT signal. Therefore, the microcontroller can confirm that the dynamic offset calibration was enforced by reading the Control 2 Register [Address=0x40] after having confirmed assertion (“High” level) of the INTOUT signal.
8. The microcontroller waits until it is time to wake up the LC717A30.
9. If it is time for the microcontroller to start the next measurement, the microcontroller writes 01h to the Control 2 Register [Address=0x40].
10. The microcontroller repeats the above (7.) through (10.).

The control flow figure corresponding to the control sequence described above is shown on the next page.

Note: The important thing about “Sleep Mode”.

When the LC717A30 operating in the sleep mode performed sleep (Operation stop), please be careful about the following conditions.

- If the LC717A30 has gone to sleep, the LC717A30 doesn’t resume its operation as long as the microcontroller doesn’t wake up the LC717A30.
- The time interval between the current measurement and the next measurement depends on only the wake-up timing of the LC717A30 by the microcontroller. (In a word, the microcontroller determines the time interval)
- In the case of the “Sleep Mode”, the LC717A30 does not refer to contents of the Short Interval Time Register [Address=0x34], the Long Interval Time Register [Address=0x35] and the Long Interval Mode Start Count Register [Address=0x3C] setting. (In other words, the LC717A30 ignores those setting, because the sleep mode does not have the period of interval)
- When the sleep mode is selected, be sure to set the Short Interval Dynamic OffCal Cycle Register[Address=0x36] to 01h. In this time, the number of execution cycles for the judgment of the dynamic offset calibration operation is once every 1 measurement at the time of the short interval mode.



Note: In this flow, the value in the square bracket shows the address of the register.

Figure 45. Control Flow Example When the Microcontroller Reads the Measurement Result with the INTOUT Signal at the “Sleep Mode”

In the Case of Reading and Writing of the CdacP/CdacM/DigitalOffset Registers

The LC717A30 can read and write from a microcontroller with the offset capacity value (CdacP/CdacM) and digital offset value of all channels which adjusts by enforcement of the static offset calibration and the dynamic offset calibration.

The microcontroller writes the setting corresponding to a channel targeted for Cin0 to Cin3 or Cin4 to Cin7 in the CdacSel bit of the Control 3 Register [Address=0x2B]. These registers are controllable with four channels at a time. When the CdacSel bit is set to "0", the microcontroller can read and write the CdacP/CdacM/ DigitalOffset registers from Cin0 to Cin3. Otherwise, when the CdacSel bit is set to "1", the microcontroller can read and write the CdacP/CdacM/DigitalOffset registers from Cin4 to Cin7.

When the value of the CdacP/CdacM/DigitalOffset registers written with the microcontroller, the microcontroller enforces changing parameters processing by the ParaCh bit in the Control 1 Register [Address= 0x2F] is set to "1", and reflected inside the LC717A30 by changing parameters, the following processing changes. In addition, after having changed the target channels by the CdacSel bit, the value of new CdacP/CdacM/DigitalOffset reflects it to registers when the measurement processing is completed.

In this control example, the microcontroller reads and writes values of the CdacP/CdacM/DigitalOffset.

1. After releasing a reset on the nRST signal line, the microcontroller checks the status of the INTOUT. As soon as the microcontroller detects the rising edge of the INTOUT signal, it sets 88h to the Control 1 Register [Address=0x2F] over the I^2C bus or SPI. (To put it concretely, the microcontroller writes 88h to the Control 1 Register [Address=0x2F] within 5 milliseconds after the INTOUT signal goes "High" level)

   NOTE: By doing (1.), the execution of the static offset calibration and "Measurement", which is performed automatically after initialization in the LC717A30, can be cancelled. (Conversely, if you allow the microcontroller to perform the static offset calibration and the subsequent measurement which are performed automatically by the LC717A30 according to the default setting of the LC717A30, the microcontroller need not do the processing described above, but the microcontroller usually has to wait at least until the static offset calibration has completed)
2. The microcontroller writes an appropriate parameter value to each register of the LC717A30 over the I^2C bus or SPI.

   NOTE: At this time, new settings on all the registers are not still reflected to the LC717A30's operation (In other words, the LC717A30 still operates not according to the new settings but according to the previous settings).
   In addition, we recommend that we write values for stopping enforcement of the dynamic offset calibration to the registers (0x01, 0x36 to 0x38 and the PDCLP bit in the 0x3A) relating to the dynamic offset calibration because the values of the CdacP/CdacM/DigitalOffset are replaced by the dynamic offset calibration having been enforced.
3. To reflect the new settings to the LC717A30's operation and to make the LC717A30 perform the static offset calibration and the "Measurement", the microcontroller writes 8Fh to the Control 1 Register [Address=0x2F] over the I^2C bus or SPI. This demand for the LC717A30 is pending until the internal trigger signal which occurred after progress at appointed long interval time.
4. If internal trigger signal occurs, the new settings on all the registers are reflected to the LC717A30's operation (That is to say, the LC717A30 operates according to the new settings). The LC717A30 performs the static offset calibration based on the new settings. After completing the static offset calibration, the LC717A30 starts the "Measurement".
5. Firstly, In order to check the completion of the measurement in the LC717A30, the microcontroller checks the assertion ("High" level) of the INTOUT signal. After confirmation, the microcontroller reads the Cin0 to Cin3 CDAC Plus Register and Cin0 to Cin3 CDAC Minus Register [Address=0x22 to 0x29]. Furthermore, it reads the Cin0 to Cin3 Digital Offset Register [Address=0x06 to 0x09].
6. The microcontroller wrote 90h (CdacSel="1") to the Control 3 Register [Address=0x2B] for changing the target channels from Cin4 to Cin7.

   NOTE: At this time, the CdacP/CdacM/ DigitalOffset registers are not still reflected to a value from Cin4 to Cin7. After having changed the target channels by the CdacSel bit, if the measurement processing is completed, it is reflected to registers.

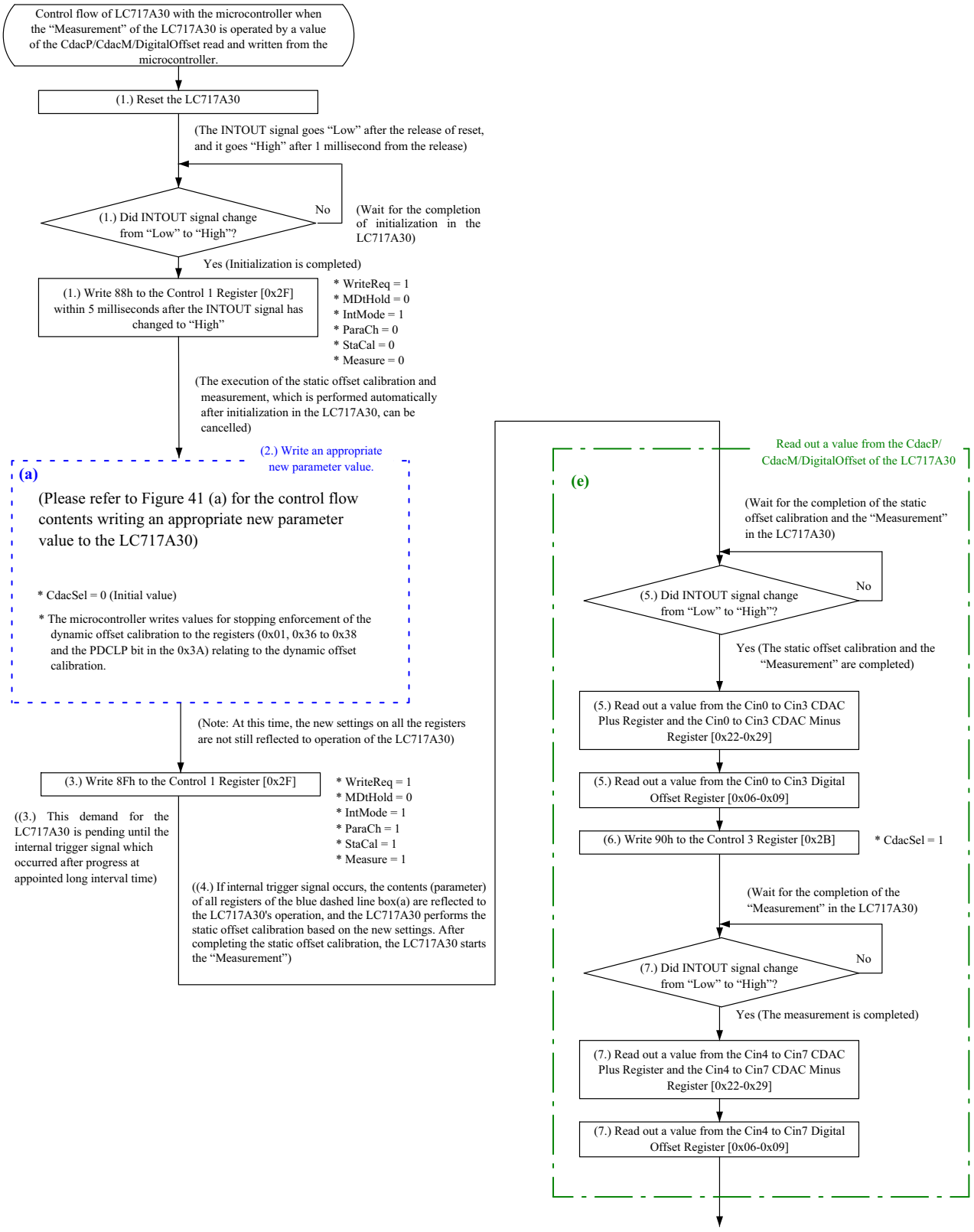
7. Next, In order to check the completion of the measurement in the LC717A30, the microcontroller checks the assertion (“High” level) of the INTOUT signal. After confirmation, the microcontroller reads the Cin4 to Cin7 CDAC Plus Register and Cin4 to Cin7 CDAC Minus Register [Address=0x22 to 0x29]. Furthermore, it reads the Cin4 to Cin7 Digital Offset Register [Address=0x06 to 0x09].
8. The microcontroller writes to the new parameters in the Cin4 to Cin7 CDAC Plus Register and Cin4 to Cin7 CDAC Minus Register [Address=0x22 to 0x29]. Furthermore, it writes to the new parameters in the Cin4 to Cin7 Digital Offset Register [Address=0x06 to 0x09].

   NOTE: At this time, new settings on all the registers are not still reflected to the LC717A30’s operation (In other words, the LC717A30 still operates not according to the new settings but according to the previous settings).
9. To reflect the new settings to the LC717A30’s operation, the microcontroller writes 8Dh to the Control 1 Register [Address=0x2F] over the I^2C bus or SPI. (In this time, the microcontroller does not enforce the static offset calibration because the values of the CdacP/CdacM/DigitalOffset are replaced by the static offset calibration having been enforced)
10. The microcontroller wrote 80h (CdacSel =“1”) to the Control 3 Register [Address=0x2B] for changing the target channels from Cin0 to Cin3.

    NOTE: At this time, the CdacP/CdacM/DigitalOffset registers are not still reflected to a value from Cin0 to Cin3. After having changed the target channels by the CdacSel bit, if the measurement processing is completed, it is reflected to registers.
11. The microcontroller writes to the new parameters in the Cin0 to Cin3 CDAC Plus Register and Cin0 to Cin3 CDAC Minus Register [Address=0x22 to 0x29]. Furthermore, it writes to the new parameters in the Cin0 to Cin3 Digital Offset Register [Address=0x06 to 0x09].

    NOTE: At this time, new settings on all the registers are not still reflected to the LC717A30’s operation (In other words, the LC717A30 still operates not according to the new settings but according to the previous settings).
12. Finally, to reflect the new settings to the LC717A30’s operation, the microcontroller writes 8Dh to the Control 1 Register [Address=0x2F] over the I^2C bus or SPI. (In this time, the microcontroller does not enforce the static offset calibration because the values of the CdacP/CdacM/DigitalOffset are replaced by the static offset calibration having been enforced)
13. In order to check the completion of the measurement in the LC717A30, the microcontroller checks the assertion (“High” level) of the INTOUT signal. After detecting the assertion (“High” level) of the INTOUT signal, the microcontroller writes 00h to the Control 2 Register [Address=0x40] to negate (“Low” level) the INTOUT signal, and it reads measurement results from the Result Data Register [Address=0x2A] and so on.
14. After the elapse of a predetermined time (Either the short interval time or the long interval time) from the completion of the “Measurement”, the LC717A30 starts the next “Measurement” automatically.
15. The microcontroller repeats the above (13.) through (14.).

The control flow figure corresponding to the control sequence described above is shown on the next page.

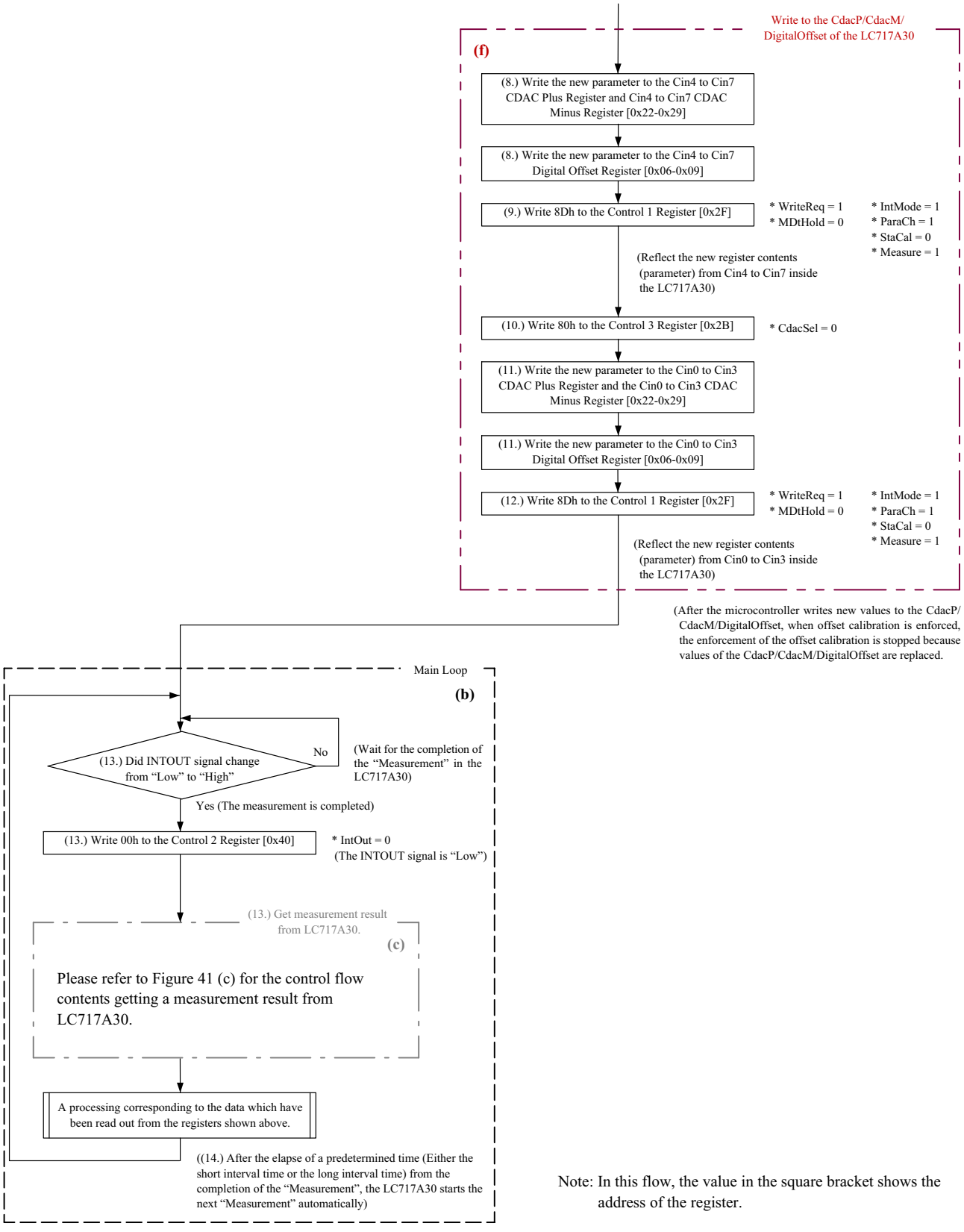


Note: In this flow, the value in the square bracket shows the address of the register.

Continued to the next page.

Figure 46. Control Flow Example When the Microcontroller Reads and Writes Values of the CdacP/CdacM/DigitalOffset

Continued from the previous page.



Note: In this flow, the value in the square bracket shows the address of the register.

Figure 46. Control Flow Example When the Microcontroller Reads and Writes Values of the CdacP/CdacM/DigitalOffset

In the case of Reading the Measurement Result Using Two LC717A30

When application constitution uses two LC717A30, the control from the microcontroller is necessary because the LC717A30 does not have the hardware which connects LSI to LSI and synchronizes. If the switch space on the board is near, an accurate measurement may be impossible because an electrical flux line between Cdrv and Cdrv influences it by Cdrv signal drive. We recommend a method to operate each LSI by the microcontroller in turn to enforce an accurate measurement. (The microcontroller controls the LC717A30 using the sleep mode) When the sleep mode is used, the time interval between the current measurement and the next measurement depends on only the wake-up timing by the microcontroller. In addition, the dynamic offset calibration function can use even the sleep mode and can read the Cin0 to Cin7 Data Register (AD level) and Result Register (Touch ON/OFF judgement result) from the microcontroller anytime.

If the microcontroller operates the LC717A30 in the interval mode, the LC717A30 doesn't start the "Measurement" for the order from the microcontroller immediately. And the elapse of a predetermined time (Either the short interval time or the long interval time) from the completion of the "Measurement", the LC717A30 starts the next "Measurement" automatically. Therefore, we do not recommend it because unevenness occurs in the measurement interval. However, If the microcontroller operates the LC717A30 in the interval mode without minding the measurement interval, there is the method to control the "Measurement" operation of each LSI in the Measure bit in the Control 1 Register [Address=0x2F]. In this time, The MDtHold bit in the Control 1 Register [Address=0x2F] was set to "0" in an initial setting processing of the LC717A30. Thereby, when the Measure bit is set to "0", a value of Cin0 to Cin7 Data Register [Address=0x1A to 0x29] and Result Register [Address= 0x2A] is cleared. Therefore, the microcontroller cannot enforce the "Measurement" with each LSI in turn so that an electrical flux line by each other's Cdrv drive is not affected. Consequently, when the MDtHold and the WriteReq bits in the Control 1 Register [Address=0x2F] are set to "1" and it is reflected inside of the LC717A30, the value of the Cin0 to Cin7 Data Register [Address= 0x1A to 0x29] and Result Register [Address=0x2A] is maintained without clearing it.

In such case, explains the control example of the application that a microcontroller controlled LC717A30 in the sleep mode using two LC717A30.

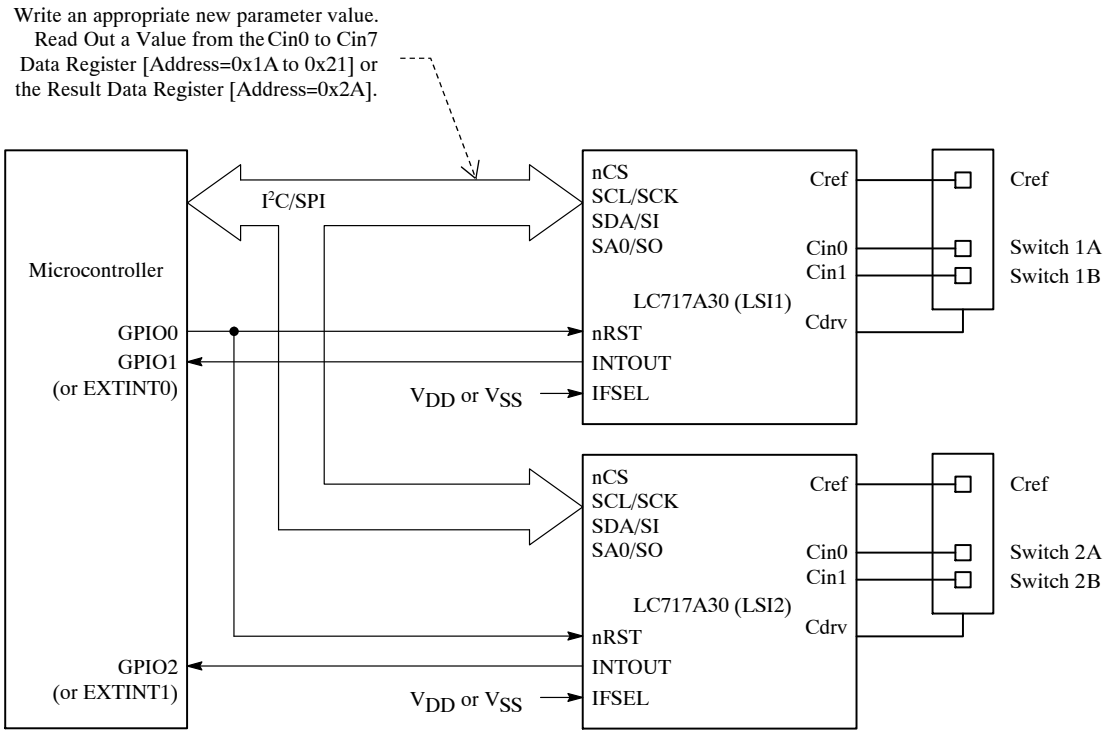


Figure 47. Connection (5) Between the Microcontroller and the LC717A30

1. The microcontroller resets the LSI1 and the LSI2 by controlling the nRST signal line via a GPIO port. (In concrete terms, the microcontroller outputs “Low” to nRST signal line, and then it outputs “High” to nRST signal line. The output from the GPIO port of the microcontroller, which is connected to the nRST pin, has to be kept “Low” for at least 1 microsecond)
2. After controlling the nRST signal line, the microcontroller checks the status of the INTOUT signal via another GPIO port. As soon as the microcontroller detects the both rising edge of the INTOUT signal of the LSI1 and the LSI2, it sets 90h to the Control 1 Register [Address=0x2F] over the I^2C bus or SPI for the LSI1 and the LSI2. (To put it concretely, the microcontroller writes 90h to the Control 1 Register [Address=0x2F] within 5 milliseconds after the INTOUT signal goes “High” level)

   NOTE: By doing (2.), the execution of the static offset calibration and “Measurement”, which is performed automatically after initialization in the LC717A30, can be cancelled.
3. The microcontroller writes an appropriate parameter value to each register of the LSI1 and the LSI2 over the I^2C bus or SPI. (For more information about registers the microcontroller may write a parameter to, refer to the inside of the blue dashed line box(a) on the control flow figure shown in Figure 48)
   Especially, in this example, the microcontroller writes “0” to both the INTMD1 bit and the INTMD2 bit in the Measurement 1 Register [Address=0x3A] so that the LC717A30 may not negate (“Low” level) the INTOUT signal automatically.

   NOTE: At this time, new settings on all the registers are not still reflected to operation of the LSI1 and the LSI2. (In other words, the LC717A30 still operates not according to the new settings but according to the previous settings)
4. The microcontroller writes 97h to the Control 1 Register [Address=0x2F] over the I^2C bus or SPI. And then, in order to negate (“Low” level) the INTOUT signal and wake up the LSI1, the microcontroller writes 01h to the Control 2 Register [Address=0x40]. After wake up, the LSI1 restarts operation.
5. After (4.), the new settings on all the registers are reflected to operation of the LSI1 (That is to say, the LSI1 operates according to the new settings), and the LSI1 performs the static offset calibration based on the new settings. After completing the static offset calibration, the LSI1 starts the “Measurement”.

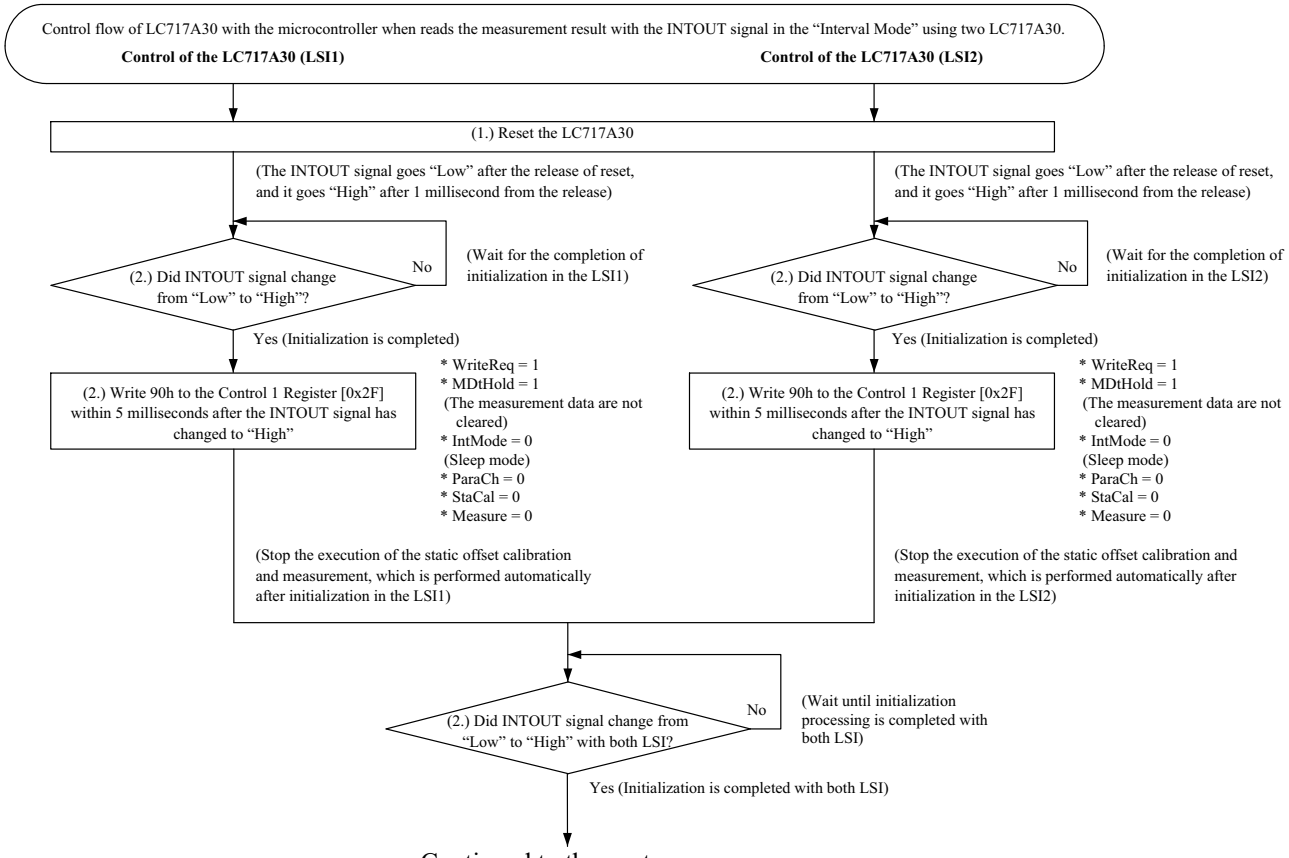
   NOTE: In addition, when reflection of new setting is completed to the inside of the LC717A30, the INTOUT signal of the LC717A30 does negation (“Low” level) automatically. Furthermore, the Cin0 to Cin7 Data Register [Address=0x1A to 0x21], the Result Data Register [Address=0x2A], the Error Status Register [Address=0x2C] and the Error Channel Status Register [Address=0x2D] are all initialized into 00h. Particularly, please be careful about initializing the touch ON/OFF judgement result of all channels to OFF. And counters inside this LSI which are used for the processing of the dynamic offset calibration and the processing of debounce are all cleared.
6. After the completion of the “Measurement”, the LSI1 asserts (“High” level) the INTOUT signal. And then it goes to sleep. The microcontroller checks the assertion (“High” level) of the INTOUT signal in order to check that the LSI1 has gone to sleep.

   NOTE: At the time of the completion of the “Measurement”, the LC717A30 outputs “High” to the INTOUT signal line.
7. After detecting the assertion (“High” level) of the INTOUT signal, the microcontroller writes 97h to the Control 1 Register [Address=0x2F] over the I^2C bus or SPI. And then, in order to negate (“Low” level) the INTOUT signal and wake up the LSI2, the microcontroller writes 01h to the Control 2 Register [Address=0x40]. After wake up, the LSI2 restarts operation.
8. After (7.), the new settings on all the registers are reflected to operation of the LSI2 (That is to say, the LSI2 operates according to the new settings), and the LSI2 performs the static offset calibration based on the new settings. After completing the static offset calibration, the LSI2 starts the “Measurement”.
9. After the completion of the “Measurement”, the LSI2 asserts (“High” level) the INTOUT signal. And then it goes to sleep. The microcontroller checks the assertion (“High” level) of the INTOUT signal in order to check that the LSI2 has gone to sleep.
10. The microcontroller waits until it is time to wake up the LSI1 and the LSI2.
11. If it is time for the microcontroller to start the next measurement, the microcontroller writes 01h to the Control 2 Register [Address=0x40] of the LSI1 over the I^2C bus or SPI. And then, the INTOUT signal of the LSI1 does negation (“Low” level) and the LSI1 restarts operation.
12. After the completion of the “Measurement”, the LSI1 asserts (“High” level) the INTOUT signal. And then it goes to sleep. The microcontroller checks the assertion (“High” level) of the INTOUT signal in order to check that the LSI1 has gone to sleep.
13. Next, if it is time for the microcontroller to start the next measurement, the microcontroller writes 01h to

the Control 2 Register [Address=0x40] of the LSI2 over the I^2C bus or SPI. And then, the INTOUT signal of the LSI2 does negation (“Low” level) and the LSI2 restarts operation.

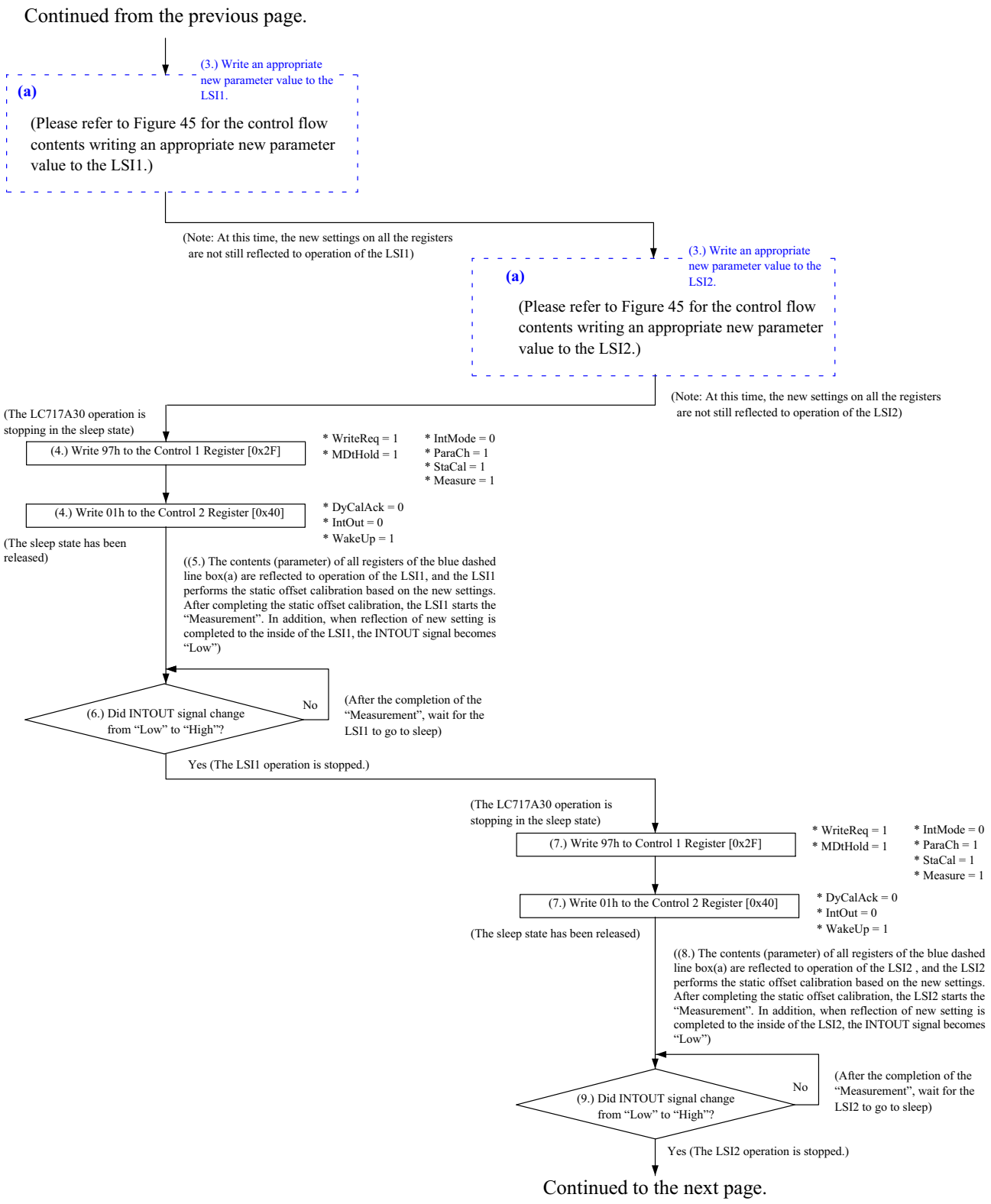
14. After the completion of the “Measurement”, the LSI2 asserts (“High” level) the INTOUT signal. And then it goes to sleep. The microcontroller checks the assertion (“High” level) of the INTOUT signal in order to check that the LSI2 has gone to sleep.
15. Finally, the microcontroller reads measurement results from the Result Data Register [Address=0x2A] of LSI1 and LSI2 and so on.
16. The microcontroller repeats the above (10.) through (15.) The time interval between the current measurement and the next measurement depends on only the timing by the microcontroller.

The control flow figure corresponding to the control sequence described above is shown in follows.



Note: In this flow, the value in the square bracket shows the address of the register.

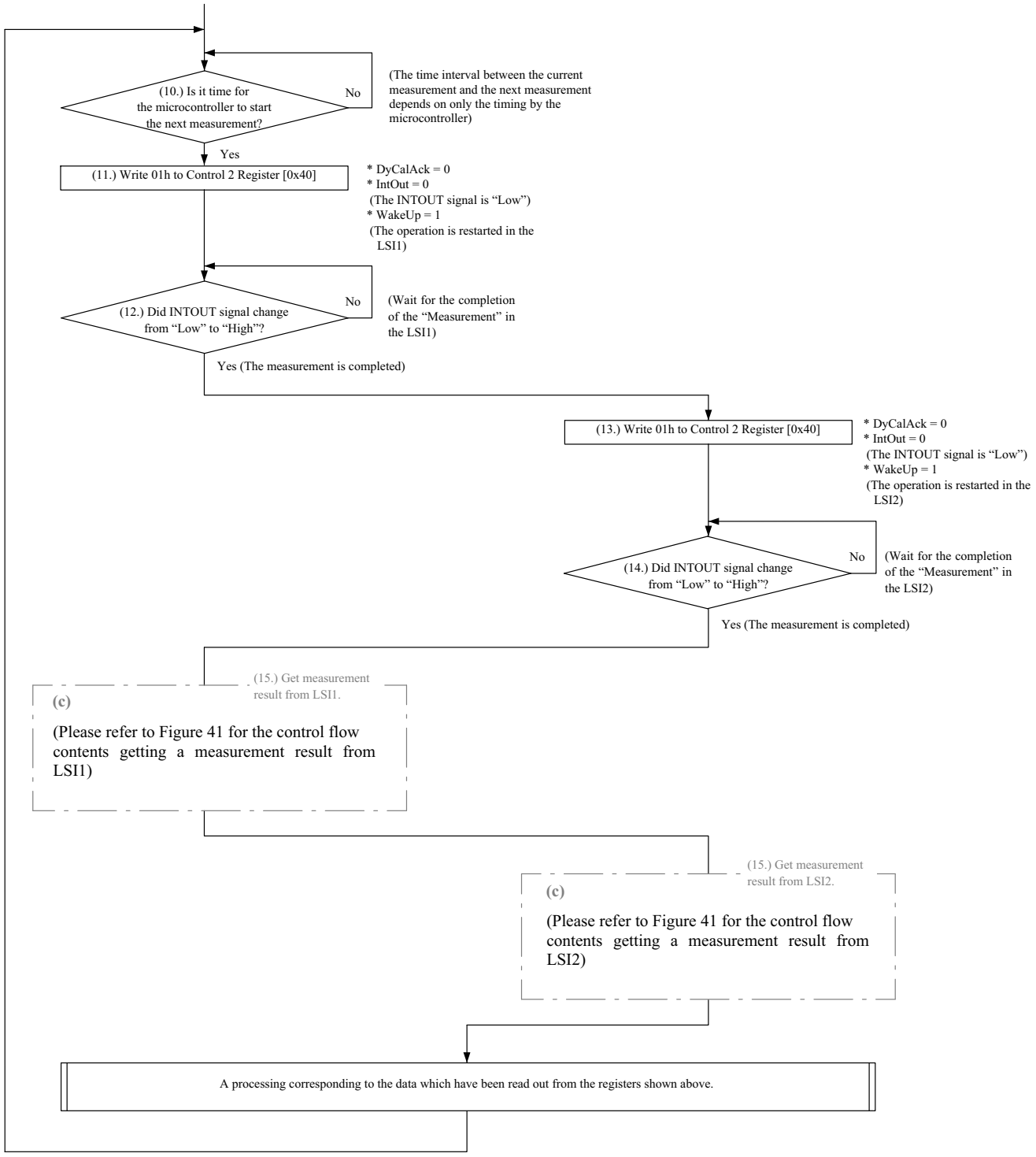
Figure 48. Control Flow Example When the Microcontroller Reads the Measurement Result Using Two LC717A30



Note: In this flow, the value in the square bracket shows the address of the register.

Figure 48. Control Flow Example When the Microcontroller Reads the Measurement Result Using Two LC717A30

Continued from the previous page.



Note: In this flow, the value in the square bracket shows the address of the register.

Figure 48. Control Flow Example When the Microcontroller Reads the Measurement Result Using Two LC717A30

In the Case of the Sensitivity Adjustment

1. The microcontroller writes the setting parameters necessary for sensitivity adjustment to each register of the LC717A30 over the I^2C bus or SPI.

   NOTE: At this time, new settings on all the registers are not still reflected to the LC717A30's operation. (In other words, the LC717A30 still operates not according to the new settings but according to the previous settings)

- Cin0 toCin7 ON Threshold Register [Address= 0x0A to 0x11] are set to 0Ah (AD level=10).
- Cin0 to Cin7 OFF Threshold Register [Address= 0x12 to 0x19] are set to 07h (AD level=7).
- To stop the dynamic offset calibration enforcement, set 00h to the Dynamic OffCal Count Plus Register [Address=0x37].

2. You release the finger from a switch pattern of Cin.
3. To reflect the new settings to the LC717A30's operation and to make the LC717A30 perform the static offset calibration and the "Measurement", the microcontroller writes 8Fh to the Control 1 Register [Address=0x2F] over the I^2C bus or SPI.
4. After (3.), the new settings on all the registers are reflected to the LC717A30's operation (That is to say, the LC717A30 operates according to the new settings). And the LC717A30 performs the static offset calibration based on the new settings. After completing the static offset calibration, the LC717A30 starts the "Measurement".
5. In the state that you touched with the finger a switch pattern of Cin, the microcontroller confirms the AD level of the Cin0 to Cin7 Data Register [Address=0x1A to 0x21].
6. You release the finger from a switch pattern of Cin.
7. Adjust the Cin0 to Cin7 2^{nd} Gain Register [Address= 0x02 to 0x05] so that AD level of the Cin0 to Cin7 Data Register [Address=0x1A to 0x21] becomes about 20 (14h) to 25 (19h). (Please use the gain of the 1^{st}-amplifier of the Cin 1^{st} Gain Adjust Register [Address=0x3D] basically in 00h (Minimum gain))

   NOTE: At this time, new settings on all the registers are not still reflected to the LC717A30's operation. (In other words, the LC717A30 still operates not according to the new settings but according to the previous settings)

8. To reflect the new settings to the LC717A30's operation and to make the LC717A30 perform the static offset calibration and the "Measurement", the microcontroller writes 8Fh to the Control 1 Register [Address=0x2F] over the I^2C bus or SPI.
9. After (8.), the new settings on all the registers are reflected to the LC717A30's operation (That is to say, the LC717A30 operates according to the new settings). And the LC717A30 performs the static offset calibration based on the new settings. After completing the static offset calibration, the LC717A30 starts the "Measurement".
10. In the state that you touched with the finger a switch pattern of Cin, the microcontroller confirms the AD level of the Cin0 to Cin7 Data Register [Address=0x1A to 0x21].
11. The microcontroller repeats the above (6.) through (10.).

    NOTE: After completing the sensitivity adjustment, when you want to enforce the dynamic offset calibration, the microcontroller set the registers (0x01, 0x36 to 0x38 and the PDCLP bit in the 0x3A) relating to the Dynamic Offset Calibration.

The control flow figure corresponding to the control sequence described above is shown on the next page.

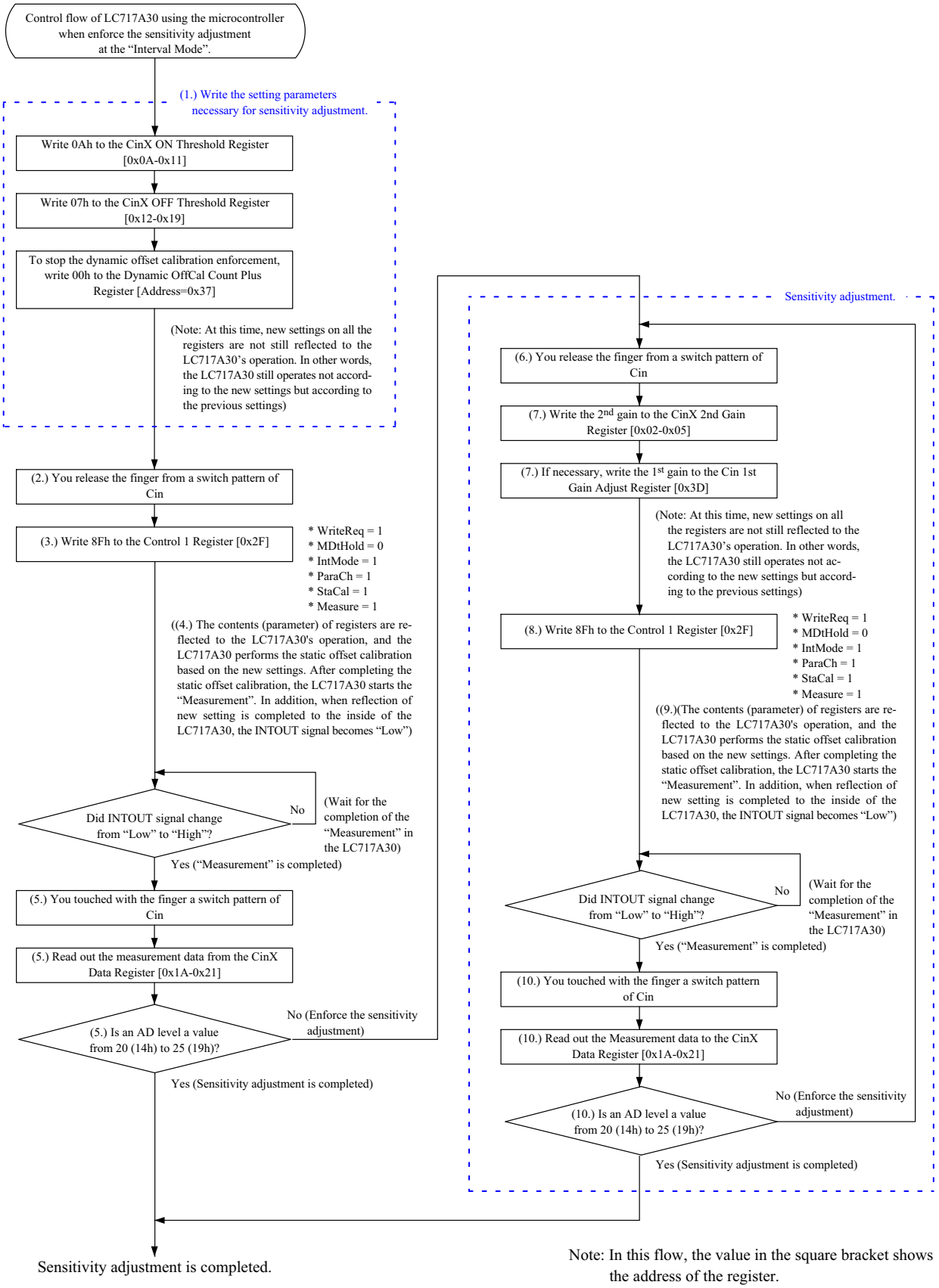


Figure 49. Control Flow Example When the Sensitivity Adjustment

Introduction of the Failsafe Function

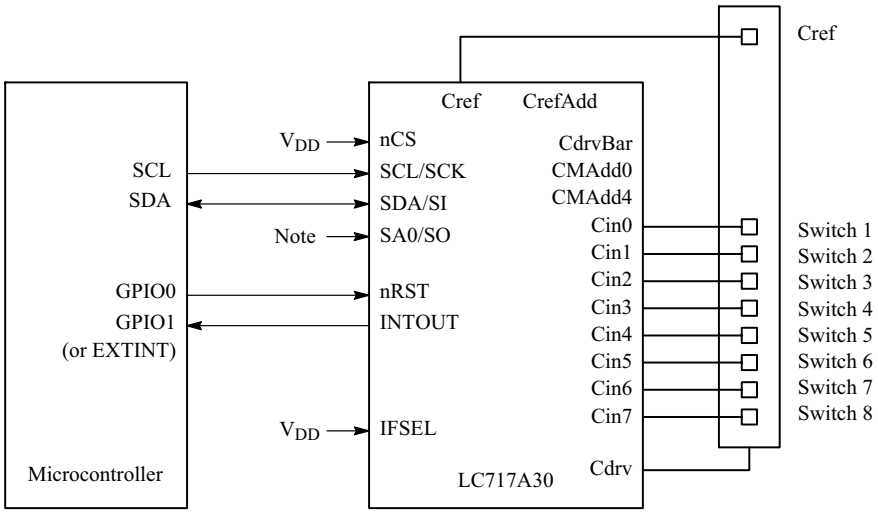
The “Touch-ON Automatic Cancellation Function” is a fail-safe function. When a finger does not touch it and has become the touch ON state in some kind of environmental factors by any chance, this function operates as a touch ON state does not continue forever. For example, if the touch ON state continues ten seconds, changing to the touch OFF state forcibly.

The LC717A30 does not have the “Touch-ON Automatic Cancellation Function”. Therefore, you need to implement the auto touch-off function to the firmware of microcontroller for a fail-safe. For example, when a periodical or abnormal AD level lasted a fixed period of time, we recommend initialization (The changing parameters and the static offset calibration by the Control 1 Register [Address=0x2F]) or reset of the LC717A30 for a fail-safe.

The LC717A30 has the offset calibration function for supporting the aging of sensor board and the change of temperature, however, when operating time is long (For example, it continues operating for 24 hours), we recommend initialization (The changing parameters and the static offset calibration by the Control 1 Register [Address=0x2F]) of the LC717A30 periodically for a fail-safe.

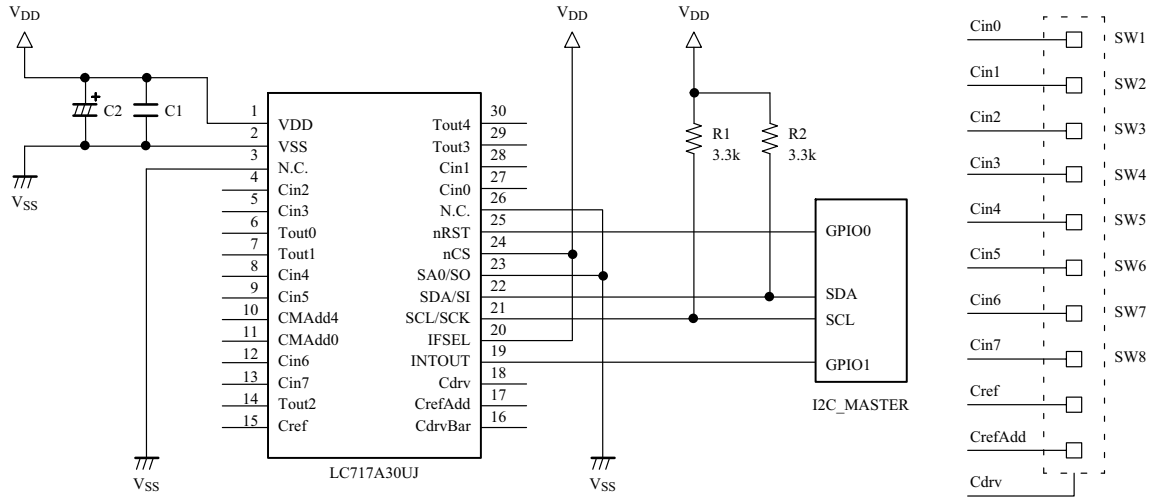
APPLICATION CIRCUIT EXAMPLES

Configuration Using I²C Bus Interface



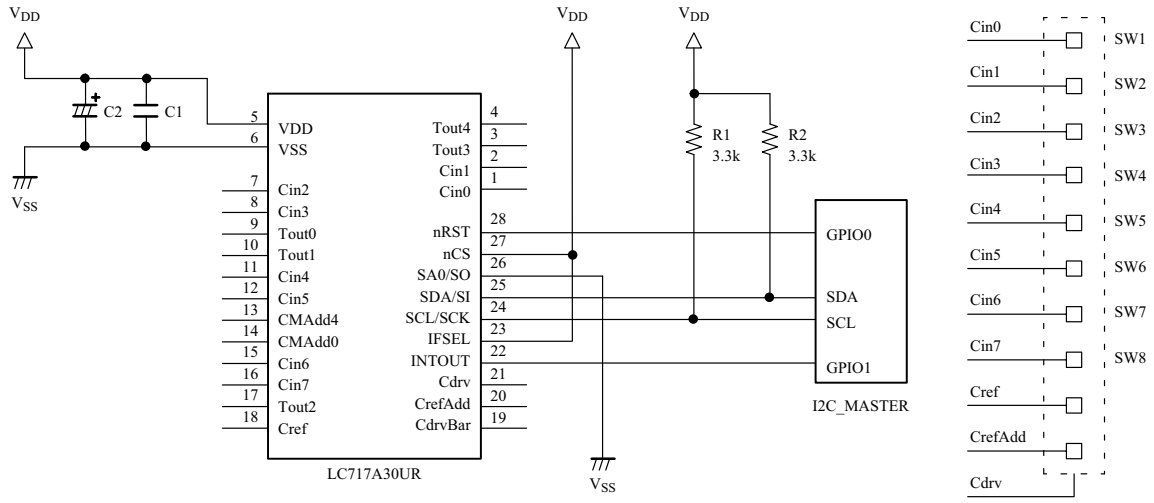
NOTE: Choice of two kinds of slave addresses is possible by SA0 pin.

Figure 50. Connection Configuration Example Using I²C Bus Interface



NOTE: For noise de-coupling place a high-valued capacitor(C2) and a low-valued capacitor(C1) in parallel between V_{DD} and V_{SS}. The small-valued capacitor(C1), at least 0.1 μF, should be mounted near the LSI.

Figure 51. LC717A30UJ's Application Circuit Example Using the I²C Bus Interface



NOTE: For noise de-coupling place a high-valued capacitor(C2) and a low-valued capacitor(C1) in parallel between V_{DD} and V_{SS}. The small-valued capacitor(C1), at least 0.1 μF, should be mounted near the LSI.

Figure 52. LC717A30UR's Application Circuit Example Using the I²C Bus Interface

Configuration Using SPI Interface

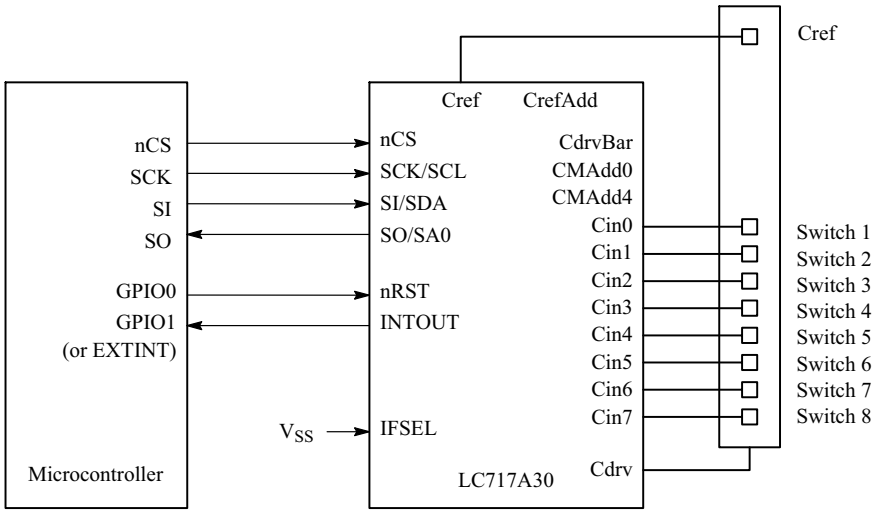
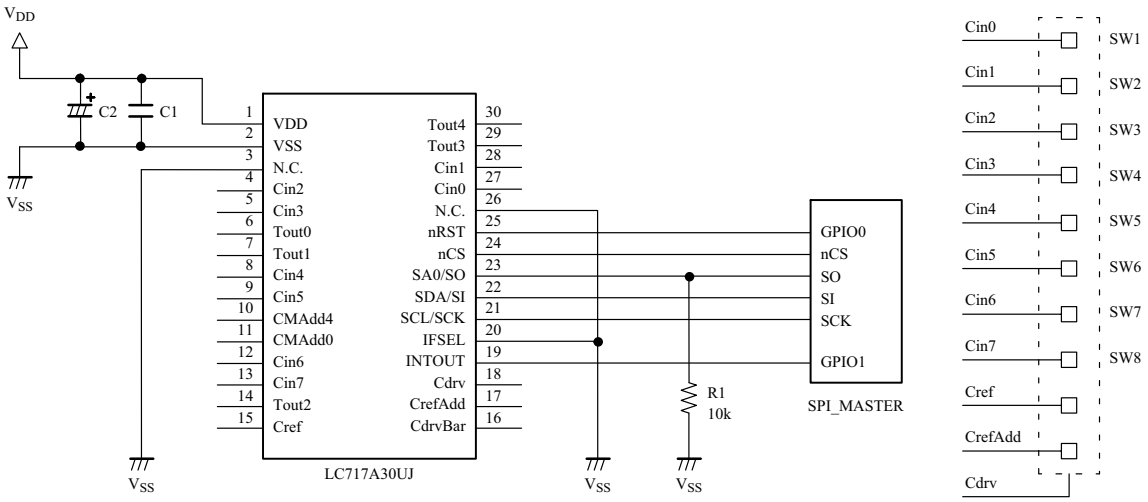
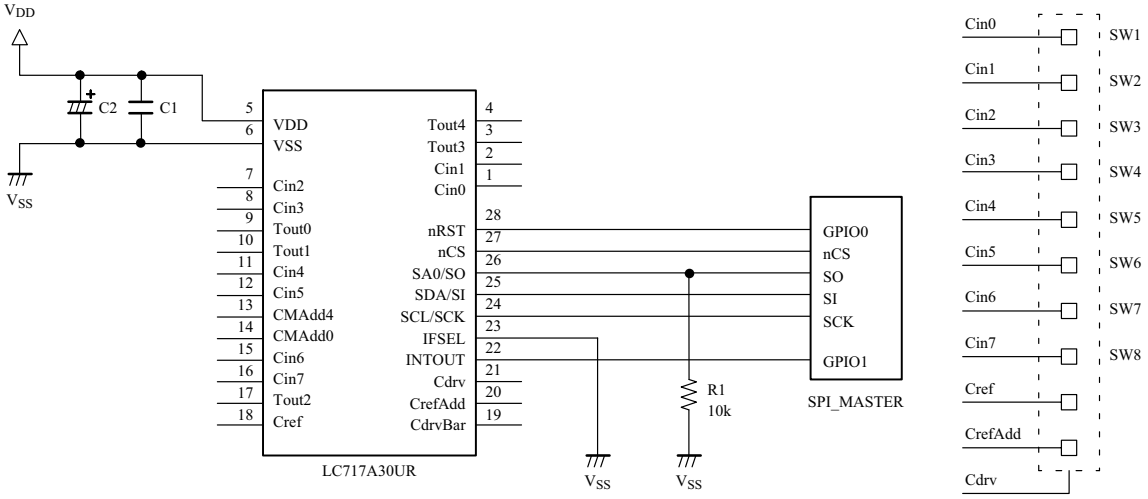


Figure 53. Connection Configuration Example Using SPI Interface



NOTE: For noise de-coupling place a high-valued capacitor (C2) and a low-valued capacitor (C1) in parallel between V_{DD} and V_{SS}. The small-valued capacitor (C1), at least 0.1 μF, should be mounted near the LSI.

Figure 54. LC717A30UJ's Application Circuit Example Using the SPI Interface

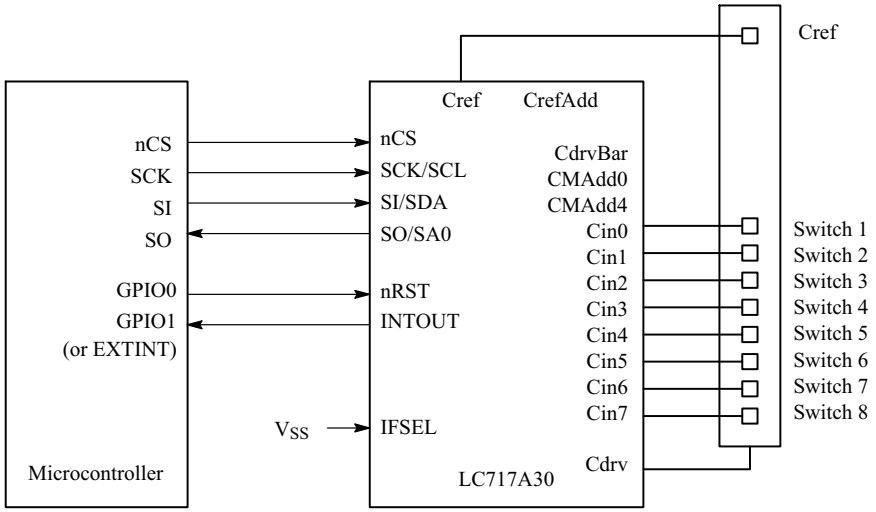


NOTE: For noise de-coupling place a high-valued capacitor (C2) and a low-valued capacitor (C1) in parallel between V_{DD} and V_{SS}. The small-valued capacitor (C1), at least 0.1 μF, should be mounted near the LSI.

Figure 55. LC717A30UR's Application Circuit Example Using the SPI Interface

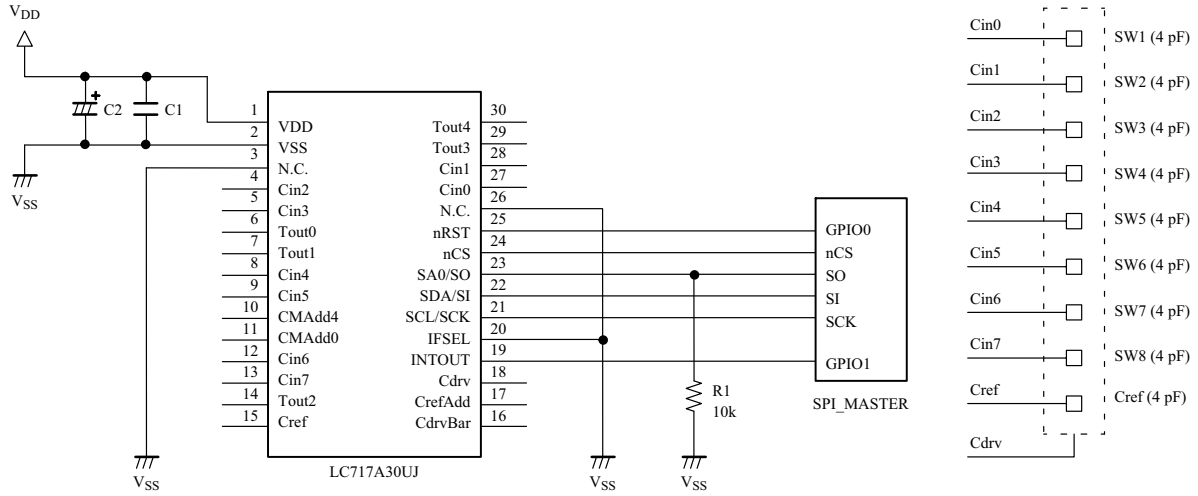
Configuration by Value of Sensor Capacitive

(1) Configuration of Small Capacitive Sensors (8 pF or less)



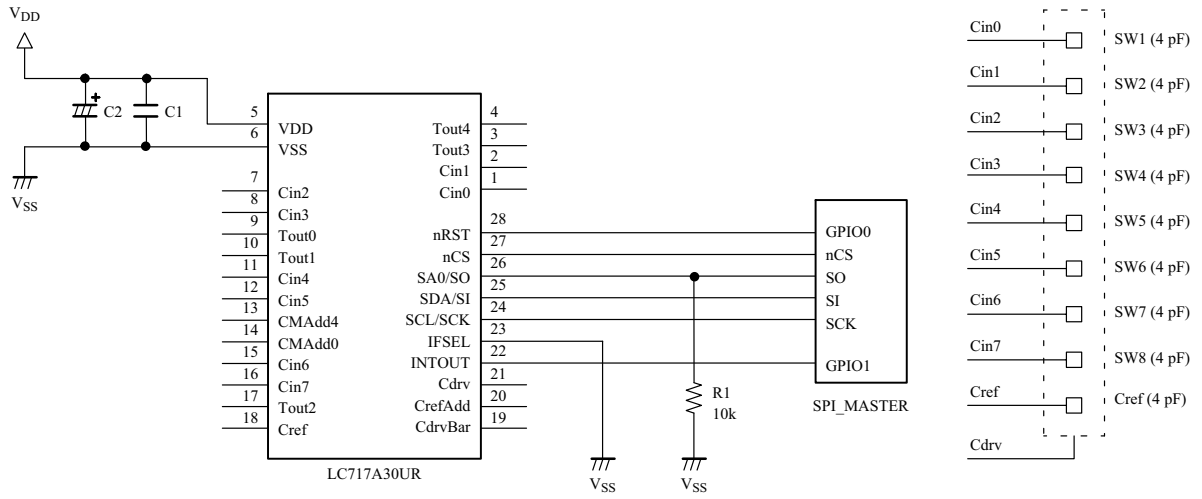
NOTE: Constitute a relation of CinX (X = 0 to 7) = CdacM and Cref = CdacP.

Figure 56. Connection Configuration Example of Small Capacitive Sensors (8 pF or less)



NOTE: For noise de-coupling place a high-valued capacitor (C2) and a low-valued capacitor (C1) in parallel between V_{DD} and V_{SS}. The small-valued capacitor (C1), at least 0.1 μF, should be mounted near the LSI.

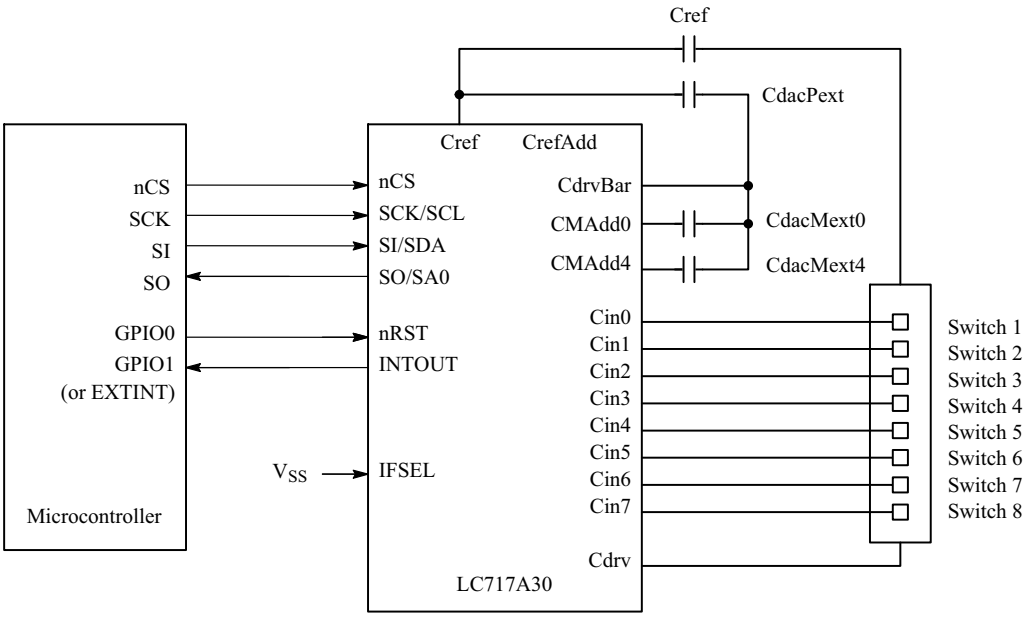
Figure 57. LC717A30UJ's Application Circuit Example of Small Capacitive Sensors (8 pF or less)



NOTE: For noise de-coupling place a high-valued capacitor (C2) and a low-valued capacitor (C1) in parallel between V_{DD} and V_{SS}. The small-valued capacitor(C1), at least 0.1 μF, should be mounted near the LSI.

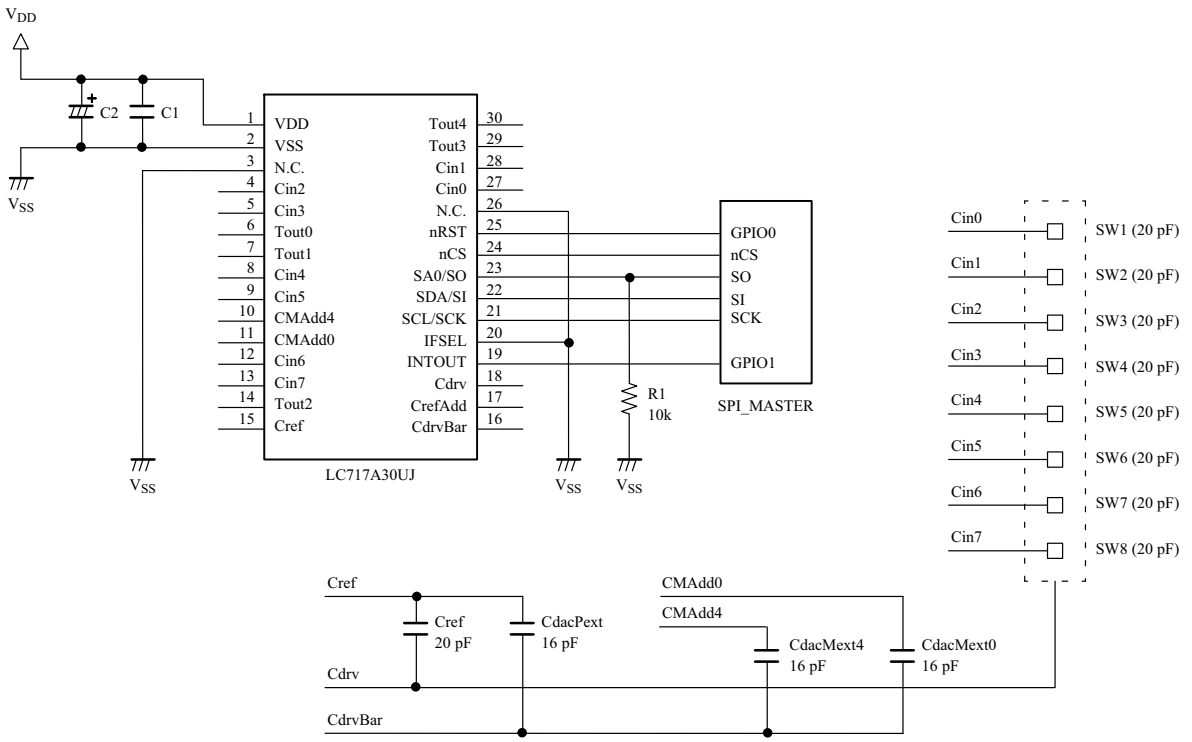
Figure 58. LC717A30UR's Application Circuit Example of Small Capacitive Sensors (8 pF or less)

(2) Configuration of Large Capacitive Sensors (More than 8 pF)



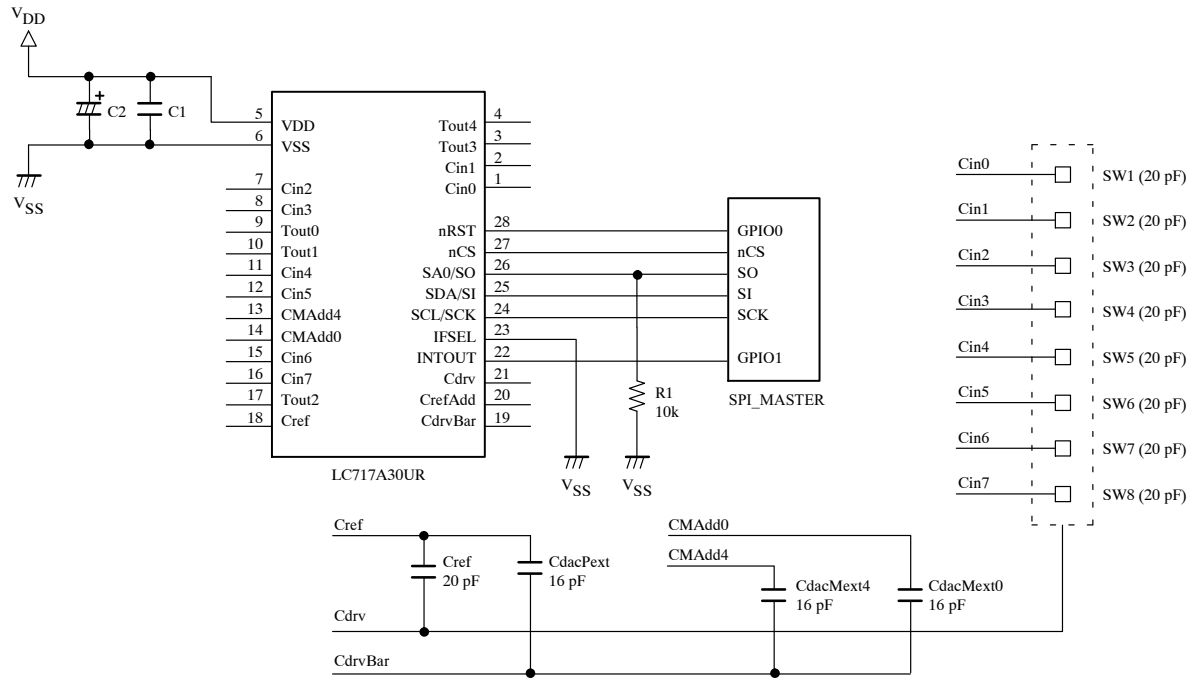
NOTE: Constitute a relation of CinX (X = 0 to 3) = CdacM + CdacMext0, Cref = CdacP + CdacPext, CinY (Y = 4 to 7) = CdacM + CdacMext4 and Cref = CdacP + CdacPext.

Figure 59. Connection Configuration Example of Large Capacitive Sensors (More than 8 pF)



NOTE: For noise de-coupling place a high-valued capacitor (C2) and a low-valued capacitor (C1) in parallel between V_{DD} and V_{SS}. The small-valued capacitor (C1), at least 0.1 μF, should be mounted near the LSI.

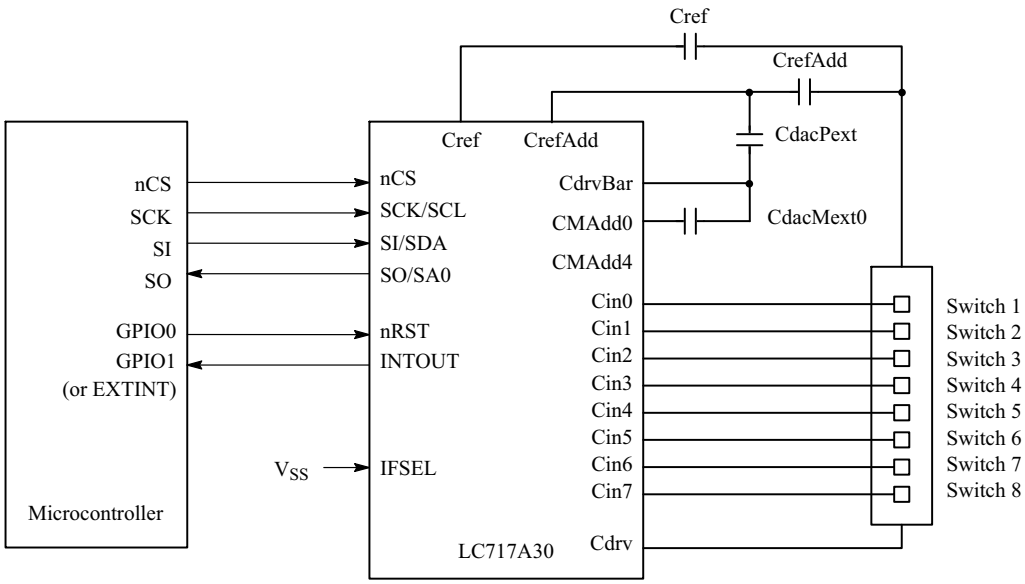
Figure 60. LC717A30UJ's Application Circuit Example of Large Capacitive Sensors (More than 8 pF)



NOTE: For noise de-coupling place a high-valued capacitor (C2) and a low-valued capacitor (C1) in parallel between V_{DD} and V_{SS}. The small-valued capacitor (C1), at least 0.1 μF, should be mounted near the LSI.

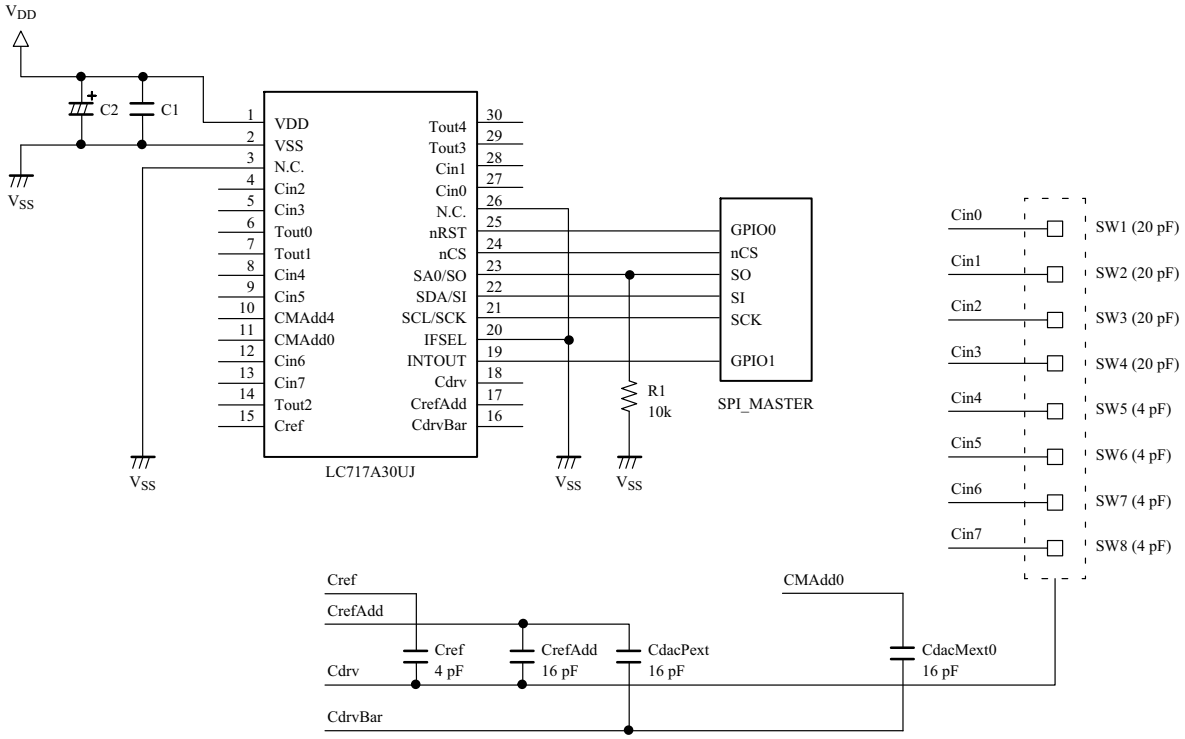
Figure 61. LC717A30UR's Application Circuit Example of Large Capacitive Sensors (More than 8 pF)

(3) Configuration that Small Capacitive Sensors and Large Capacitive Sensors are Mixed



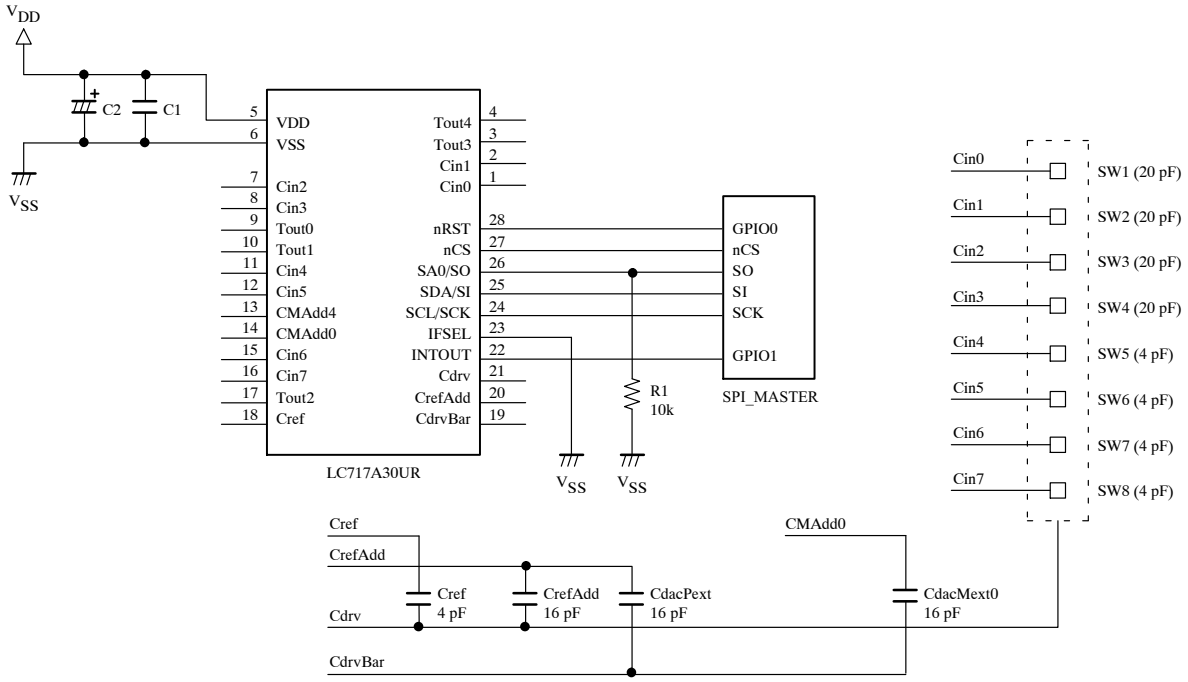
NOTE: Constitute a relation of CinX (X = 0 to 3) = CdacM + CdacMext0, Cref + CrefAdd = CdacP + CdacPext, CinY (Y = 4 to 7) = CdacM and Cref = CdacP.

Figure 62. Connection Configuration Example that Small Capacitive Sensors and Large Capacitive Sensors are Mixed



NOTE: For noise de-coupling place a high-valued capacitor (C2) and a low-valued capacitor (C1) in parallel between V_{DD} and V_{SS}. The small-valued capacitor (C1), at least 0.1 μF, should be mounted near the LSI.

Figure 63. LC717A30UJ's Application Circuit Example that Small Capacitive Sensors and Large Capacitive Sensors are Mixed



NOTE: For noise de-coupling place a high-valued capacitor (C2) and a low-valued capacitor (C1) in parallel between V_{DD} and V_{SS}. The small-valued capacitor (C1), at least 0.1 μF, should be mounted near the LSI.

Figure 64. LC717A30UR's Application Circuit Example that Small Capacitive Sensors and Large Capacitive Sensors are Mixed

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