1. Introduction

This application note describes a complete flyback switched mode power supply that uses a Fairchild Power Switch. The MOSFET and its control IC are built into one package. The MOSFET is in fact a SenseFET. Various protection features are also included. Fairchild Power Switch can enhance the reliability and productivity of the system when compared to other designs. The FS6M series has a more avalanche rugged SenseFET than the previous Fairchild Power Switch series. The FS6M series features include burst mode operation for low power consumption in DPMS mode. This application note describes the features and design considerations of the FS6M series for the LCD monitor power supply and adaptor, which improves upon the existing KA5X-series.

FS6Mxx652RT has one package type: TO-220F-5L as shown below. Fairchild Power Switch is classified according to the voltage and current rating of the internal SenseFET. The FS6M series parts with absolute voltage and absolute current ratings of 650V/7A and 650V/12A. When in power saving mode, the FS6M series pulls down the output voltages to a predetermined level and enters burst mode with a switching frequency of 70kHz.

![Figure 1-1. Package Line-Up](image)

<table>
<thead>
<tr>
<th>Product</th>
<th>Rating</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>FS6M07652RTC</td>
<td>7A/650V</td>
<td>TO-220F-5L</td>
</tr>
<tr>
<td>FS6M12653RTC</td>
<td>12A/650V</td>
<td>TO-220F-5L</td>
</tr>
</tbody>
</table>
2. Internal Block and Important Features

2.1 Internal Block and Features

- Pulse by pulse current limiting
- Fixed frequency (70kHz)
- Internal Burst Mode Controller for DPMS
- Internal high voltage SenseFET (QFET)
- World wide Input voltage
- Optimum Gate Driver
- Low Standby Power Consumption (Low start-up current & low operating current)
- Various Internal Protection Circuits
  - Over Voltage Protection (OVP) (Auto-restart)
  - Over Load Protection (OLP) (Auto-restart)
  - Over Current Latch (OCL) (Auto-restart)
  - Thermal Shutdown Protection (TSD) (Latch)
- Soft start

Figure 2-1. Internal Block Diagram
2.2 Starting Resistance Design And UVLO

Input voltage range: 80 ~ 265V (Ac)
At Minimum Input Voltage Va(dc), the starting resistance is

\[ \text{Va}(\text{dc}) = 113V \quad (V_p = 80\sqrt{2}) \]
\[ \text{R}_{\text{start}} = \frac{113 + 200\mu A}{565K} \]

and, at Maximum Input Voltage Va(dc), the power loss is

\[ \text{P(loss)} = \frac{\text{Vac}(\text{dc})^2}{\text{R}_{\text{start}}} = 0.246W \]

Select: \( \text{R}_{\text{start}} = 565K\Omega /0.5W \)

At the minimum voltage, the starting resistance is set to ensure that the current through it is larger than the maximum start up current for the Fairchild Power Switch (170µA). The starting resistor produces a starting current, which charges the VCC capacitor. The Fairchild Power Switch starts switching the internal SenseFET when the VCC voltage becomes greater than 15V (the start voltage). Once it starts to operate, the current drawn by the control IC suddenly increases to 10mA. The starting resistor cannot source this and consequently, the transformer auxiliary winding supplies most of the IC current after start up. The start time will be delayed if the VCC capacitor is too large, so a moderate size capacitor should be used. Generally, 22~47 µF capacitor values are considered good. This operation is described in Figure 2-2. VCC only needs to be maintained above 9V after starting, but should be set so that OVP (Min. VCC voltage above 30V) is not triggered. Approximately 24V is appropriate for the VCC voltage.

![Figure 2-2. Start-up Waveform](image)

2.3 Fairchild Power Switch Protection Circuit

The Fairchild Power Switch has several self-protection circuits, which can be used without adding external components, thus providing system reliability without increasing cost.

Under auto restart mode, protection circuits become deactivated when VCC falls below 9V (stop voltage), after which Fairchild Power Switch tries to restart. Under latch mode, protection circuits become deactivated only when VCC falls to 6.5V (reset voltage), then Fairchild Power Switch tries to restart. When VCC drops to 9V due to latch protection, the operating current of the IC drops from 10mA to 100µA. Therefore the VCC capacitor starts to charge towards 15V through the starting resistor. For VCC to fall to 6.5V (reset voltage), the input voltage must be removed.

2.3.1 Over Load Protection (OLP)

Overload as described here is different from a load short circuit. It is a condition where a load becomes greater than the preset level, though it is operating normally. Essentially, the overload protection circuit forces the Fairchild Power Switch to stop its operation if the load draws a higher current than the predetermined maximum value. A problem associated with this type of protection circuit is that it can trigger erroneously on load transients. As a security measure, the Fairchild Power Switch triggers the protection circuit after a specific time delay. This avoids false triggering on short load transients. The above operations are executed as follows. Since the Fairchild Power Switch uses current mode control, maximum switch current is limited internally. For a fixed input voltage, this limits the power. Therefore, if the power at the output exceeds this maximum, V_{O} shown in figure 2-4 becomes less than the set voltage, and the KA431(LM431) can draw only the allowed minimum current. As a result, the photo-transistor’s current becomes zero. If all the current of the 0.9mA current source flows through the internal resistor (2.5R+R= 3.3K), Vfb becomes approximately 3V. At this time the 2µA current source starts to charge Cfb. Because the photo transistor’s current is zero, Vfb continues to increase. The Fairchild Power Switch shuts down when Vfb reaches 7.5V. The shutdown delay time can be easily determined as the time required to increase the Cfb...
by 4.5V (from 3V to 7.5V) using 2µA. When Cfb is 47nF, delay time is approximately 100ms. Fairchild Power Switch will not shut down within this time. Increasing Cfb to get a longer delay time can become a problem, because Cfb is an important parameter in determining the SMPS dynamic response time.

One method to delay the shutdown time is to add a resistor between the F/B pin and GND and to subtract the amount of the delay current. When the 4.7MΩ resistor was used experimentally with Cfb of 47nF, shutdown time was almost doubled to 180~200ms. When Vfb voltage is 7.5V, the current flowing to the 4.7MΩ resistor is approximately 1.6µA.

To obtain the same results, a zener diode (approx. 3.9V) can be series connected to a capacitor (47nF) which can then be parallel connected to Cfb as shown in Figure 2.4.

![Figure 2-4. Fairchild Power Switch (FPS) Long Delayed Shutdown](image)

### 2.3.2 Over Voltage Protection

Fairchild Power Switch has self protection features that function even when abnormal states occur such as an open or short circuits in the feedback loop. When the feedback terminal shorts as viewed from the primary side, the feedback terminal voltage becomes zero and prevents switching from starting. If it opens, the protection circuit acts as an over voltage protection circuit. When there is an abnormal state or a possibility of opening due to improper soldering etc. in the secondary side feedback circuit, the primary side continues to switch using the maximum set current until the protection circuit starts to operate. In such instances, it is common for the secondary side voltage to become greater than the rated voltage, which can lead to a fuse blowing or, more seriously, a fire if a protection circuit is not in place. Even if this was not the case, ICs immediately connected to the secondary output without a regulator can be destroyed. Therefore, the Fairchild Power Switch employs the over voltage protection circuit to protect against feedback anomalies. The Fairchild Power Switch VCC is proportional to the output voltage. When the Fairchild Power Switch VCC exceeds 33V, the over voltage protection feature is triggered. Therefore, VCC must be maintained at less than 30V during normal operation.

### 2.3.3 Over Current Protection (OCP)

The existing concept of Ipeak control does not go beyond limiting the amount of current during normal operation. The OCP block prevents damage to Fairchild Power Switch from abnormal states, such as a diode or a load short. A diode or a load short causes a large current to flow through the SenseFet for a short time. This can be tens of amperes. The leading edge blanking circuit sets the minimum turn on time at 600nS. Tens of amperes for 600nS could destroy the Fairchild Power Switch and so the OCL block senses this instantaneous current and latches like the existing protection circuit.
3. Display Power Management Signalling (DPMS) Design Method

With high interest in power management recently, much effort has been concentrated in implementing the DPMS mode. The FS6S series uses burst mode for DPMS in order to achieve cost effectiveness and minimize the power consumption.

3.1 Burst Mode Operation

The FS6S-series has a particularly useful function for the DPMS mode: burst mode operation. Normally, customers use an auxiliary power system for DPMS in large monitors. This method can lower power consumption but increases costs. The FS6S-series can drop the output voltage with only minimal external components by using burst mode. This reduces power loss in DPMS mode.

In the DPMS mode, Vfb is pulled low by the external micro-controller.

3.2 Implementation of the Burst Mode

The required circuit for implementing the burst mode is shown in Figure 4-1. Q1, D1, Rx, R5 and R6 are added to the secondary feedback network. During normal operation, Q1 is on, which isolates Rx from the feedback network.

Vo2 is sensed and the amplified error is transferred to the primary side through the photo coupler. By turning off Q1, Rx is connected to the feedback network.

The error amplifier increases the current through the photo coupler, and thus Vfb of the FS6S-series drops to zero. Therefore no additional opto coupler is required to switch into burst mode. Rx can be calculated by the following equation when KA431(LM431) is used as an error amp.

\[ Rx < \frac{R7 \times R8 (Vo1 - 2.5 - V_{D1})}{2.5 (R7 + R8) - R8 \cdot Vo2} \]

where Vo1 and Vo2 are the reduced voltages in burst mode.
3.3 Experiment of the Burst mode operation

3.3.1 Vcc/Vds/ Vregin/Vregout waveform at the Burst Mode operation

Experimental results are shown in, Figure 4-2 and Figure 4-3. With minimum load and normal operation:
Vac = 240V, Pin = 4.82W, VCC = 18V, Vo = 12.24V.
When Fairchild Power Switch operates Burst Mode:
Pin = 2.72W, VCC = 11~12V, Vo = 6.7V.
4. Application for the LCD Monitor

4.1 Flyback converter demo circuit for LCD Monitor

Figure 4-1. Fairchild Power Switch (FPS) Flyback Converter DEMO BOARD for the LCD Monitor
### 4.2 Part List for Fairchild Power Switch (FPS) Flyback Converter DEMO BOARD for the LCD Monitor

<table>
<thead>
<tr>
<th>Part</th>
<th>Value</th>
<th>Note</th>
<th>Part</th>
<th>Value</th>
<th>Note</th>
</tr>
</thead>
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<tr>
<td>Fuse</td>
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<td></td>
<td>C204</td>
<td>1000μF 10V Electrolytic Capacitor</td>
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</tr>
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<td>C205</td>
<td>47nF 50V Electrolytic Capacitor</td>
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<td></td>
<td>C206</td>
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<td>C301</td>
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<td>UF4007</td>
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<td></td>
<td></td>
<td></td>
<td>L202</td>
<td>6μH</td>
<td></td>
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<tr>
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<td></td>
<td>LF101</td>
<td>13mH</td>
<td></td>
</tr>
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<td>IC</td>
<td></td>
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<td>FS6S07652RT</td>
<td>FPSFPS(2A 650V): Fairchild</td>
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<td>KA431 (LM431)</td>
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<td></td>
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<td>IC301</td>
<td>HC11A817A</td>
<td>Photo Coupler/QT</td>
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<tr>
<td>Bridge Diode</td>
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<td>BD1</td>
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<tr>
<td>Capacitor</td>
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<td>IC</td>
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<td></td>
<td>IC101</td>
<td>FS6S07652RT</td>
<td>FPSFPS(2A 650V): Fairchild</td>
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<td>KA7805</td>
<td>Voltage regulator Fairchild</td>
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<td></td>
<td>IC301</td>
<td>HC11A817A</td>
<td>Photo Coupler/QT</td>
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</table>
4.3 Transformer Specification

1. SCHEMATIC DIAGRAM. (TOP VIEW)

2. WINDING SPECIFICATION

<table>
<thead>
<tr>
<th>NO.</th>
<th>PIN(S → F)</th>
<th>WIRE</th>
<th>TURNS</th>
<th>WINDING METHOD</th>
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<tbody>
<tr>
<td>Np/2</td>
<td>2 → 1</td>
<td>0.3φ×1</td>
<td>40</td>
<td>SOLENOID WINDING</td>
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<tr>
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<td></td>
<td></td>
<td></td>
<td>INSULATION : POLYESTER TAPE t=0.050mm, 2Layer</td>
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<tr>
<td>Nv2</td>
<td>8 → 7</td>
<td>0.3φ×4</td>
<td>4</td>
<td>CENTER WINDING</td>
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<td></td>
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<td></td>
<td>INSULATION : POLYESTER TAPE t=0.050mm, 2Layers</td>
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<td>Nvcc</td>
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<td>0.3φ×2</td>
<td>13</td>
<td>CENTER WINDING</td>
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<td></td>
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</tr>
<tr>
<td>Np/2</td>
<td>3 → 2</td>
<td>0.3φ×1</td>
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<td>SOLENOID WINDING</td>
</tr>
<tr>
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<td></td>
<td></td>
<td></td>
<td>OUTER INSULATION : POLYESTER TAPE t=0.050mm, 2Layers</td>
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3. ELECTRICAL CHARACTERISTIC

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<tr>
<th>CLOSURE</th>
<th>PIN</th>
<th>SPEC.</th>
<th>REMARKS</th>
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<tbody>
<tr>
<td>INDUCTANCE</td>
<td>1-3</td>
<td>650uH ± 10%</td>
<td>100KHz, 1V</td>
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<tr>
<td>LEAKAGE L</td>
<td>1-3</td>
<td>10uH MAX.</td>
<td>2nd ALL SHORT</td>
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4. CORE & BOBBIN

CORE : EFD3030
BOBBIN : EFD3030

Figure 4-2. FS6M07652RT Transformer Spec for LCD Monitor
5. Example Transformer Design for a Monitor SMPS

When designing the transformer for a LCD monitor SMPS several parameters should be taken into account. Input and output voltages will determine the windings. Consideration should be given to the switching frequency range, continuous and discontinuous current modes and core size.

A typical design sequence is as follows:

5-1. Determine System Specifications:

Output Power, \( P_O = 30\text{W} \) (at 12 and 3.3V) Vac input range = 85 to 265Vac (universal input), 60Hz

Efficiency \( \eta \geq 70\% \)

5-2. Determine Minimum Dc Input Voltage (\( V_{\text{min}} \)), Primary Peak Current (\( I_{\text{peak}} \)) And Primary Rms Current (\( I_{\text{rms}} \)).

When the SMPS operates at the same output power for all ac inputs, the maximum peak drain current occurs at the minimum input voltage (\( V_{\text{min}} \)). Also, \( V_{\text{min}} \) will exhibit the largest ripple voltage (\( \Delta V \)) at that time. The dc link capacitor \( C_{\text{in}} \) is charged and discharged at 120Hz (Figure 5-1).

![Figure 5-1](image)

Figure 5-1. If power output stays constant as the ac input varies, peak current drain will occur at \( V_{\text{min}} \). Also, the largest ripple on \( V_{\text{min}} \) occurs at this point; dc link capacitor \( C_{\text{in}} \) is charged/discharged at 120Hz.

a. Calculate energy discharge time, \( T_d \):

\[
T_d = \frac{1}{f_s} \times \frac{1}{4} \times \left\{ \frac{\arcsin \left( \frac{V_{\text{min}}}{V_{\text{min, peak}}} \right)}{\pi/2} \right\}
\]

b. Calculate dc link capacitor, \( C_{\text{in}} \):

\[
Win = Pin \times T_d \quad \text{(Win = input energy during discharge)}
\]

\[
Win = \frac{1}{2} C_{\text{in}} \cdot (V_{\text{min, peak}} - V_{\text{min}}^2)
\]

c. For this charger:

\[
T_d = 6.78\text{ms}(V_{\text{min, peak}} = 85\sqrt{2}, V_{\text{min}} = 85\sqrt{2} - 20)
\]

\[
Win = \frac{P_{\text{out}}}{\eta} \quad T_d = 0.7 \times 6.78\text{ms} = 0.29\text{J}
\]

d. Assume 20Vac of ripple, from which:

\[
C_{\text{in}} = \frac{2Win}{V_{\text{min, peak}} - V_{\text{min}}^2} = \frac{2 \times 0.29}{(85\sqrt{2} \times 85)^2 - (85\sqrt{2} \times 20 - 20)^2} = 132\mu\text{F}
\]

However, 132\(\mu\text{F}\) is not a standard value of capacitor. Hence, to calculate the true \( V_{\text{min}} \), select the nearest standard value for \( C_{\text{in}} \) (82\(\mu\text{F}\)) and substitute it above, solving for \( V_{\text{min}} \) = 86V.

e. Primary current reaches its \( I_{\text{peak}} \) value at \( V_{\text{min}} \) and maximum duty (\( D_{\text{max}} \)). Also in most current mode SMPSs, \( D_{\text{max}} \) should be kept below 50% to eliminate any possibility of sub harmonic instabilities.

\[
I_{\text{peak}} = \frac{2 \times P_{\text{out}}}{\eta \times V_{\text{min}} \times D_{\text{max}}} = \frac{2 \times 30}{0.7 \times 86 \times 0.45} \approx 2.2\text{A}
\]

Primary \( I_{\text{rms}} \) can be derived from \( I_{\text{peak}} \):

\[
I_{\text{rms}} = I_{\text{peak}} \times \frac{4}{3} = 2.2 \times \frac{0.45}{3} = 0.85\text{A}
\]

5-3. Determine Primary Inductance, \( L_p \):

This is the primary inductance needed to transfer the required power from primary to secondary.

\[
L_p = \frac{D_{\text{max}} \times V_{\text{min}}}{\Delta I_{\text{fs}}} = \frac{0.45 \times 86}{0.7 \times 70 \times 10^{-5}} = 650\mu\text{H}
\]

It is recommended to select the minimum synchronous frequency as the switching frequency, \( f_s \), of the monitor application.

5-4. Determine Core Size:

The core used must be able to store the required peak energy in a small gap without saturation and with acceptable core losses. The following equation is commonly used to ensure proper core size (area product) in a saturation limited case.

\[
AP = A_w \cdot A_p = \left[ \frac{L_p \cdot I_{\text{rms}} \cdot 10^{-6}}{420 \cdot K \cdot B_m} \right]^{1.31} \text{cm}^2
\]

where, \( A_w \) = magnetic window area, cm\(^2\)

\( A_p \) = magnetic cross section area, cm\(^2\)

\( K \) = core utilization factor, 0.2

\( B_m \) = maximum flux density, Teasel; therefore,

\[
AP = \left[ \frac{650 \times 10^{-6} \times 1.52 \times 0.85 \times 10^{-6}}{420 \times 0.2 \times 0.1} \right]^{1.31} = 2.47\text{cm}^2
\]
From the catalog data, select the smallest ferrite core available with an area product, AP, that exceeds the calculated value. The specifications of the selected core, EFD3030 are AP = 2.47 cm², $A_w = 2.23 \text{cm}^2$, $A_e = 1.07 \text{cm}^2$

5-5. Determine Primary Turns, $N_p$:

$$T_{\text{on(max)}} = \frac{1}{f_s} \times D_{\text{max}}$$

$$= \frac{1}{70 \times 10^3} \times 0.45$$

$$= 6.43 \mu\text{s}$$

From Faraday’s law, the minimum number of primary turns can be expressed as

$$N_{P\text{(min)}} = \frac{V_{\text{min}} \times T_{\text{on(max)}}}{\Delta B_m \times A_e} = \frac{86 \times 6.43 \times 10^{-6}}{0.1 \times 69 \times 10^{-6}} = 80\text{[turns]}$$

where, $T_{\text{on(max)}}$ is maximum turn on time, and $\Delta B_m$ is maximum peak to peak flux density swing

5-6. Determine Secondary Turns, $N_s$:

Using the Volt-seconds equation, the turns ratio $n = N_p/N_s$ can be calculated at maximum duty ratio, as

$$n = \frac{V_{\text{min}} \times D_{\text{utymax}}}{(V_o + V_d) \times (1-D_{\text{utymax}})} = 6$$

where, $V_o$ = output voltage, and $V_d$ = diode forward voltage drop; hence,

$$N_s = \frac{N_p}{n} = \frac{80}{6} = 13\text{[turns]}$$

5-7. Determine Bias Turns, $N_b$, And Auxiliary Turns, $N_a$:

Secondary side calculation in volts per turn units is

$$\text{Secondary Volt/turn} = \frac{V_s}{N_s} = \frac{12}{13} = 1\text{[V/turn]}$$

The bias side must have same volts-per-turn value as the secondary side and so can be calculated as

$$N_b = \frac{V_b}{V_s \times N_s} = \frac{24}{1} = 24\text{[turns]}$$

Auxiliary turns are calculated using the same volts per unit.
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