AN-9738
Design Guideline on 150W Power Supply for LED Street Lighting Design Using FL7930B and FAN7621S

Introduction

This application note describes a 150W rating design guideline for LED street lighting. The application design consists of CRM PFC and LLC SRC with high power factor and high power conversion efficiency using FL7930B and FAN7621S. To verify the validity of the application board and scheme, a demonstration board 150W (103V/1.46A) AC-DC converter was implemented and its results are presented in this application note. In CRM active PFC, the most popular topology is a boost converter. This is because boost converters can have continuous input current that can be manipulated with peak current mode control techniques to force peak current to track changes in line voltage. The FAN7930B is an active Power Factor Correction (PFC) controller for boost PFC applications that operate in critical conduction mode (CRM). Since it was first introduced in early 1990s, LLC-SRC (series resonant converter) has become a most popular topology because of its outstanding performance in areas such as the output regulation of switching frequency, ZVS capability for entire load range, low turn-off current, small resonant components using the integrated transformer, zero current switching (ZCS), and no reverse recovery loss on secondary rectifier. Figure 1 shows the typical application circuit, with the CRM PFC converter in the front end and the LLC SRC DC-DC converter in the back end. FL7930B and FAN7621S achieve high efficiency with medium power for 150W rating applications where CRM and LLC SRC operation with a two-stage shows best performance. CRM boost PFC converters can achieve better efficiency with light and medium power rating than Continuous Conduction Mode (CCM) boost PFC converters. These benefits result from the elimination of the reverse-recovery losses of the boost diode and Zero-Current Switching (ZCS). The LLC SRC DC-DC converter achieves higher efficiency than the conventional hard switching converter. The FL7930B provides a controlled on-time to regulate the output DC voltage and achieves natural power factor correction. The FAN7621S includes a high-side gate driver circuit, accurate current-controlled oscillator, frequency -limit circuit, soft-start, and built-in protections. The high-side gate drive circuit has a common-mode noise cancellation capability, which guarantees stable operation with excellent noise immunity. Using Zero Voltage Switching (ZVS) dramatically reduces switching losses and significantly improves efficiency. ZVS also reduces switching noise noticeably, which allows a small-sized Electromagnetic Interference (EMI) filter.

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Figure 1. Typical Application Circuit
1. Basic Operation of BCM PFC Pre-Regulator

The most widely used operation modes for the boost converter are Continuous Conduction Mode (CCM) and Boundary Conduction Mode (BCM). These two descriptive names refer to the current flowing through the energy storage inductor of the boost converter, as depicted in Figure 2. As the names indicate, the inductor current in CCM is continuous; while in BCM, the new switching period is initiated when the inductor current returns to zero, which is at the boundary of continuous conduction and discontinuous conduction operations. Even though the BCM operation has higher RMS current in the inductor and switching devices, it allows better switching condition for the MOSFET and the diode. As shown in Figure 2, the diode reverse recovery is eliminated and a fast-recovery diode is not needed. The MOSFET is also turned on with zero current, which reduces the switching loss.

A side effect of BCM is that the boost converter runs with variable switching frequency that depends primarily on the selected output voltage, the instantaneous value of the input voltage, the boost inductor value, and the output power delivered to the load. The operating frequency changes as the input current follows the sinusoidal input voltage waveform, as shown in Figure 3. The lowest frequency occurs at the peak of sinusoidal line voltage.

![Figure 3. Operation Waveforms of BCM PFC](image)

The voltage-second balance equation for the inductor is:

$$V_{IN}(t) \cdot t_{ON} = (V_{OUT} - V_{IN}(t)) \cdot t_{OFF} \quad (1)$$

where $V_{IN0}$ is the rectified line voltage and $V_{OUT}$ is the output voltage.

The switching frequency of BCM boost PFC converter is:

$$f_{SW} = \frac{1}{t_{ON} + t_{OFF}} = \frac{1}{t_{ON}} \cdot \frac{V_{OUT} - V_{IN}(t)}{V_{OUT}} = \frac{1}{t_{ON}} \cdot \frac{V_{OUT} - V_{IN,PK} \cdot \sin(2\pi \cdot f_{LINE} \cdot t)}{V_{OUT}} \quad (2)$$

where $V_{IN,PK}$ is the amplitude of the line voltage and $f_{LINE}$ is the line frequency.

Figure 4 shows how the MOSFET on-time and switching frequency change as output power decreases. When the load decreases, as shown in the right side of Figure 4, the peak inductor current diminishes with reduced MOSFET on-time and, therefore, the switching frequency increases. Since this can cause severe switching losses at light-load condition and too-high switching frequency operation may occur at startup, the maximum switching frequency of FL7930B is limited to 300kHz.
Since the design of the filter and inductor for a BCM PFC converter with variable switching frequency should be at minimum frequency condition, it is worthwhile to examine how the minimum frequency of BCM PFC converter changes with operating conditions.

2. Consideration of LLC Resonant Converter

The attempt to obtain ever-increasing power density in switched-mode power supplies has been limited by the size of passive components. Operation at higher frequencies considerably reduces the size of passive components, such as transformers and filters; however, switching losses have been an obstacle to high-frequency operation. To reduce switching losses and allow high-frequency operation, resonant switching techniques have been developed. These techniques process power in a sinusoidal manner and the switching devices are softly commutated. Therefore, the switching losses and noise can be dramatically reduced.

Among various kinds of resonant converters, the simplest and most popular is the LC series resonant converter, where the rectifier-load network is placed in series with the LC resonant network, as depicted in Figure 5. In this configuration, the resonant network and the load act as a voltage divider. By changing the frequency of driving voltage \( V_{\text{drive}} \), the impedance of the resonant network changes. The input voltage is split between this impedance and the reflected load. Since it is a voltage divider, the DC gain of a LC series resonant converter is always \(<1\). At light-load condition, the impedance of the load is large compared to the impedance of the resonant network; all the input voltage is imposed on the load. This makes it difficult to regulate the output at light load. Theoretically, frequency should be infinite to regulate the output at no load.

To overcome the limitation of series resonant converters, the LLC resonant converter has been proposed. The LLC resonant converter is a modified LC series resonant converter implemented by placing a shunt inductor across the transformer primary winding, as depicted in Figure 6. When this topology was first presented, it did not receive much attention due to the counterintuitive concept that increasing the circulating current in the primary side with a shunt inductor can be beneficial to circuit operation. However, it can be very effective in improving efficiency for high-input voltage applications where the switching loss is more dominant than the conduction loss.

In most practical designs, this shunt inductor is realized using the magnetizing inductance of the transformer. The circuit diagram of LLC resonant converter looks much the same as the LC series resonant converter: the only difference is the value of the magnetizing inductor. While the series resonant converter has a magnetizing inductance larger than the LC series resonant inductor \( L_r \), the magnetizing inductance in an LLC resonant converter is just 3–8 times \( L_r \), which is usually implemented by introducing an air gap in the transformer.

An LLC resonant converter has many advantages over a series resonant converter. It can regulate the output over wide line and load variations with a relatively small variation of switching frequency. It can achieve zero voltage switching (ZVS) over the entire operating range. All essential parasitic elements; including the junction capacitances of all semiconductor devices, the leakage inductance, and magnetizing inductance of the transformer; are utilized to achieve soft switching.
This application note presents design considerations for an LLC resonant half-bridge converter employing Fairchild’s FAN7621S. It includes explanation of the LLC resonant converter operation principles, designing the transformer and resonant network, and selecting the components. The step-by-step design procedure, explained with a design example, helps design the LLC resonant converter. Figure 7 shows a simplified schematic of a half-bridge LLC resonant converter, where $L_m$ is the magnetizing inductance that acts as a shunt inductor, $L_r$ is the series resonant inductor, and $C_r$ is the resonant capacitor. Figure 8 illustrates the typical waveforms of the LLC resonant converter. It is assumed that the operation frequency is the same as the resonance frequency, determined by the resonance between $L_r$ and $C_r$. Since the magnetizing inductor is relatively small, a considerable amount of magnetizing current ($I_m$) exists, which freewheels in the primary side without being involved in the power transfer. The primary-side current ($I_p$) is the sum of the magnetizing current and the secondary-side current referred to the primary.

In general, the LLC resonant topology consists of the three stages shown in Figure 7: square-wave generator, resonant network, and rectifier network.

- The square-wave generator produces a square-wave voltage, $V_{ds}$, by driving switches $Q_1$ and $Q_2$ alternately with 50% duty cycle for each switch. A small dead time is usually introduced between the consecutive transitions. The square-wave generator stage can be built as a full-bridge or half-bridge type.

- The resonant network consists of a capacitor, leakage inductances, and the magnetizing inductance of the transformer. The resonant network filters the higher harmonic currents. Essentially, only sinusoidal current is allowed to flow through the resonant network even though a square-wave voltage is applied. The current ($I_p$) lags the voltage applied to the resonant network (that is, the fundamental component of the square-wave voltage ($V_d$) applied to the half-bridge totem pole), which allows the MOSFETs to be turned on with zero voltage. As shown in Figure 8, the MOSFET turns on while the voltage across the MOSFET is zero by flowing current through the anti-parallel diode.

- The rectifier network produces DC voltage by rectifying the AC current with rectifier diodes and a capacitor. The rectifier network can be implemented as a full-wave bridge or a center-tapped configuration with capacitive output filter.

The filtering action of the resonant network allows the use of the fundamental approximation to obtain the voltage gain of the resonant converter, which assumes that only the fundamental component of the square-wave voltage input to the resonant network contributes to the power transfer to the output. Because the rectifier circuit in the secondary side acts as an impedance transformer, the equivalent load resistance is different from actual load resistance. Figure 9 shows how this equivalent load resistance is derived. The primary-side circuit is replaced by a sinusoidal current source, $I_{ac}$, and a square wave of voltage, $V_{ds}$, appears at the input to the rectifier. Since the average of $I_{ac}$ is the output current, $I_o$, $I_{ac}$ is obtained as:

$$I_{ac} = \frac{\pi}{2} I_o \sin(\omega t)$$

(3)
and $V_{R_i}$ is given as:

$$V_{R_i} = \begin{cases} +V_o & \text{if } \sin(\omega t) > 0 \\ -V_o & \text{if } \sin(\omega t) < 0 \end{cases}$$

where $V_o$ is the output voltage.

The fundamental component of $V_{R_i}$ is given as:

$$V_{R_i}^F = \frac{4V_o}{\pi} \sin(\omega t)$$

(5)

Since harmonic components of $V_{R_i}$ are not involved in the power transfer, AC equivalent load resistance can be calculated by dividing $V_{R_i}^F$ by $I_{ac}$ as:

$$R_{ac} = \frac{V_{R_i}^F}{I_{ac}} = \frac{8V_o}{\pi I_o} = \frac{8}{\pi^2} R_o$$

(6)

Considering the transformer turns ratio (n=Np/Ns), the equivalent load resistance shown in the primary side is obtained as:

$$R_{ac} = \frac{8n^2}{\pi^2} R_o$$

(7)

By using the equivalent load resistance, the AC equivalent circuit is obtained, as illustrated in Figure 10, where $V_d^F$ and $V_R^F$ are the fundamental components of the driving voltage, $V_d$ and reflected output voltage, $V_R(nV_R)$, respectively.

With the equivalent load resistance obtained in Equation 7, the characteristics of the LLC resonant converter can be derived. Using the AC equivalent circuit of Figure 10, the voltage gain, $M$, is obtained as:

$$M = \frac{V_d^F}{V_o} = \frac{n \cdot V_R^F}{V_o} = \frac{4n \cdot V_o}{\pi} \frac{\sin(\omega t)}{2n \cdot V_m} = \frac{2n \cdot V_o}{V_m}$$

(8)

where:

$$L_r = L_n + L_r, \quad R_{ac} = \frac{8n^2}{\pi^2} R_o, \quad m = \frac{L_p}{L_r}, \quad Q = \frac{L_p}{\sqrt{L_nC_r}}, \quad \omega_o = \frac{1}{\sqrt{L_nC_r}}, \quad \omega_p = \frac{1}{\sqrt{L_pC_r}}$$

As can be seen in Equation (8), there are two resonant frequencies. One is determined by $L_r$ and $C_r$, while the other is determined by $L_p$ and $C_r$.

Equation (8) shows the gain is unity at resonant frequency ($\omega_o$), regardless of the load variation, which is given as:

$$M = \frac{2n \cdot V_o}{V_{in}} = \frac{(m-1) \cdot \omega_o^2}{\omega_o^2 - \omega_p^2} = 1 \quad \text{at } \omega = \omega_o$$

(9)

The gain of Equation (8) is plotted in Figure 11 for different Q values with $m=3$, $f_o=100$kHz, and $f_p=57$kHz. As observed in Figure 11, the LLC resonant converter shows gain characteristics that are almost independent of the load when the switching frequency is around the resonant frequency, $f_o$. This is a distinct advantage of LLC-type resonant converter over the conventional series resonant converter. Therefore, it is natural to operate the converter around the resonant frequency to minimize the switching frequency variation.
The operating range of the LLC resonant converter is limited by the peak gain (attainable maximum gain), which is indicated with 'Q' in Figure 11. Note that the peak voltage gain does not occur at $f_p$ or $f_o$. The peak gain frequency, where the peak gain is obtained, exists between $f_p$ and $f_o$, as shown in Figure 11. As Q decreases (as load decreases), the peak gain frequency moves to $f_p$ and higher peak gain is obtained. Meanwhile, as Q increases (as load increases), the peak gain frequency moves to $f_o$ and the peak gain drops; the full-load condition should be worst case for the resonant network design.

![Figure 11. Typical Gain Curves of LLC Resonant Converter (m=3)](image)

### 3. Design Considerations

This design procedure uses the schematic in Figure 1 as a reference. A 150W street lighting application with universal input range is selected as a design example. The design specifications are:

- Line Voltage Range: $85V_{AC}$–$277V_{AC}$ (50Hz)
- Output of Converter: $103V/1.46A$ (150W)
- PFC Output Voltage: 430V
- Overall Efficiency: 90% (PFC: 95%, LLC: 95%)

#### 3.1 PFC Section

**[STEP-1] Define System Specification**

- Line Frequency Range ($V_{LINE,MIN}$ and $V_{LINE,MAX}$)
- Line Frequency ($f_{LINE}$)
- Output-Voltage ($V_{OUT}$)
- Output Load Current ($I_{OUT}$)
- Output Power ($P_{OUT} = V_{OUT} \times I_{OUT}$)
- Estimated Efficiency ($\eta$)

To calculate the maximum input power, it is necessary to estimate the power conversion efficiency. At universal input range, efficiency is recommended at 0.9; 0.93–0.95 is recommended when input voltage is high. When input voltage is set at the minimum, input current becomes the maximum to deliver the same power compared at high line. Maximum boost inductor current can be detected at the minimum line voltage and at its peak. Inductor current can be divided into two categories; rising current when the MOSFET is on and output diode current when the MOSFET is off, as shown in Figure 12.

![Figure 12. Inductor and Input Current](image)

Because switching frequency is much higher than line frequency, input current can be assumed to be constant during a switching period, as shown in Figure 13.

![Figure 13. Inductor and Input Current](image)

With the estimated efficiency, Figure 12 and Figure 13, inductor current peak ($I_{LPK}$), maximum input current ($I_{IN,MAX}$), and input Root Mean Square (RMS) current ($I_{IN,RMS}$) are given as:

\[
I_{LPK} = \frac{4 \cdot P_{OUT}}{\eta \cdot \sqrt{2} \cdot V_{LINE,MIN}} \quad [A] \\
I_{IN,MAX} = \frac{I_{LPK}}{2} \quad [A] \\
I_{IN,RMS} = \frac{I_{IN,MAX}}{\sqrt{2}} \quad [A]
\]

(Design Example) Input voltage range is universal input, output load is 465mA, and estimated efficiency is selected as 0.9.

\[
V_{LINE,MIN} = 85V_{AC}, \quad V_{LINE,MAX} = 277V_{AC} \\
V_{LINE} = 50Hz \\
V_{OUT} = 430V, \quad I_{OUT} = 465mA \\
\eta = 0.9 \\
I_{LPK} = \frac{4 \cdot 430V \cdot 0.465A}{0.9 \cdot \sqrt{2} \cdot 85} = 7.392A \\
I_{IN,MAX} = \frac{I_{LPK}}{2} = \frac{7.392A}{2} = 3.696A \\
I_{IN,RMS} = \frac{I_{IN,MAX}}{\sqrt{2}} = \frac{3.696A}{\sqrt{2}} = 2.613A
\]
[STEP-2] Boost Inductor Design

The boost inductor value is determined by the output power and the minimum switching frequency. The minimum switching frequency must be higher than the maximum audible frequency band of 20kHz. Minimum frequency near 20kHz can decrease switching loss with the cost of increased inductor size and line filter size. Too-high minimum frequency may increase the switching loss and make the system respond to noise. Selecting in the range of about 30–60kHz is a common choice; 40–50kHz is recommended with FL7930B.

The minimum switching frequency may appear at minimum recommended with FL7930B. Increased inductor size and line filter size. Toomhigh audible frequency band of 20kHz. Minimum frequency near

When selecting wire diameter and strands; current density, window area (\(A_w\), refer to Figure 14) of the selected core, and fill factor need to be considered. The winding sequence of the boost inductor is relatively simple compared to a DC-DC converter, so fill factor can be assumed about 0.2–0.3. Layers cause the skin effect and proximity effect in the coil, so real current density may be higher than expected.

\[ \Delta L, DENSITY = L, DENSITY, L \] decreases as the temperature increases, the highm

\[ (13) \]

\( L = \frac{\eta \left(\sqrt{2} \cdot V_{\text{LINE}}\right)^2}{4 \cdot f_{\text{SW,MIN}} \cdot P_{\text{OUT}} \cdot \left(f + \frac{\sqrt{2} \cdot V_{\text{LINE}}}{V_{\text{OUT}} \cdot \sqrt{2} \cdot V_{\text{LINE}}}\right)} \] (H)

where \( L \) is boost inductance and \( f_{\text{SW,MIN}} \) is the minimum switching frequency.

The maximum on-time needed to carry peak inductor current is calculated as:

\[ t_{\text{ON,MAX}} = L \cdot \frac{I_{\text{L,PK}}}{\sqrt{2} \cdot V_{\text{LINE,MIN}}} \text{ [s]} \] (14)

Once inductance and the maximum inductor current are calculated, the turn number of the boost inductor should be determined considering the core saturation. The minimum number of turns is given as:

\[ N_{\text{BOOST}} \geq \frac{I_{\text{L,PK}} - I_{\text{L,DENSITY}}}{A_w \cdot \Delta B} \text{ [Turns]} \] (15)

where \( A_w \) is the cross-sectional area of the core and \( \Delta B \) is the maximum flux swing of the core in Tesla. \( \Delta B \) should be set below the saturation flux density.

Figure 14 shows the typical B-H characteristics of a ferrite core from TDK (PC45). Since the saturation flux density (\( \Delta B \)) decreases as the temperature increases, the high-temperature characteristics should be considered.

RMS inductor current \( (I_{\text{L,RMS}}) \) and current density of the coil \( (I_{\text{L,DENSITY}}) \) can be given as:

\[ I_{\text{L,RMS}} = \frac{I_{\text{L,PK}}}{\sqrt{2}} \text{ [A]} \] (16)

\[ I_{\text{L,DENSITY}} = \frac{I_{\text{L,RMS}} \cdot \pi \left(\frac{d_{\text{WIRE}}}{2}\right)^2}{N_{\text{WIRE}}} \text{ [A/mm}^2\text{]} \] (17)

where \( d_{\text{WIRE}} \) is the diameter of winding wire and \( N_{\text{WIRE}} \) is the number of strands of winding wire.

When 0.10mm diameter and 50-strand wire is used, RMS current of inductor and current density are:
**[STEP-3] Inductor Auxiliary Winding Design**

Figure 16 shows the application circuit of the nearby ZCD pin from auxiliary winding.

![Figure 16. Application Circuit of ZCD Pin](image)

The first role of ZCD winding is detecting the zero-current point of the boost inductor. Once the boost inductor current becomes zero, the effective capacitance ($C_{eff}$) at the MOSFET drain pin and the boost inductor resonate together. To minimize the constant turn-off time deterioration and turn-on loss, the gate is turned on again when the drain source voltage of the MOSFET ($V_{DS}$) reaches the valley point shown in Figure 17. When input voltage is lower than half of the boosted output voltage, Zero Voltage Switching (ZVS) is possible if MOSFET turn-off is triggered at valley point.

$$I_{L,RMS} = \frac{I_{L,PK}}{\sqrt{2}} = \frac{7.59V}{\sqrt{2}} = 5.07[A]$$

$$I_{L,DENSITY} = \frac{I_{L,RMS}}{\pi \left( d_{wire}/2 \right) \cdot N_{wire} \cdot \pi \left( d_{wire}/2 \right)^2 \cdot 50} = 7.68[A/mm^2]$$

Auxiliary winding must give enough energy to trigger ZCD threshold to detect zero current. Minimum auxiliary winding turns are given as:

$$N_{AUX} \geq \frac{1.5V \cdot N_{BOOST}}{V_{OUT} - \sqrt{2V_{LINEMAX}}} \text{[Turns]} \quad (18)$$

where 1.5V is the positive threshold of the ZCD pin.

To guarantee stable operation, it is recommended to add 2~3 turns to the auxiliary winding turns calculated in Equation (18). However, too many auxiliary winding turns raise the negative clamping loss at high line and positive clamping loss at low line.

**[STEP-4] ZCD Circuit Design**

If a transition time when $V_{AUXILIARY}$ drops from 1.4V to 0V is ignored from Figure 17, the necessary additional delay by the external resistor and capacitor is one quarter of the resonant period. The time constant made by ZCD resistor and capacitor should be the same as one quarter of the resonant period:

$$\frac{4}{2 \cdot L \cdot C_{ZCD}} \cdot \pi = \pi \quad (19)$$

where $C_{eff}$ is the effective capacitance at the MOSFET drain pin; $C_{ZCD}$ is the external capacitance at the ZCD pin; and $R_{ZCD}$ is the external resistance at the ZCD pin.

The second role of $R_{ZCD}$ is the current limit of the internal negative clamp circuit when auxiliary voltage drops to negative due to MOSFET turn on. ZCD voltage is clamped 0.65V and minimum $R_{ZCD}$ can be given as:

$$R_{ZCD} \geq \frac{0.65V}{N_{AUX} \cdot \sqrt{2V_{LINEMAX} - 0.65V} - 3mA} \text{[\Omega]} \quad (20)$$

where 3mA is the clamping capability of the ZCD pin.

The calculation result of Equation (20) is normally higher than 15kΩ. If 20kΩ is assumed as $R_{ZCD}$, calculated $C_{ZCD}$ from Equation (19) is around 10pF when the other components are assumed as conventional values used in the field. Because most IC pins have several pF of parasitic capacitance, $C_{ZCD}$ can be eliminated when $R_{ZCD}$ is higher than 30kΩ. However, a small capacitor would be helpful when auxiliary winding suffers from operating noise.

The PFC control loop has two conflicting goals: output voltage regulation and making the input current shape the same as input voltage. If the control loop reacts to regulate output voltage smoothly, as shown in Figure 18, control
voltage varies widely with the input voltage variation. Input current acts to the control loop and sinusoidal input current shape cannot be attained. This is the reason control response of most PFC topologies is very slow and turn-on time over AC period is kept constant. This is also the reason output voltage ripple is made by input and output power relationship, not by control-loop performance.

If on-time is controlled constantly over one AC period, the inductor current peak follows AC input voltage shape and achieves good power factor. Off-time is basically inductor current reset time due to Boundary Mode and is determined by the input and output voltage difference. When input voltage is at its peak, the voltage difference between input and output voltage is small and long turn-off time is necessary. When input voltage is near zero, turn-off time is short, as shown in Figure 19 and Figure 20. Though inductor current drops to zero, the minor delay is explained above. The delay can be assumed as fixed when AC is at line peak and zero. Near AC line peak, the inductor current decreasing slope is slow and inductor current slope is also slow during the ZCD delay. The amount of negative current is not much higher than the inductor current peak. Near the AC line zero, inductor current decreasing slope is very high and the amount of negative current is higher than positive inductor current peak because input voltage is almost zero.

Negative inductor current creates zero-current distortion and degrades the power factor. Improve this by extending turn-on time at the AC line input near the zero cross.

Negative auxiliary winding voltage, when the MOSFET is turned on, is linearly proportional to the input voltage. Sourcing current generated by the internal negative clamping circuit is also proportional to sinusoidal input voltage. That current is detected internally and added to the internal sawtooth generator, as shown in Figure 21.

When the AC input voltage is almost zero, no negative current is generated from inside, but sourcing current when input voltage is high is used to raise the sawtooth generator slope and turn-on time is shorter. As a result, turn-on time when AC voltage is zero is longer compared to AC voltage, in peaks shown in Figure 22.
control voltage decreases rapidly. For example, if input voltage doubles, control voltage drops to one quarter. Making control voltage maximum when input voltage is low and at full load is necessary to use the whole control range for the rest of the input voltage conditions. Matching maximum turn-on time needed at low line is calculated in Equation (14) and turn-on time adjustment by $R_{ZCD}$ guarantees use of the full control range. $R_{ZCD}$ for control range optimization is obtained as:

$$R_{ZCD} \geq \frac{28 \mu s}{t_{ON,\text{MAX}1} - t_{ON,\text{MAX}}} \frac{\sqrt{2} \cdot V_{\text{LINE,MIN}} \cdot N_{\text{AUX}}}{0.469 \text{mA} \cdot N_{\text{BOOST}}} \Omega$$  (21)

where:
- $t_{ON,\text{MAX}1}$ is calculated by Equation (14);
- $N_{\text{BOOST}}$ is the winding turns of boost inductor; and
- $N_{\text{AUX}}$ is the auxiliary winding turns.

$R_{ZCD}$ calculated by Equation (20) is normally lower than the value calculated in Equation (21). To guarantee the needed turn-on-time for the boost inductor to deliver rated power, the $R_{ZCD}$ from Equation (20) is normally not suitable. $R_{ZCD}$ should be higher than the result of Equation (21) when output voltage drops as a result of low line voltage.

When input voltage is high and load is light, not much input current is needed and control voltage of $V_{\text{COMP}}$ touches switching stop level, such as if FL7930B is 1V. However, in some applications, a PFC block is needed to operate normally at light load. To compensate control range correctly, input voltage sensing is necessary, such as with Fairchild’s interleaved PFC controller FAN9612, or special care on sawtooth generator is necessary. To guarantee enough control range at high line, clamping output voltage lower than rated on the minimum input condition can help.

### (Design Example) Minimum $R_{ZCD}$ for clamping capability is calculated as:

$$R_{ZCD} \geq \frac{N_{\text{AUX}}}{N_{\text{BOOST}}} \frac{\sqrt{2} \cdot V_{\text{LINE,MAX}} - 0.65V}{3 \text{mA}}$$

$$= \frac{5 \sqrt{2} \cdot 277 - 0.65V}{3 \text{mA}} = 18.9 \Omega$$

Minimum $R_{ZCD}$ for control range is calculated as:

$$R_{ZCD} \geq \frac{28 \mu s}{t_{ON,\text{MAX}1} - t_{ON,\text{MAX}}} \frac{\sqrt{2} \cdot V_{\text{LINE,MIN}} \cdot N_{\text{AUX}}}{0.469 \text{mA} \cdot N_{\text{BOOST}}}$$

$$= \frac{28 \mu s}{4.2 \mu s - 10.9 \mu s} \frac{\sqrt{2} \cdot 0.85 - 5}{0.469 \text{mA} \cdot 55} = 20.97 \Omega$$

A choice close to the value calculated by the control range is recommended. 39kΩ is chosen in this case.
[STEP-5] **Output Capacitor Selection**

The output voltage ripple should be considered when selecting the output capacitor. Figure 25 shows the line frequency ripple on the output voltage. With a given specification of output ripple, the condition for the output capacitor is obtained as:

\[
C_{OUT} \geq \frac{I_{OUT}}{2\pi \cdot f_{LINE} \cdot \Delta V_{OUT,ripple}} \quad \text{(22)}
\]

where \( V_{OUT,ripple} \) is the peak-to-peak output voltage ripple specification.

The output voltage ripple caused by the ESR of the electrolytic capacitor is not as serious as other power converters because output voltage is high and load current is small. Since too much ripple on the output voltage may cause premature OVP during normal operation, the peak-to-peak ripple specification should be smaller than 15% of the nominal output voltage.

The hold-up time should also be considered when determining the output capacitor as:

\[
C_{OUT} \geq \frac{2 \cdot t_{HOLD}}{V_{OUT} - \alpha \cdot (\Delta V_{OUT,ripple})^2 - V_{OUT,MIN}} \quad \text{(23)}
\]

where \( t_{HOLD} \) is the required hold-up time and \( V_{OUT,MIN} \) is the minimum output voltage during hold-up time.

![Figure 25. Output Voltage Ripple](image)

The voltage rating of capacitor can be obtained as:

\[
V_{ST,COUT} = \frac{V_{OV,P MAX}}{V_{REF}} \cdot V_{OUT} [V] \quad \text{(24)}
\]

where \( V_{OV,P MAX} \) and \( V_{REF} \) are the maximum tolerance specifications of over-voltage protection triggering voltage and reference voltage at error amplifier, respectively.

(Design Example) With the ripple specification of 8V\(_{pp}\), the capacitor should be:

\[
C_{O} \geq \frac{I_{OUT}}{2\pi \cdot f_{LINE} \cdot \Delta V_{OUT,ripple}} = \frac{0.455}{2\pi \cdot 50 \cdot 8} = 110 [\mu F]
\]

Since minimum allowable output voltage during one cycle (20ms) drop-outs is 330V, the capacitor should be:

\[
C_{O} \geq \frac{2 \cdot V_{OUT} - V_{OUT,MIN}}{2 \cdot 200 \cdot 2 \times 10^{-3}} = \frac{430 - 0.5 \cdot 8}{200 \times 2 \times 10^{-3}} = 110 [\mu F]
\]

To meet both conditions, the output capacitor must be larger than 140\( \mu \)F. A 240\( \mu \)F capacitor is selected for the output capacitor.

[STEP-6] **MOSFET and DIODE Selection**

Selecting the MOSFET and diode requires extensive knowledge and calculation regarding loss mechanisms and gets more complicated if proper selection of a heatsink is added. Sometimes the loss calculation itself is based on assumptions that may be far from reality. Refer to industry resources regarding these topics. This note shows the voltage rating and switching loss calculations based on a linear approximation.

The voltage stress of the MOSFET is obtained as:

\[
V_{ST,Q} = \frac{V_{OV,P MAX}}{V_{REF}} \cdot V_{OUT} + V_{DROP,DOUT} [V] \quad \text{(25)}
\]

where \( V_{DROP,DOUT} \) is the maximum forward-voltage drop of output diode.

After the MOSFET is turned off, the output diode turns on and a large output electrolytic capacitance is shown at the drain pin; thus a drain voltage clamping circuit that is necessary on other topologies is not necessary in PFC. During the turn-off transient, boost inductor current changes the path from MOSFET to output diode. Before the output diode turns on; a minor voltage peak can be shown at drain pin, which is proportional to MOSFET turn-off speed.

MOSFET loss can be divided into three parts: conduction loss, turn-off loss, and discharge loss. Boundary mode guarantees Zero Current Switching (ZCS) of the MOSFET when turned on, so turn-on loss is negligible.

The MOSFET RMS current and conduction loss are obtained as:

\[
I_{Q,RMS} = \frac{I_{L,PK}}{\sqrt{2}} \cdot \frac{\sqrt{2} \cdot V_{LINE}}{\sqrt{2} \cdot V_{OUT}} [A] \quad \text{(26)}
\]

\[
P_{Q,CON} = (I_{Q,RMS})^2 \cdot R_{DS,ON} [W] \quad \text{(27)}
\]
where $I_{Q,\text{RMS}}$ is the RMS value of MOSFET current, $P_{Q,\text{CON}}$ is the conduction loss caused by MOSFET current, and $R_{DS,\text{ON}}$ is the ON resistance of the MOSFET.

On resistance is described as “static on resistance” and varies depending on junction temperature. That variation information is normally supplied as a graph in the datasheet and may vary by manufacturer. When calculating conduction loss, generally multiply three by the $R_{DS,\text{ON}}$ for more accurate estimation.

The precise turn-off loss calculation is difficult because of the nonlinear characteristics of MOSFET turn-off. When piecewise linear current and voltage of MOSFET during turn-off and inductive load are assumed, MOSFET turn-off loss is obtained as:

$$P_{Q,\text{SWOFF}} = \frac{1}{2} V_{\text{OUT}} I_{L\cdot t_{\text{OFF}}} f_{\text{SW}} [W]$$  \hspace{1cm} (28)

where $t_{\text{OFF}}$ is the turn-off time and $f_{\text{SW}}$ is the switching frequency.

Boundary Mode PFC inductor current and switching frequency vary at every switching moment. RMS inductor current and average switching frequency over one AC period can be used instead of instantaneous values.

Individual loss portions are changed according to the input voltage; maximum conduction loss appears at low line because of high input current; and maximum switching off loss appears at high line because of the high switching frequency. The resulting loss is always lower than the summation of the two losses calculated above.

Capacitive discharge loss made by effective capacitance shown at drain and source, which includes MOSFET $C_{\text{OSS}}$, an externally added capacitor to reduce dv/dt and parasitic capacitance shown at drain pin, is also dissipated at MOSFET. That loss is calculated as:

$$P_{Q,\text{DISCHG}} = \frac{1}{2} (C_{\text{OSS}} + C_{\text{EXT}} + C_{\text{PAR}}) V_{\text{OUT}}^2 f_{\text{SW}} [W]$$  \hspace{1cm} (29)

where:

- $C_{\text{OSS}}$ is the output capacitance of MOSFET;
- $C_{\text{EXT}}$ is an externally added capacitance at drain and source of MOSFET; and
- $C_{\text{PAR}}$ is the parasitic capacitance at drain pin.

Because the $C_{\text{OSS}}$ is a function of the drain and source voltage, it is necessary to refer to graph data showing the relationship between $C_{\text{OSS}}$ and voltage.

Estimate the total power dissipation of MOSFET as the sum of three losses:

$$P_Q = P_{Q,\text{CON}} + P_{Q,\text{SWOFF}} + P_{Q,\text{DISCHG}} [W]$$  \hspace{1cm} (30)

Diode voltage stress is the same as the output capacitor stress calculated in Equation (24).

The average diode current and power loss are obtained as:

$$I_{\text{DOUT,AVE}} = \frac{I_{\text{OUT}}}{\eta} [A]$$  \hspace{1cm} (31)

$$P_{\text{DOUT}} = V_{\text{DROPOUT}} I_{\text{DOUT,AVE}} [W]$$  \hspace{1cm} (32)

where $V_{\text{DROPOUT}}$ is the forward voltage drop of diode.

### (Design Example)

Internal reference at the feedback pin is 2.5V and maximum tolerance of OVP trigger voltage is 2.73V. If Fairchild’s FDPF17N60NT MOSFET and FFP08H60S diode are selected, $V_{\text{D,FOR}}$ is 2.1V at 8A, 25°C, maximum $R_{DS,\text{ON}}$ is 0.34Ω at drain current is 17A, and maximum $C_{\text{OSS}}$ is 32pF at drain-source voltage is 480V.

$$V_{\text{ST,Q}} = \frac{V_{\text{DPMAX}}}{V_{\text{REF}}} \cdot (V_{\text{OUT}} + V_{\text{DROPOUT}})$$

$$= \frac{27.5}{2.5} \cdot (450 + 2.1) = 4766 [V]$$

$$P_{Q,\text{CON}} = \left( \frac{I_{\text{PK}} \sqrt{\frac{2}{\pi} \cdot \frac{V_{\text{GATE}}}{\eta \cdot V_{\text{OUT}}}} \right)^2 \cdot \frac{V_{\text{OUT}}}{R_{\text{DS,ON}}}$$

$$= \left( \frac{7.592 \cdot 4.5}{\pi \cdot 450} \right) \cdot (0.34) = 2.25 [W]$$

$$P_{Q,\text{SWOFF}} = \frac{1}{2} V_{\text{OUT}} \cdot I_{L\cdot t_{\text{OFF}}} \cdot f_{\text{SW}}$$

$$= \frac{1}{2} \cdot 450 \cdot 2.615 \cdot 50 \mu s \cdot (50 \text{ k} / \text{ \Omega}) = 1.755 [W]$$

$$P_{Q,\text{DISCHG}} = \frac{1}{2} (C_{\text{OSS}} + C_{\text{EXT}} + C_{\text{PAR}}) V_{\text{OUT}}^2 \cdot f_{\text{SW}}$$

$$= \frac{1}{2} \cdot 52 \text{ p} \cdot 450^2 \cdot (50 \text{ k} / \text{ \Omega}) = 0.164 [W]$$

Diode average current and forward-voltage drop loss as:

$$I_{\text{DOUT,AVE}} = \frac{I_{\text{OUT}}}{\eta} \cdot \frac{5}{6} = 0.5 \cdot \frac{5}{6} = 0.5 [A]$$

$$P_{\text{DOUT,LOSS}} = V_{\text{DROPOUT}} \cdot I_{\text{DOUT,AVE}} \cdot 2.1 \cdot 0.5 = 1.46 [W]$$

### [STEP-7] Determine Current-Sense Resistor

It is typical to set pulse-by-pulse current limit level a little higher than the maximum inductor current calculated by Equation (10). For 10% margin, the current-sensing resistor is selected as:

$$R_{\text{CS,SLM}} = \frac{V_{\text{CS,SLM}}}{I_{\text{PK}}} - 11 \Omega$$  \hspace{1cm} (33)

Once resistance is calculated, its power loss at low line is calculated as:

$$P_{RCS} = I_{Q,\text{RMS}}^2 \cdot R_{\text{CS}} [W]$$  \hspace{1cm} (34)

Power rating of the sensing resistor is recommended a twice the power rating calculated in Equation (34).
(Design Example) Maximum inductor current is 4.889A and sensing resistor is calculated as:

\[ R_{CS} = \frac{V_{CS, MAX}}{I_{ind, MAX}} = \frac{0.8}{7.582 \times 10^{-7}} = 0.098 \Omega \]

Choosing 0.1Ω as \( R_{CS} \), power loss is calculated as:

\[ P_{RCS, LOSS} = I_{PK, RMS}^2 \cdot R_{CS} = 2.43 \times 2 \cdot 0.098 = 1.19 \text{W} \]

Recommended power rating of sensing resistor is 1.19W.

[STEP-8] Design Compensation Network

The boost PFC power stage can be modeled as shown in Figure 26 MOSFET and diode can be changed to loss-free resistor model and then modeled as a voltage-controlled current source supplying RC network.

\[ V_{AC, RMS} \]

\[ D_{OUT} \]

\[ V_{OUT} \]

\[ I_0 \]

\[ C_{OUT} \]

\[ R_L \]

\[ L_{OCOST} \]

\[ V_{OUT} \]

\[ V_{AC, RMS} \]

\[ R_L = R_{C, RESISTIVE LOAD} \]

\[ R_{L, OUT} \]

\[ C_{OUT} \]

\[ V_{OUT} \]

\[ V_{OUT} \]

\[ V_{OUT} \]

\[ V_{OUT} \]

\[ V_{OUT} \]

\[ V_{OUT} \]

Figure 26. Small Signal Modeling of the Power Stage

By averaging the diode current during the half line cycle, the low-frequency behavior of the voltage controlled current source of Figure 26 is obtained as:

\[ I_{DOUT, AVE} = K_{SAAW} \frac{\sqrt{V_{LINE, RMS} \cdot V_{AC, RMS}}}{\sqrt{V_{OUT, RMS}}} \cdot \frac{\pi}{L} \]  \hspace{1cm} (35)

where:

- \( L \) is the boost inductance;
- \( V_{OUT} \) is the output voltage; and
- \( K_{SAAW} \) is the internal gain of sawtooth generator (that of FL7930B is 8.496 × 10^{-6}).

Then the low-frequency, small-signal, control-to-output transfer function is obtained as:

\[ \frac{V_{OUT}^{\wedge}}{V_{COMP}^{\wedge}} = \frac{K_{SAAW} \left( \frac{V_{LINE}}{V_{OUT}} \right)^2 R_L}{\frac{f}{2 \pi f_p}} \frac{f}{s + \frac{f_p}{2 \pi f_p}} \]  \hspace{1cm} (36)

where \( f_p = \frac{2}{\pi R_L C_{OUT}} \) and \( R_L \) is the output resistance in a given load condition.

Figure 27 and Figure 28 show the variation of the control-to-output transfer function for different input voltages and different loads. Since DC gain and crossover frequency increase as input voltage increases, and DC gain increases as load decreases, high input voltage and light load is the worst condition for feedback loop design.

Proportional and integration (PI) control with high-frequency pole is typically used for compensation, as shown in Figure 29. The compensation zero (\( f_{CZ} \)) introduces phase boost, while the high-frequency compensation pole (\( f_{CP} \)) attenuates the switching ripple.

The transfer function of the compensation network is obtained as:

\[ \frac{V_{COMP}^{\wedge}}{V_{OUT}^{\wedge}} = \frac{2 \pi f_C}{s + \frac{2 \pi f_C}{2 \pi f_{CZ}}} \]  \hspace{1cm} (37)
\[ f_l = \frac{25}{V_{OUT}} \frac{115\mu \text{mho}}{2\pi \left( \frac{1}{C_{\text{COMP,LF}}} + \frac{1}{C_{\text{COMP,LF}}} \right)} \]

where \[ f_{CZ} = \frac{1}{2\pi \cdot R_{\text{COMP}} \cdot C_{\text{COMP,LF}}} \]

\[ f_{CP} = \frac{f}{2\pi \cdot R_{\text{COMP}} \cdot C_{\text{COMP,LF}}} \]

If \( C_{\text{COMP,LF}} \) is much larger than \( C_{\text{COMP,LF}} \), \( f_l \) and \( f_{CP} \) can be simplified as:

\[ f_l \approx \frac{25}{V_{OUT}} \frac{115\mu \text{mho}}{2\pi \cdot C_{\text{COMP,LF}}} \text{ [Hz]} \]

\[ f_{CP} \approx \frac{f}{2\pi \cdot R_{\text{COMP}} \cdot C_{\text{COMP,LF}}} \text{ [Hz]} \]  

(38)

Typically, high \( R_{FB1} \) is used to reduce power consumption and \( C_{FB} \) can be added to raise the noise immunity. The maximum \( C_{FB} \) currently used is several nano farads. Adding a capacitor at the feedback loop introduces a pole as:

\[ f_{FP} = \frac{1}{2\pi \cdot \left( R_{FB1} \parallel R_{FB2} \right) \cdot C_{FB}} \]

\[ \approx \frac{f}{2\pi \cdot R_{FB2} \cdot C_{FB}} \text{ [Hz]} \]  

(40)

where \( R_{FB1} \parallel R_{FB2} = \frac{R_{FB1} \cdot R_{FB2}}{R_{FB1} + R_{FB2}} \)

Though \( R_{FB1} \) is high, pole frequency made by the synthesized total resistance and several nano farads is several kilo hertz and rarely affects control-loop response.

The procedure to design the feedback loop is:

a. Determine the crossover frequency \( f_c \) around 1/10 ~ 1/5 of line frequency. Since the control-to-output transfer function of the power stage has -20dB/dec slope and -90° phase at the crossover frequency; it is required to place the zero of the compensation network \( f_{CZ} \) around the crossover frequency so 45° phase margin is obtained. The capacitor \( C_{\text{COMP,LF}} \) is determined as:

\[ C_{\text{COMP,LF}} = \frac{K_{SAT} \cdot V_{LINE}}{2 \cdot V_{OUT} \cdot L \cdot C_{OUT} \cdot \left( \frac{1}{2\pi f_c} \right)^2} \text{ [f]} \]  

(41)

To place the compensation zero at the crossover frequency, the compensation resistor is obtained as:

\[ R_{\text{COMP}} = \frac{1}{2\pi f_c \cdot C_{\text{COMP,LF}}} \text{ [\Omega]} \]  

(42)

b. Place this compensator high-frequency pole \( f_{CP} \) at least a decade higher than \( f_c \) to ensure that it does not interfere with the phase margin of the voltage regulation loop at its crossover frequency. It should also be sufficiently lower than the switching frequency of the converter for noise to be effectively attenuated. The capacitor \( C_{\text{COMP,HE}} \) is determined as:

\[ C_{\text{COMP,HE}} = \frac{1}{2\pi f_{CP} \cdot R_{\text{COMP}}} \text{ [\Omega]} \]  

(43)
(Design Example) If $R_{FB1}$ is 11.7MΩ, then $R_{FB2}$ is:

\[ R_{FB2} = 2.5V/V_{OUT} - 2.5R_{FB1} = \frac{2.5}{430} - 2.5 \times 1.17 \times 10^8 = 68kΩ \]

Choosing the crossover frequency (control bandwidth) at 15Hz, $C_{COMP,LF}$ is obtained as:

\[ C_{COMP,LF} = \frac{K_{SFAW}(V_{LINE})^2 \cdot 2.5 \cdot 115 \mu mho}{2 \cdot V_{OUT} \cdot L \cdot C_{OUT} \cdot (2\pi f_c)^2} = -8.496 \times 10^{-4} (230)^2 \cdot 2.5 \cdot 115 \times 10^{-6} \\
= \frac{2 \cdot 430 \cdot 199 \times 10^{-6} \cdot 240 \times 10^{-6} (2\pi 15)^2}{823 nF} \]

Actual $C_{COMP,LF}$ is determined as 1000nF since it is the closest value among the off-the-shelf capacitors. $R_{COMP}$ is obtained as:

\[ R_{COMP} = \frac{1}{2\pi \cdot f_c \cdot C_{COMP,LF}} = \frac{1}{2\pi \cdot 15 \cdot 823 \times 10^{-6}} = 12.8kΩ \]

Selecting the high-frequency pole as 150Hz, $C_{COMP,HF}$ is obtained as:

\[ C_{COMP,HF} = \frac{1}{2\pi \cdot f_{HF} \cdot R_{COMP}} = \frac{1}{2\pi \cdot 150 \cdot 12.8 \times 10^{-6}} = 82nF \]

These components result in a control loop with a bandwidth of 19.5Hz and phase margin of 45.6°. The actual bandwidth is a little larger than the asymptotic design.

[STEP-9] Line Filter Capacitor Selection

It is typical to use small bypass capacitors across the bridge rectifier output stage to filter the switching current ripple, as shown in Figure 30. Since the impedance of the line filter inductor at line frequency is negligible compared to the impedance of the capacitors, the line frequency behavior of the line filter stage can be modeled, as shown in Figure 30. Even though the bypass capacitors absorb switching ripple current, they also generate circulating capacitor current, which leads the line voltage by 90°, as shown in Figure 31. The circulating current through the capacitor is added to the load current and generates displacement between line voltage and current.

The displacement angle is given by:

\[ \theta = \tan^{-1} \left( \frac{\eta \cdot (V_{LINE})^2 \cdot 2\pi \cdot f_{LINE} \cdot C_{EQ}}{R_{OUT}} \right) \]

where $C_{EQ}$ is the equivalent capacitance that appears across the AC line ($C_{EQ}=C_{F1}+C_{F2}+C_{HF}$). The resultant displacement factor is:

\[ DF = \cos(\theta) \]

Since the displacement factor is related to power factor, the capacitors in the line filter stage should be selected carefully. With a given minimum displacement factor ($DF_{MIN}$) at full-load condition, the allowable effective input capacitance is obtained as:

\[ C_{EA} < \frac{P_{OUT}}{\eta \cdot (V_{LINE})^2 \cdot 2\pi \cdot f_{LINE} \cdot tan(\cos^{-1}(DF_{MIN}))} \]

One way to determine if the input capacitor is too high or PFC control routine has problems is to check Power Factor (PF) and Total Harmonic Distortion (THD). PF is the degree to which input energy is effectively transferred to the load by the multiplication of displacement factor and THD that is input current shape deterioration ratio. PFC control loop rarely has no relation to displacement factor and input capacitor rarely has no impact on the input current shape. If PF is low (high is preferable), but THD is quite good (low is preferable), it can be concluded that input capacitance is too high and PFC controller is fine.

(Design Example) Assuming the minimum displacement factor at full load is 0.98, the equivalent input capacitance is obtained as:

\[ C_{EA} < \frac{P_{OUT}}{\eta \cdot (V_{LINE})^2 \cdot 2\pi \cdot f_{LINE} \cdot tan(\cos^{-1}(0.98))} \]

\[ < \frac{200}{0.9 \cdot (277)^2 \cdot 2\pi \cdot 50} \cdot tan(\cos^{-1}(0.98)) = 1.6μF \]

Thus, the sum of the capacitors on the input side should be smaller than 2.0μF.
[STEP-10] Define System Specifications

Estimated Efficiency \( (E_i) \): The power conversion efficiency must be estimated to calculate the maximum input power with a given maximum output power. If no reference data is available, use \( E_i = 0.88 \text{–} 0.92 \) for low-voltage output applications and \( E_i = 0.92 \text{–} 0.96 \) for high-voltage output applications. With the estimated efficiency, the maximum input power is given as:

\[
P_{in} = \frac{P_{out}}{E_i}
\]  

(47)

Input Voltage Range \( (V_{in \text{min}} \text{ and } V_{in \text{max}}) \): The maximum input voltage would be the nominal PFC output voltage as:

\[
V_{in \text{max}} = V_{O,PFC}
\]  

(48)

Even though the input voltage is regulated as constant by PFC pre-regulator, it drops during the hold-up time. The minimum input voltage considering the hold-up time requirement is given as:

\[
V_{in \text{min}} = \sqrt{V_{O,PFC}^2 - \frac{2P_{in}T_{HU}}{C_{DL}}} 
\]  

(49)

where \( V_{O,PFC} \) is the nominal PFC output voltage, \( T_{HU} \) is a hold-up time, and \( C_{DL} \) is the DC link bulk capacitor.

(Design Example) Assuming the efficiency is 92%,

\[
P_{in} = \frac{P_{out}}{E_i} = \frac{150}{0.92} = 163W
\]

\[
V_{in \text{min}} = \sqrt{V_{O,PFC}^2 - \frac{2P_{in}T_{HU}}{C_{DL}}} = \sqrt{430^2 - \frac{2 \cdot 163 \cdot 30 \times 10^{-3}}{240 \times 10^{-6}}} = 379V
\]


As discussed in the previous section, it is typical to operate the LLC resonant converter around the resonant frequency \( (f_o) \) to minimize switching frequency variation. Since the input of the LLC resonant converter is supplied from PFC output voltage, the converter should be designed to operate at \( f_o \) for the nominal PFC output voltage.

As observed in Equation (9), the gain at \( f_o \) is a function of \( m \) \( (m = L_2/L_1) \). The gain at \( f_o \) is determined by choosing that value of \( m \). While a higher peak gain can be obtained with a small \( m \) value, too small \( m \) value results in poor coupling of the transformer and deteriorates the efficiency. It is typical to set \( m \) to be 3\text{–}7, which results in a voltage gain of 1.1\text{–}1.2 at the resonant frequency \( (f_o) \).

With the chosen \( m \) value, the voltage gain for the nominal PFC output voltage is obtained as:
which would be the minimum gain because the nominal PFC output voltage is the maximum input voltage \( V_{in}^{max} \).

The maximum voltage gain is given as:

\[
M_{\text{max}} = \frac{V_{in}^{max}}{V_{in}^{min}} M_{\text{min}} \tag{51}
\]

\( M_{\text{min}} = \sqrt{\frac{m}{m-1}} \) \( @f=f_o \) \hspace{1cm} \tag{50}

\[
R_{\text{ac}} = \frac{8n^2 V_o^2}{\pi^2 P_o} \tag{53}
\]

### (Design Example)

The ratio \( m \) between \( L_p \) and \( L_r \) is chosen as 5. The minimum and maximum gains are obtained as:

\[
M_{\text{min}} = \frac{V_{RO}}{\sqrt{V_{in}^{max}^2 / 2}} = 1.12 \sqrt{\frac{m}{m-1}} = 1.12 \sqrt{\frac{5}{5-1}} = 1.12
\]

\[
M_{\text{max}} = \frac{V_{in}^{max} / m_{\text{min}}}{V_{in}^{min} / m_{\text{min}}} = \frac{400}{341} \cdot 1.12 = 1.31
\]

\[ \text{Gain (M) for } V_{in}^{min} \]

\[ \text{Peak Gain (Available Maximum Gain)} \]

\[ 1.31 \]

\[ 1.12 \]

\[ \text{for } V_{in}^{max} \]

\[ \text{for } V_{in}^{min} \]

\[ \text{m=M} \]

\[ \text{V_{O,PFC}} \]

\[ \text{f_o} \]

\[ \text{f_s} \]

Figure 32. Maximum Gain / Minimum Gain

### [STEP-12] Determine the Transformer Turns Ratio \( (n=N_p/N_s) \)

With the minimum gain \( (M_{\text{min}}) \) obtained in STEP-11, the transformer turns ratio is given as:

\[
n = \frac{N_p}{N_s} = \frac{V_{in}^{max}}{2(W_o + V_F)} \cdot M_{\text{min}} \tag{52}
\]

where \( V_F \) is the secondary-side rectifier diode voltage drop.

### (Design Example)

assuming \( V_F \) is 0.9V:

\[
n = \frac{N_p}{N_s} = \frac{V_{in}^{max}}{2(W_o + V_F)} \cdot M_{\text{min}} = \frac{430}{2 \cdot (103 + 0.9)} \cdot 1.12 \cdot 1.2 = 2.06
\]

### [STEP-13] Calculate Equivalent Load Resistance

With the transformer turns ratio obtained from Equation (52), the equivalent load resistance is obtained as:

\[
L_p = m \cdot L_r = 665 \mu H
\]

\[
C_r = \frac{1}{2\pi f_o R_{\text{ac}}} = 19 \mu F
\]

\[
L_r = \frac{1}{(2\pi f_o)^2 C_r} = 153 \mu H
\]

### [STEP-14] Design the Resonant Network

With the \( m \) value chosen in STEP-11, read the proper \( Q \) value from the peak gain curves in Figure 33 that allows enough peak gain. Considering the load transient and stable zero-voltage-switching (ZVS) operation, 10~20% margin should be introduced on the maximum gain when determining the peak gain. Once the \( Q \) value is determined, the resonant parameters are obtained as:

\[
C_r = \frac{1}{2\pi f_o R_{\text{ac}}} \tag{54}
\]

\[
L_r = \frac{1}{(2\pi f_o)^2 C_r} \tag{55}
\]

\[
L_p = m \cdot L_r \tag{56}
\]

### (Design Example)

As calculated in STEP-11, the maximum voltage gain \( (M_{\text{max}}) \) for the minimum input voltage \( (V_{in}^{min}) \) is 1.31. With 15% margin, a peak gain of 1.51 is required. \( m \) has been chosen as 5 in STEP-11 and \( Q \) is obtained as 0.38 from the peak gain curves in Figure 33. By selecting the resonant frequency as 100kHz, the resonant components are determined as:

\[
C_r = \frac{1}{2\pi f_o R_{\text{ac}}} = \frac{1}{2\pi \cdot 0.38 \cdot 100 \times 10^{-3} \cdot 217} = 59 \mu F
\]

\[
L_r = \frac{1}{(2\pi f_o)^2 C_r} = \frac{1}{(2\pi \times 100 \times 10^{-3})^2 \cdot 59 \times 10^{-6}} = 153 \mu H
\]

\[
L_p = m \cdot L_r = 665 \mu H
\]
[STEP-15] Design the Transformer

The worst case for the transformer design is the minimum switching frequency condition, which occurs at the minimum input voltage and full-load condition. To obtain the minimum switching frequency, plot the gain curve using gain Equation (8) and read the minimum switching frequency. The minimum number of turns for the transformer primary-side is obtained as:

\[
N_p^\text{min} = \frac{n(V_o + V_F)}{2f_s^\text{max} \cdot M_p \cdot \Delta B \cdot A_e}
\]  

(57)

where \(A_e\) is the cross-sectional area of the transformer core in \(m^2\) and \(\Delta B\) is the maximum flux density swing in Tesla, as shown in Figure 34. If there is no reference data, use \(\Delta B = 0.3-0.4\) T.

Choose the proper number of turns for the secondary side that results in primary-side turns larger than \(N_p^\text{min}\) as:

\[
N_p = n \cdot N_s > N_p^\text{min}
\]  

(58)

(Design Example) EER3542 core (\(A_e=107mm^2\)) is selected for the transformer. From the gain curve of Figure 35, the minimum switching frequency is obtained as 82KHz. The minimum primary-side turns of the transformer is given as:

\[
N_p^\text{min} = \frac{n(V_o + V_F)}{2f_s^\text{min} \cdot \Delta B \cdot 1.11 \cdot A_e} = \frac{1.93 \times 103.9}{2 \times 82 \times 10^{-1} \times 0.411 \times 10^{-7} \times 10^{-10}} = 26 \text{ turns}
\]

Choose \(N_s\) so that the resultant \(N_p\) is larger than \(N_p^\text{min}\):

\[
N_p = n \cdot N_s = 1.93 \times 14 = 27 < N_p^\text{min}
\]

\[
N_p = n \cdot N_s = 1.93 \times 15 = 29 < N_p^\text{min}
\]

\[
N_p = n \cdot N_s = 1.93 \times 16 = 31 > N_p^\text{min}
\]

\[
N_p = n \cdot N_s = 1.93 \times 17 = 33 > N_p^\text{min}
\]

\[
N_p = n \cdot N_s = 1.93 \times 18 = 35 > N_p^\text{min}
\]

\[
N_p = n \cdot N_s = 1.93 \times 19 = 37 > N_p^\text{min}
\]

[STEP-16] Transformer Construction

Parameters \(L_p\) and \(L_r\) of the transformer were determined in STEP-14. \(L_p\) and \(L_r\) can be measured in the primary side with the secondary-side winding open circuited and short circuited, respectively. Since LLC converter design requires a relatively large \(L_r\), a sectional bobbin is typically used, as shown in Figure 36, to obtain the desired \(L_r\) value. For a sectional bobbin, the number of turns and winding configuration are the major factors determining the value of \(L_r\), while the gap length of the core does not affect \(L_r\) much. \(L_p\) can be controlled by adjusting the gap length. Table 1. shows measured \(L_p\) and \(L_r\) values with different gap lengths. A gap length of 0.05mm obtains values for \(L_p\) and \(L_r\) closest to the designed parameters.

Table 1. Measured \(L_p\) and \(L_r\) with Different Gap Lengths

<table>
<thead>
<tr>
<th>Gap Length</th>
<th>(L_p)</th>
<th>(L_r)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0mm</td>
<td>2,295µH</td>
<td>123µH</td>
</tr>
<tr>
<td>0.05mm</td>
<td>943µH</td>
<td>122µH</td>
</tr>
<tr>
<td>0.10mm</td>
<td>630µH</td>
<td>118µH</td>
</tr>
<tr>
<td>0.15mm</td>
<td>488µH</td>
<td>117µH</td>
</tr>
<tr>
<td>0.20mm</td>
<td>419µH</td>
<td>115µH</td>
</tr>
<tr>
<td>0.25mm</td>
<td>366µH</td>
<td>114µH</td>
</tr>
</tbody>
</table>
(Design Example)

Final Resonant Network Design

Even though the integrated transformer approach in LLC resonant converter design can implement the magnetic components in a single core and save one magnetic component, the value of $L_r$ is not easy to control in real transformer design. Resonant network design sometimes requires iteration with a resultant $L_r$ value after the transformer is built. The resonant capacitor value is also changed since it should be selected among off-the-shelf capacitors. The final resonant network design is summarized in Table 2. and the new gain curves are shown in Figure 37.

### Table 2. Final Resonant Network Design Parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Initial Design</th>
<th>Final Design</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_p$</td>
<td>665µH</td>
<td>691µH</td>
</tr>
<tr>
<td>$L_r$</td>
<td>133H</td>
<td>122µH</td>
</tr>
<tr>
<td>$C_r$</td>
<td>19nF</td>
<td>22nF</td>
</tr>
<tr>
<td>$f_o$</td>
<td>100kHz</td>
<td>96kHz</td>
</tr>
<tr>
<td>$m$</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>$Q$</td>
<td>0.38</td>
<td>0.3</td>
</tr>
<tr>
<td>$M$ at $f_o$</td>
<td>1.12</td>
<td>1.12</td>
</tr>
<tr>
<td>Minimum Frequency</td>
<td>75kHz</td>
<td>74.4kHz</td>
</tr>
</tbody>
</table>

![Figure 37. Gain Curve of the Final Resonant Network Design](image)

The nominal voltage of the resonant capacitor in normal operation is given as:

$$V_{C_{nom}} \approx \frac{V_{in}^{max} + \sqrt{2} \cdot I_{rms_{C_r}}}{2} + \frac{\sqrt{2} \cdot f_o \cdot C_r}{2 \cdot \pi \cdot f_o}$$

(60)

However, the resonant capacitor voltage increases higher than this at overload condition or load transient. Actual capacitor selection should be based on the Over-Current Protection (OCP) trip point. With the OCP current, $I_{OCP}$, the maximum resonant capacitor voltage is obtained as:

$$V_{C_{nom}} = \frac{V_{in}^{max} + I_{OCP}}{2} + \frac{I_{OCP} \cdot f_o \cdot C_r}{2 \cdot \pi \cdot f_o}$$

(61)

### [STEP-17] Select the Resonant Capacitor

When choosing the resonant capacitor, the current rating should be considered because a considerable amount of current flows through the capacitor. The RMS current through the resonant capacitor is given as:

$$I_{C_{r, RMS}} = \frac{1}{E_{ff}} \sqrt{\frac{\pi I_{o}}{2 \cdot \sqrt{2} n}} + \frac{n(V_o + V_F)}{2 \cdot \sqrt{2} f_o M_r (L_p - L_s)}$$

(59)

The peak current in the primary side in normal operation is:

$$I_{C_{peak}} = \sqrt{2} \cdot I_{C_{nom}} = 1.58A$$

The OCP level is set to 2.5A with 50% margin on $I_{C_{peak}}$:

$$V_{C_{nom}} = \frac{V_{in}^{max} + \sqrt{2} \cdot I_{rms_{C_r}}}{2} + \frac{\sqrt{2} \cdot f_o \cdot C_r}{2 \cdot \pi \cdot f_o}$$

$$= \frac{430 + \sqrt{2} \cdot 1.18}{2 \cdot \pi \cdot 9.6 \times 10^3 \cdot 22 \times 10^9} = 340V$$

$$V_{C_{max}}^{max} = \frac{V_{in}^{max} + I_{OCP} \cdot f_o \cdot C_r}{2} + \frac{2.5}{2 \cdot \pi \cdot 9.6 \times 10^3 \cdot 22 \times 10^9} = 403.3V$$

A 630V rated low-ESR film capacitor is selected for the resonant capacitor.

### [STEP-18] Rectifier Network Design

When the center tap winding is used in the transformer secondary side, the diode voltage stress is twice of the output voltage expressed as:

$$V_D = 2(V_o + V_F)$$

(62)

The RMS value of the current flowing through each rectifier diode is given as:

$$I_{D_{rms}} = \frac{\pi}{4} I_o$$

(63)
Meanwhile, the ripple current flowing through output capacitor is given as:

\[ I_{\text{Co, RMS}} = \sqrt{\left(\frac{\pi I_o}{2\sqrt{2}}\right)^2 - I_o^2} = \sqrt{\frac{\pi^2 - 8}{8}} I_o \]  

(64)

The voltage ripple of the output capacitor is:

\[ \Delta V_o = \frac{\pi}{2} I_o \cdot R_C \]  

(65)

where \( R_C \) is the effective series resistance (ESR) of the output capacitor and the power dissipation is the output capacitor is:

\[ P_{\text{Loss,Co}} = (I_{\text{Co, RMS}})^2 \cdot R_C \]  

(66)

### Design Example

The voltage stress and current stress of the rectifier diode are:

\[ V_D = 2(V_o + V_F) = 2(103 + 0.9) = 207.8V \]

\[ I_D\,\text{RMS} = \frac{\pi}{4} I_o = 1.14A \]

The 600V/8A ultra-fast recovery diode is selected for the rectifier, considering the voltage overshoot caused by the stray inductance.

The RMS current of the output capacitor is:

\[ I_{\text{Co, RMS}} = \sqrt{\left(\frac{\pi I_o}{2\sqrt{2}}\right)^2 - I_o^2} = \sqrt{\frac{\pi^2 - 8}{8}} I_o = 0.584A \]

When two electrolytic capacitors with ESR of 100mΩ are used in parallel, the output voltage ripple is given as:

\[ \Delta V_o = \frac{\pi}{2} I_o \cdot R_C = \frac{\pi}{2} \cdot 1.46 \cdot \frac{0.1}{2} = 0.114V \]

The loss in electrolytic capacitors is:

\[ P_{\text{Loss,Co}} = (I_{\text{Co, RMS}})^2 \cdot R_C = 0.584^2 \cdot 0.05 = 0.017W \]

### [STEP-19] Control Circuit Configuration

Figure 38 shows the typical circuit configuration for the RT pin of FAN7621S, where the optocoupler transistor is connected to the RT pin to control the switching frequency. The minimum switching frequency occurs when the optocoupler transistor is fully tuned off, which is given as:

\[ f_{\text{min}} = \frac{5.2k\Omega}{R_{\text{min}}} \times 100(kHz) \]  

(67)

Assuming the saturation voltage of optocoupler transistor is 0.2V, the maximum switching frequency is determined as:

\[ f_{\text{max}} = \left(\frac{5.2k\Omega}{R_{\text{min}}} + \frac{4.68k\Omega}{R_{\text{max}}}\right) \times 100(kHz) \]  

(68)

### Figure 38. Typical Circuit Configuration for RT Pin

Soft-start prevents excessive inrush current and overshoot of output voltage during startup, increases the voltage gain of the resonant converter progressively. Since the voltage gain of the resonant converter is inversely proportional to the switching frequency, soft-start is implemented by sweeping down the switching frequency from an initial high frequency \( f^\text{ISS} \) until the output voltage is established, as illustrated in Figure 39. The soft-start circuit is made by connecting RC series network on the RT pin as shown in Figure 38. FAN7621S also has an internal soft-start for 3ms to reduce the current overshoot during the initial cycles, which adds 40KHz to the initial frequency of the external soft-start circuit, as shown in Figure 39. The actual initial frequency of the soft-start is given as:

\[ f^\text{ISS} = \left(\frac{5.2k\Omega}{R_{\text{min}}} + \frac{5.2k\Omega}{R_{\text{SS}}}\right) \times 100 + 40(kHz) \]  

(69)

It is typical to set the initial frequency of soft-start \( f^\text{ISS} \) at 2~3 times of the resonant frequency \( f_o \). The soft-start time is determined by the RC time constant:

\[ t_{\text{SS}} = 3 \sim \frac{1}{4}(R_{\text{SS}} \cdot C_{\text{SS}}) \]  

(70)

### Figure 39. Frequency Sweep of the Soft-Start
(Design Example) The minimum frequency is 75kHz in STEP-15. \( R_{\text{min}} \) is determined as:

\[
R_{\text{min}} = \frac{100kHz \times 5.2K\Omega}{f_{\text{min}}} = 6.93K\Omega
\]

Considering the output voltage overshoot during transient (10%) and the controllability of the feedback loop, the maximum frequency is set as 140kHz. \( R_{\text{max}} \) is determined as:

\[
R_{\text{max}} = \frac{4.68K\Omega}{f_{\text{o}} \times 1.40} = \frac{5.2K\Omega}{100kHz} \times \frac{5.2K\Omega}{R_{\text{min}}} = 7.88K\Omega
\]

\[
R_{\text{max}} = \frac{96kHz \times 1.40 - 5.2K\Omega}{100kHz} - \frac{2.5}{5.2K\Omega} - \frac{6.93K\Omega}{100kHz} = 38.45K\Omega
\]

Setting the initial frequency of soft-start as 250kHz (2.5 times of the resonant frequency), the soft-start resistor \( R_{SS} \) is given as:

\[
R_{SS} = \frac{5.2K\Omega}{f_{\text{o}} \times 40kHz} = \frac{5.2K\Omega}{100kHz} \times \frac{5.2K\Omega}{R_{\text{min}}} = 3.85K\Omega
\]

\[
R_{SS} = \frac{250kHz \times 40kHz - 5.2K\Omega}{100kHz} - \frac{5.2K\Omega}{6.93K\Omega} = 38.45K\Omega
\]

[STEP-20] Current Sensing and Protection

FAN7621S senses low-side MOSFET drain current as a negative voltage, as shown in Figure 40 and Figure 41. Half-wave sensing allows low power dissipation in the sensing resistor, while full-wave sensing has less switching noise in the sensing signal. Typically, an RC low-pass filter is used to filter out the switching noise in the sensing signal. The RC time constant of the low-pass filter should be 1/100~1/20 of the switching period.

![Figure 40. Half-Wave Sensing](image)

![Figure 41. Full-Wave Sensing](image)

(Design Example) Since the OCP level is determined as 2.5A in STEP-17 and the OCP threshold voltage is -0.6V, a sensing resistor of 0.24\( \Omega \) is used. The RC time constant is set to 100ns (1/100 of switching period) with 1K\( \Omega \) resistor and 100pF capacitor.

[STEP-21] Voltage and Current Feedback

Power supplies for LED lighting must be controlled by Constant Current (CC) Mode as well as a Constant Voltage (CV) Mode. Because the forward-voltage drop of LED varies with the junction temperature and the current also increases greatly consequently, devices can be damaged.

Figure 42 shows an example of a CC and CV Mode feedback circuit for single-output LED power supply. During normal operation, CC Mode is dominant and the CV control circuit does not activate as long as the feedback voltage is lower than reference voltage, which means that CV control circuit only acts as OVP for abnormal modes.

(Design Example) The output voltage \( V_o \) is 103V in design target. \( V_o \) is determined as:

\[
V_o = 2.5(1 + \frac{R_{FU}}{R_{FL}})
\]

Set the upper-side feedback resistance \( R_{FU} \) as 330K\( \Omega \). \( R_{FL} \) is determined as:

\[
R_{FL} = \frac{2.5 \times R_{FU}}{V_o - 2.5} = \frac{2.5 \times 330K\Omega}{103 - 2.5} = 8.2K\Omega
\]

The output current \( I_{\text{LED}} \) is 1.46A in design target. Assuming the sensing resistor \( R_{\text{SENSE}} \) of 0.1\( \Omega \) and feedback resistor \( R_{202} \) of 47K\( \Omega \) are used, the input resistor \( R_{203} \) is determined as:

\[
R_{203} = \frac{V_{\text{SENSE}} \times R_{202}}{0.36} = \frac{(R_{\text{SENSE}} \times I_{\text{LED}}) \times R_{202}}{0.36} = \frac{(0.1 \times 1.46) \times 47K\Omega}{0.36} = 19K\Omega
\]

![Figure 42. Example of CC and CV Feedback Circuit](image)
4. Schematic of the Evaluation Board

Figure 43. Evaluation Board Schematic
Dimensions: 240 (W) × 80 (H) [mm]

Figure 44. Top View of Evaluation Board

Figure 45. Bottom View of Evaluation Board

5. Bill of Materials

<table>
<thead>
<tr>
<th>Item No.</th>
<th>Qty</th>
<th>Reference</th>
<th>Part Reference</th>
<th>Description (Manufacturer)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>BD1</td>
<td>600V/8A</td>
<td>Bridge Diode (Fairchild Semiconductor)</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>CN1</td>
<td>3PIN</td>
<td>Connector</td>
</tr>
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<td>3</td>
<td>1</td>
<td>CP1</td>
<td>630V22nF</td>
<td>SMD Tantal Capacitor</td>
</tr>
<tr>
<td>4</td>
<td>5</td>
<td>CP2,CP6,CP13,CP21</td>
<td>33µF/25V</td>
<td>SMD Tantal Capacitor</td>
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<td>3</td>
<td>CP4,CP5,CP8</td>
<td>120µF/450V</td>
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<td>470nF/400V</td>
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<td>C2</td>
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<td>Ultra-Fast Diode</td>
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<td>F1</td>
<td>FS101</td>
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<td>J1,J6</td>
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<td>Connector</td>
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<td>10mH/2.3A</td>
<td>Common-Mode Filter</td>
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**Related Datasheets**

- **FL7930B** — Single-Stage Flyback and Boundary Mode PFC Controller for Lighting
- **FAN7621S** — Controller for Resonant Half Bridge
- **FDPF17N60NT** — 600V N-Channel MOSFET, UniFET™2
- **FDPF7N60NZ** — 600V N-Channel MOSFET, UniFET™2

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.