A Single Stage PFC+PWM Converter for 75-150 W Distributed Power Systems

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Abstract – Many distributed power architectures (DPAs) use an intermediate bus voltage of 12 V followed by a dc-dc point of load (POL) stage. With government regulations requiring front end power factor correction (PFC) in supplies of 75 W or greater, designers are faced with additional complexity. This paper describes a novel single stage flyback topology that combines PFC and power conversion stages and demonstrates its usefulness through a design example.

Introduction

Many applications in consumer, SOHO computing and networking fields, such as wireless base stations, set top boxes and high-end game boxes often use a DPA with a mid-level bus voltage of 12 V and non-isolated local dc-dc conversion subsequently. While the DPAs add a power conversion stage, they help in terms of modularity, efficiency and configurability. However, as the load voltages continue dropping, DPAs are facing fresh challenges. Using a single stage dc-dc conversion at low load voltages and high current becomes inefficient. Also adding to the system complexity, new harmonics reduction requirement EN61000-3-2 for power supplies above 75 W input power now mandates the use of a preregulator PFC at the ac-dc stage. A typical front-end power stage consists of a boost PFC preregulator creating a fixed 400 V bus and an isolated dc-dc converter producing the desired bus voltage. The resultant power system therefore involves numerous processing stages. While it may be argued that such arrangements help optimize individual power stages, there is clearly a need for more elegant system solutions.

NCP1651, a new control IC from ON Semiconductor is designed to provide such a solution. It combines the 2 stages of the front-end converter (PFC preregulator and ac-dc converter) into a single stage. It uses a flyback topology operating in continuous-conduction mode (CCM) or discontinuous-conduction mode (DCM) with average current mode control. Figure 1 illustrates the differences between a traditional 2-stage solution and the solution offered by NCP1651.

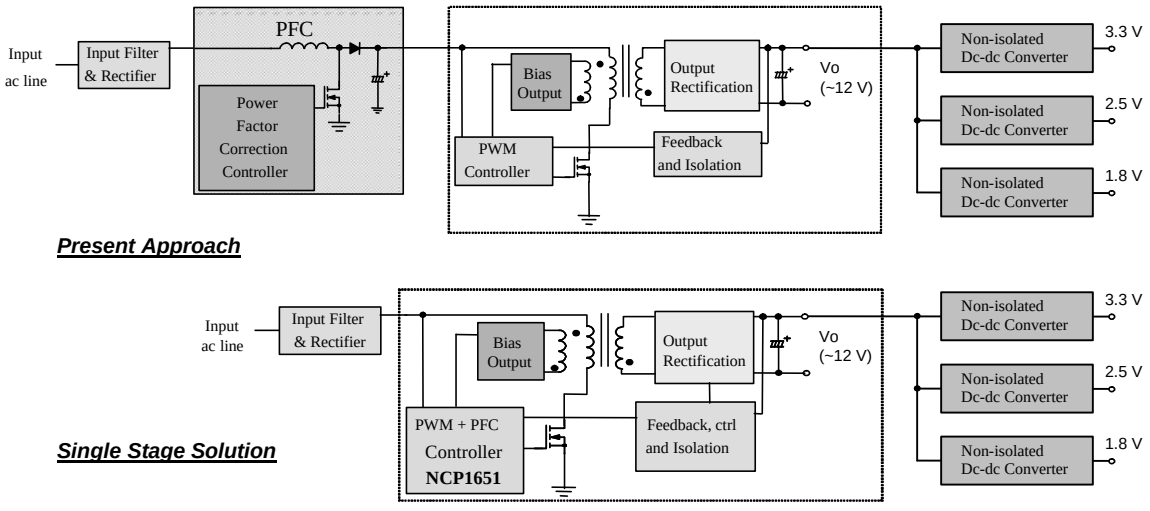

Figure 1. Architectural Advantages offered by the NCP1651 based single stage solution

As shown, this novel solution produces significant savings in component count. The NCP1651 based solution requires only one each of MOSFET, magnetic element, output rectifier (low voltage) and output capacitor (low voltage). In contrast, the 2-stage solution requires two or

more of the previous components, with at least one of the two having high voltage capability.

In terms of performance, the flyback topology operating in CCM results in very low total harmonic distortion (THD) and high efficiency. Other single-stage solutions usually force DCM operation resulting in higher peak currents and lower efficiency. Also, the offered solution operates at a fixed switching frequency leading to a much simpler design of the input filter compared to other alternatives.

NCP1651 based solutions are ideally suited for power levels below 200 W and output voltages above 12 V. To demonstrate its capability, a 120 W, 12 V converter for universal line voltage operation was designed and tested. The design is made to operate in CCM. A design aid spreadsheet was used to compute the component values and generate a bill of materials. It is downloadable from the NCP1651 product folders at:
http://www.onsemi.com/pub/Collateral/NCP1651_DESIGN-D.XLS

I. Circuit Description and Calculations

The circuit basic specifications are defined as follows. They will govern the attributes of the main circuit components, the transformer size, the selection of the MOSFET, the output rectifier and the output diode. Each will be further analyzed thereafter.

- Maximum rated output power: $Pout_{max}$ = 120 W
- Minimum operating line voltage: Vin_{min} = 85 Vac
- Maximum operating line voltage: Vin_{max} = 265 Vac
- Line frequency: f_{line} = 47 - 63 Hz
- Nominal switching frequency: f_{sw} = 100 kHz
- Nominal regulated output voltage: Vout = 12 Vdc ±10%
- System efficiency: eff. = 0.8 (expected)

Transformer

While in a 2 stage approach, the input of the dc-dc stage is regulated at 400 V, the input of the one-stage flyback is unregulated and subject to variations in the line voltage. For that reason the flyback topology is subjected to high peak currents and necessitates a rugged transformer.

The design of the transformer is done using the ON Semiconductor design aid. The primary inductance is chosen to minimize input ripple current. A higher inductance value will lower the primary peak current but favor copper losses. An inductance value of 800 uH is therefore used.

Choosing the right turns ratio is more complicated. On the one hand, using a large turns ratio means that lower power dissipation in the MOSFET and output rectifier can be achieved. A larger turns ratio allows a smaller primary current for the same load. Because power dissipation in the MOSFET is proportional to $Ip^2 \times R_{DS(on)}$, a small diminution in primary current Ip can lead to a large reduction in power dissipation. Using a larger turns ratio also lowers secondary voltage and decreases voltage stress on the boost diode during the off-state. A diode with low reverse voltage rating V_R can then be selected. This is important because lower V_R diodes have lower forward voltage drops (V_F). Diode losses being proportional to $I_F \times V_F$, it helps in minimizing the diode power dissipation.

On the other hand, using a small turns ratio has numerous advantages, the obvious being transformer size and cost. Second, having a small turns ratio means that only a small portion of the output voltage is being reflected back to the primary. In addition, the primary leakage inductance grows with the turns ratio and increases the magnitude of voltage ringing on the drain of the MOSFET. Because the power MOSFET is subjected to the rectified input voltage plus the reflected voltage and leakage spikes, it is recommended that the turns ratio be kept small. For the same reason, it is important to specify to the transformer manufacturer to minimize the primary leakage inductance.

A first approximation of the transformer turns ratio can be obtained from Figure 2. It expresses the maximum expected drain-to-source voltage (V_{DS}) of the power MOSFET and secondary voltage according to the transformer turns ratio.

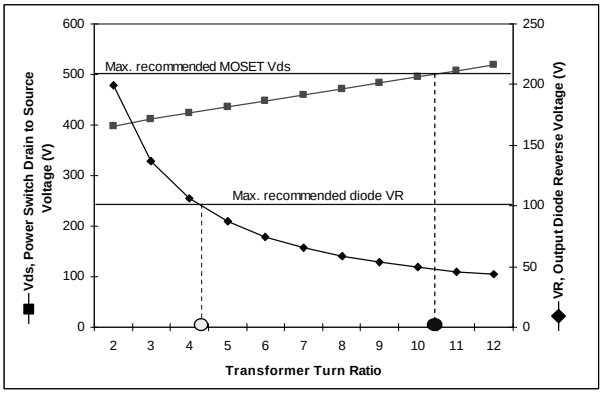

Figure 2. V_{DS} and V_R vs. transformer turns ratio (12 V output)

○ Indicates the minimum recommended turn ratio
● Indicates the maximum recommended turn ratio

The turns ratio is selected to keep the drain-to-source voltage to a reasonable level. A lower V_{DS} allows to select a MOSFET with a lower $R_{DS(on)}$, and therefore lower conduction losses. The expected V_{DS} shown in Figure 2 does not include the leakage inductance contribution. To keep some level of safety margin it is recommended to select a turns ratio yielding a V_{DS} inferior to 500 V. This design uses a 800 V MOSFET allowing for 300 V of margin while maintaining a low $R_{DS(on)}$. If the MOSFET voltage ringing is more pronounced, a snubber will be necessary to protect the switch at the detriment of efficiency as the snubber dissipates heat while absorbing the voltage spikes.

Turns ratio is also selected to achieve the lowest V_R possible. It is recommended to pick a turns ratio producing a V_R lower than 100 V.

In summary, some tradeoffs are necessary in picking the magnetics. Either the design is optimized to reduce power losses in the MOSFET and in output diode or, to lower voltage stress on the MOSFET and losses in the transformer and snubber. Choosing the right ratio has a lot to do with the available offering of MOSFETs and rectifiers and their electrical characteristics.

Power Switch

The power MOSFET selection is based on the maximum drain-to-source voltage, and maximum peak current I_{pk}. V_{DS} is determined by the rectified input voltage plus the reflected output voltage and leakage inductance voltage.

$$V_{DS} = \sqrt{2} \times Vin_{max} + \frac{Np}{Ns} \times Vout + I_p \times \sqrt{\frac{L_p(leakage)}{C_p + C_{oss}}}$$

where $\frac{Np}{Ns}$ is the primary to secondary turns ratio, I_p is the primary current, L_p(leakage) is the primary winding leakage inductance, C_p is the primary winding parasitic capacitance (1.0 nF in this example), and C_{oss} is the MOSFET output capacitance (800 pF in this example).

The maximum switch current is the same as the primary winding peak current. It is a function of the maximum line current and the allowable ripple current. It can be approximated with the following equation, or by using the design aid.

$$Ipk = \frac{\sqrt{2} \times Pin \times T}{Vin_{min} \times t_{on}} + \frac{2 \times \sqrt{2} \times Vin_{min} \times t_{on}}{Lp}$$

where L_p is the primary winding inductance and t_{on} is the power MOSFET on time.

The highest peak current will occur at low line and high load. Figure 3 shows the different currents flowing through the transformer. The minimum and maximum currents of the line current waveform are represented by the pedestal current, I_{ped}, and the peak current, I_{pk} respectively.

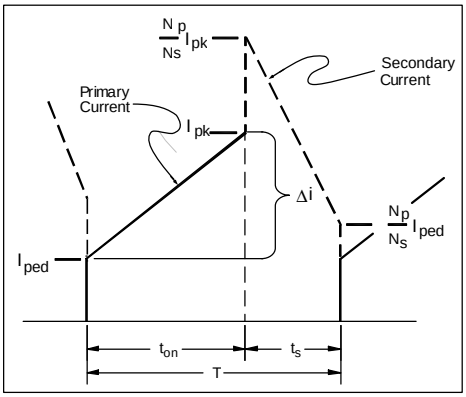

Figure 3. Primary and secondary currents of the flyback transformer

Output Rectifier

The output rectifier must be selected to minimize power losses and maximize efficiency. The most important parameters to consider are the diode forward current, I_F, forward voltage, V_F, and the reverse voltage, V_R. The diode must be able to sustain the high currents necessary to supply the load and withstand the high reverse voltage, making the device type selection (Schottky vs. ultrafast) very important. I_F should be at least equal to the average output current, and V_R should be greater than the sum of the output voltage plus the input voltage reflected to the secondary.

$$V_R = Vout + \sqrt{2} \times Vin_{max} \times \frac{Ns}{Np}$$

Conduction losses in the output rectifier can be calculated with the design aid or with the formula below.

$$Pd = V_F \times I_F \times (1 - D) \text{ with } I_F = \frac{(I_{pk} + I_{ped})}{2} \times \frac{Np}{Ns}$$

For Schottky rectifiers, conduction losses dominate the power dissipation.

Output Capacitor

One of the trade-offs made in achieving this level of input performance and system cost savings is in the output voltage characteristics. The flyback converter has no intermediate energy storage, so the output capacitor serves dual functions: energy storage capacitor for line frequency and filtering capacitor for switching frequency ripple. This results in a bulk capacitor substantially bigger than usual, to insure that ripple voltage remains low and that hold-up times are met during brown out conditions.

The output capacitor is picked based on its capacitance value, voltage and rms current ratings. The capacitance value depends on the level of output voltage ripple desired. It has two components, one due to the line frequency, the other due to the switching. Both can be calculated with the design aid. Output ripple levels of ±5% or less are acceptable. That is, less than ±600 mV for this design. The voltage rating is dictated by the output voltage of the circuit plus the output ripple voltage.

Like in any flyback converter, the output capacitor is subjected to the high switching currents present in the circuit. Those high ripple currents can not only add some voltage ripple to the output due to the ESR of the capacitor, but also damage the capacitor if not selected properly. Therefore, the rms current rating of the capacitor must be chosen accordingly.

Two 16 V, 15,000 uF large can aluminum electrolytic capacitors mounted in parallel with two 16 V, 680 uF surface mount electrolytics are used for this design. This rather odd assortment makes for a fairly compact capacitor bank. The amount of capacitance may appear excessive but it is necessary to meet the output ripple voltage requirements and to handle the low-frequency high ripple current (21 A peak). By paralleling two types of capacitors, not only is the ESR reduced, but the rms current is also divided up between them. The capacitor's ESRs are such that the low frequency current ripple is mostly directed through the heavy duty 15,000 uF capacitors which have the lowest impedance and the highest current rating. Even though the 680 uF have a lower current rating, their maximum ripple current capability is not exceeded due to the sharing of the load. With this combination of capacitors, a 120 Hz voltage ripple of 2.03 Vpp at high line is attained. If achieving a lower ripple level is a concern, additional output capacitance can be added.

II. Circuit Schematic

Following is a functional schematic of the NCP1651 PFC implementation.

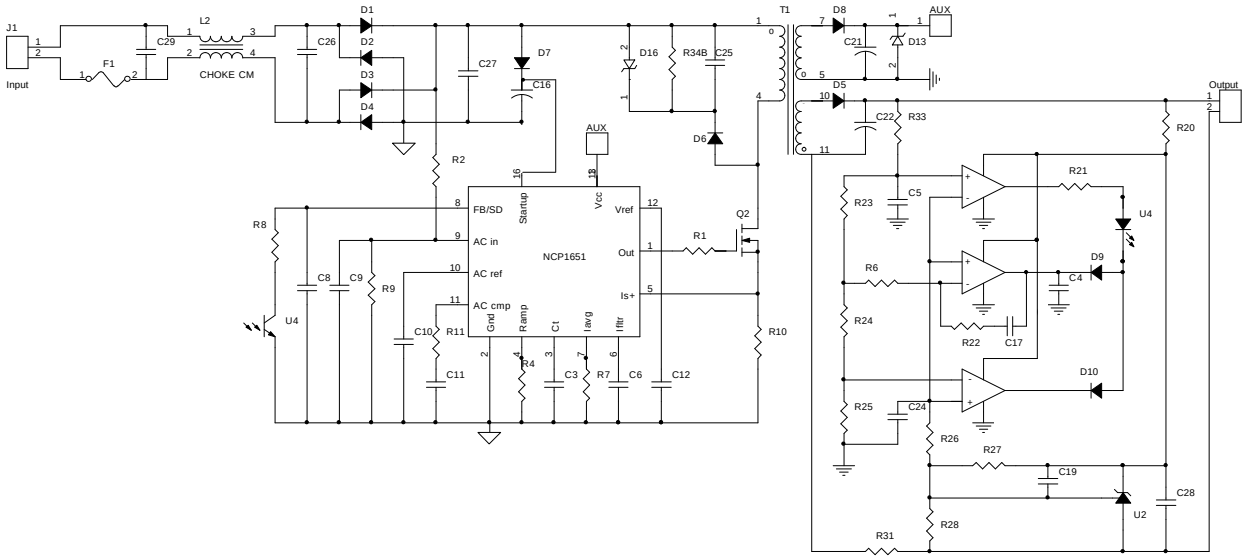

Figure 4. Simplified NCP1651 one stage flyback power factor converter schematic

III. NCP1651 Results

The measurements on the NCP1651 board were performed and the results are summarized in Table 1. These results compare very favorably to good two-stage solutions.

Table 1. NCP1651 PFC circuit results

Vin (Vac)	85	115	230	265
Vout (V)	11.72	11.78	11.77	11.78
Iout (A)	10	10	10	10
Efficiency (%)	76.2	80.7	84.0	84.0
PF (%)	99.79	99.86	96.70	93.87
THD (%)	4.76	4.29	6.40	7.90

Table 1 shows that good efficiency can be expected from the NCP1651 at input voltages of 115 Vac and above. Efficiency suffers at low line voltage where the line current increases causing higher power dissipation in the MOSFET and output rectifier. On the other hand, very good power factor (PF) and THD performance are observed at all input voltages. A slight decrease in PF and THD performance is observed at 265 Vac as the circuit alternates between DCM and CCM depending on where the input is on the rectified sinewave. DCM occurs near the zero crossing while CCM is maintained throughout the rest of the cycle period.

It is also interesting to vary the load and observe its effects on efficiency, power factor, and THD. The following three plots illustrate the results.

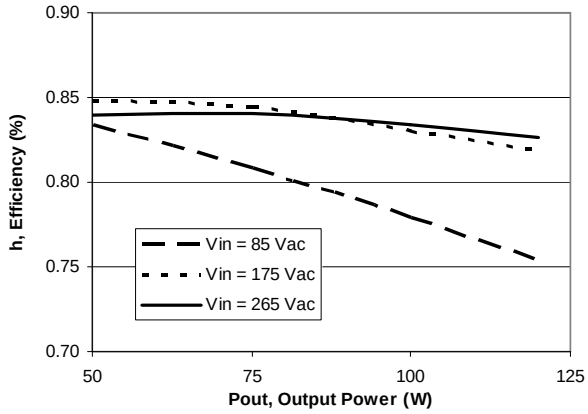

Figure 5. Efficiency vs. output power

As Figure 5 indicates, the higher the line input voltage, the higher the efficiency. At higher line voltage, the input current needed to sustain the load is lower and less power is dissipated in the various components, leading to a more efficient circuit. Efficiency is typically lower at higher loads where the line current is greater and the power dissipation in the MOSFET and output rectifier is higher.

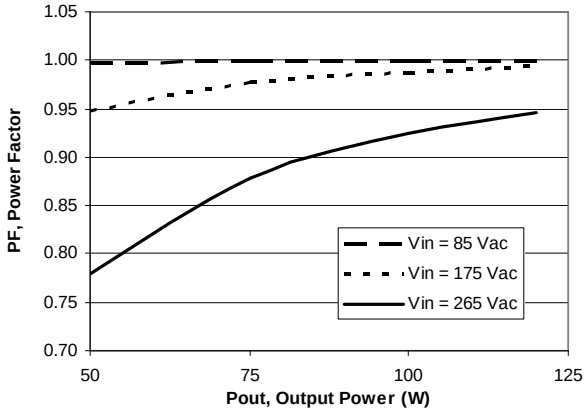

Figure 6. Power factor vs. output power

As Figure 6 attests, power factor improves as the output power increases. At lower power levels and high line (175 Vac and 265 Vac), the circuit operates in DCM. DCM operation forces faster di/dt and higher peak currents in the power switch and output rectifier. The higher the line voltage and the lower the output power, the shorter the power switch on time becomes and the more the power factor level suffers as a result. At low input line voltage, the device operates in CCM whatever the output power and distortion does not become an issue. Selecting a higher primary inductance would extend the range over which the circuit runs in CCM and help improve the power factor.

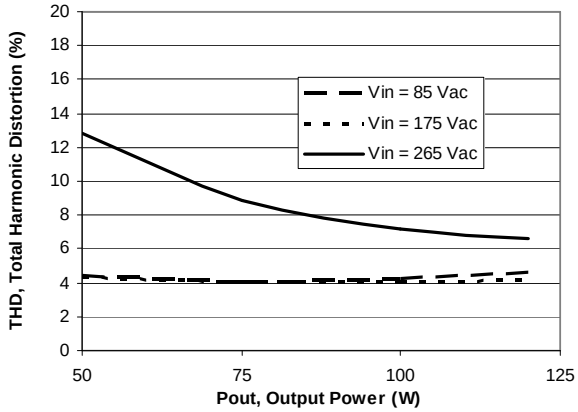

Figure 7. THD vs. output power

As seen on Figure 7, similarly to the power factor, THD is higher at high line for low output powers. Again, this is because the controller

operates in DCM which results in higher current ripple. The high ripple of the input current waveform is harder to filter in the EMI filter. In contrast, at high line high output power, THD levels are much lower because the controller is working in CCM. Using more primary inductance would help maintain CCM operation longer. It may however go against satisfying some of the design constraints.

Trend chart

The detail of the work presented is centered at 120 W. Table 8 provides projected values for each of the design attributes for different power levels. Efficiency and cost assumptions can be derived consequently.

The following assumptions were made. The value of C_{out} is based on 30% output voltage ripple and 20 ms holdup time. Because the transformer design is rather iterative, it was optimized for low power dissipation in the various components, and to ease components selection based on the circuit electrical characteristics.

Table 8. Trend chart for the single stage flyback

	T1		C_{out}		MOSFET		D_{out}	
P_{out} (W)	L_p[3] (uH)	Np/ Ns	I_{ripple} (A)	C_{out}[2] (uF)	V_{DS}[1] (V)	I_{DS}pk (A)	V_R[1] (V)	$I_F$pk (A)
100	800	9	19.8	31,360	800	4.75	80	42.7
150	800	5	22.0	31,360	800	9.62	100	48.1
200	800	3	22.8	31,360	800	18.22	150	54.6

Notes: 1. Values indicated are actual electrical rating of the device recommended for the design.

2. C_{out} is the amount of capacitance necessary to meet the ±10% output voltage ripple requirement and the capacitor ripple current. If low capacitance value with high ripple current rating capacitors were available, smaller capacitors could have been used.

3. Changing the primary inductance value does not greatly affect the design parameters therefore a value of 800 uH was used throughout. A higher inductance value would help lower the MOSFET peak current however a very large amount of inductance is needed to lower the ripple current by only a few mA. Additional cost spent on magnetics is not worth the slight improvement in current ripple.

Table 8 covers a rather narrow output power range of 100 W – 200 W. Because of the low output voltage of 12 V, it is very hard to accommodate higher output powers for this particular type of topology. Higher power level means higher peak currents in the circuit, putting extra stress on the various components and drastically increasing power losses. At 200 W, the transformer turns ratio has to be kept low in order to keep the output capacitor current ripple to a manageable level. However, this causes a higher peak current in the transformer, MOSFET, and output rectifier. It also increases the reverse voltage of the boost diode, requiring a device with a larger V_F.

It is however possible to attain higher levels of output power at higher output voltages while keeping the components to reasonable sizes. For example, a 200 W / 24 V circuit with a 800 uH primary inductance, 5 turns ratio transformer would exhibit a 495 V drain-to-source voltage, a 8.70 A MOSFET peak current, a 99 V boost diode reverse voltage with a 43.5 A peak current, and a 20.82 A output capacitor ripple current. These numbers are more manageable than the ones displayed in Table 8, and good circuit performance can be expected as a result.

Conclusion

As described in this paper, the regulatory and end applications requirements are creating new challenges for distributed power solutions. Variations in the architectures to address the specific needs of the application and the market are evolving. One of the biggest challenges identified is the minimization of power conversion stages while maintaining the overall system efficiency and performance. This article introduced the single stage flyback PFC as one such scheme and demonstrated the results to show its effectiveness.

References

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