IMPACT OF IC TECHNOLOGY ON THE POWER PROCESSING INDUSTRY

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Dhaval Dalal
Technical Marketing Director

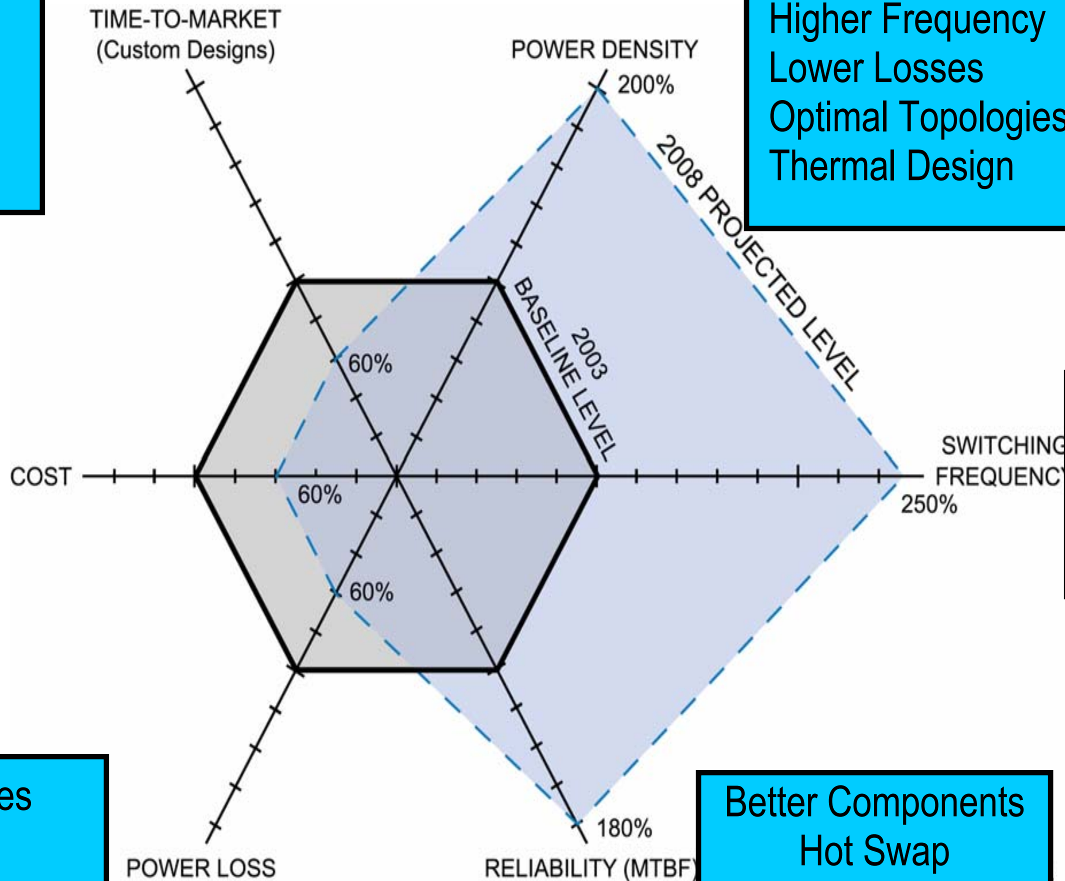
Brant Johnson
Senior Systems Engineer

PSMA Perspective - 5 Year Roadmap

Integration
Design Software
Models
Kit Solutions
Technical Support

More Integration
Higher Frequency
Lower Losses
Optimal Topologies
Thermal Design

Better Components
ICs
Power Semi's



Optimal Topologies
Better Components
ICs
Power Semi's

More Integration
Better/Cost Effective
Components
(ICs, Power Semi's)
Optimal Topologies

Optimal Topologies
Better ICs &
Power Semiconductors

Better Components
Hot Swap
Infrastructure

What drives the PSMA requirements and how do we satisfy them?

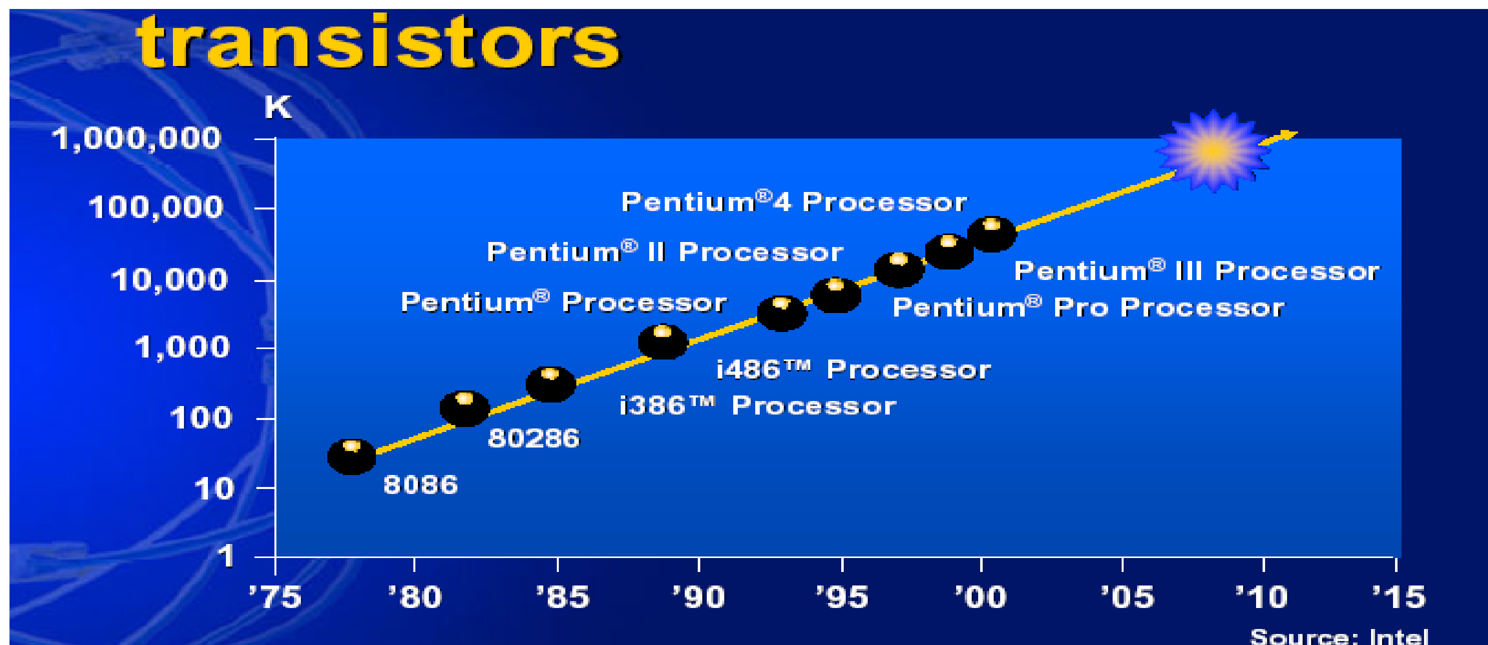
How is IC technology evolving?

What will this progress mean to the power industry?

How IC technology itself provides solutions to the problems we face.

Examples of how IC technologies are enablers for power solutions.

Moore's Law in Action



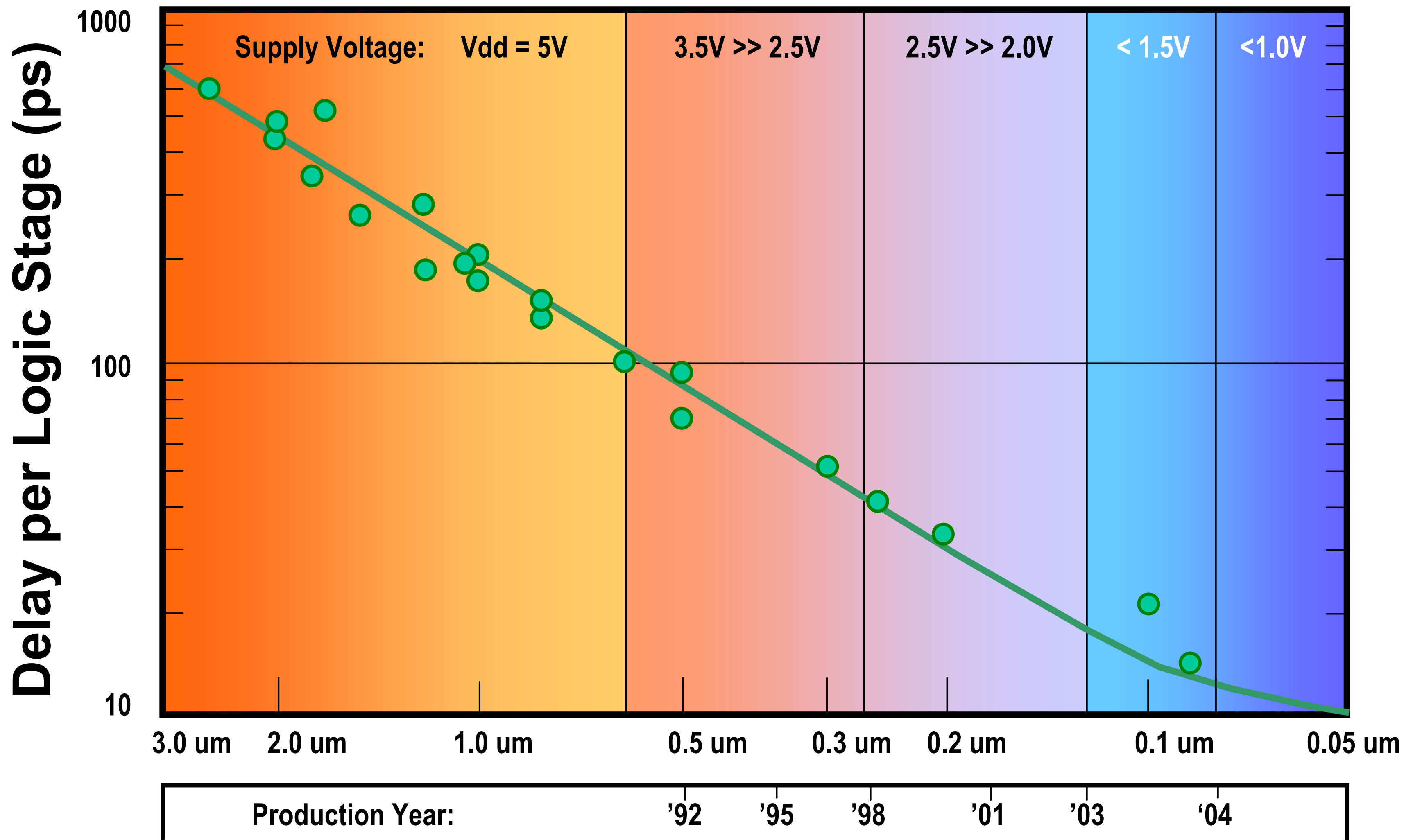
From Intel Technology Symposium September 2003

IC technology progress will enable Intel to build processors with more than a billion transistors, running at about 20 GHz by 2010.

IC Technology - *Challenges to Overcome*

- As Gate lengths continue to shrink, Gate leakage becomes excessive. SiO_2 limit ~ 23 Angstroms
- Using higher K dielectrics (SiO_2 = 4.5) required for thicker gate Tox
- Short channel lengths require shallower SD junctions. Higher doping required to maintain low resistance.
- Limits approached as devices approach atomic dimensions.

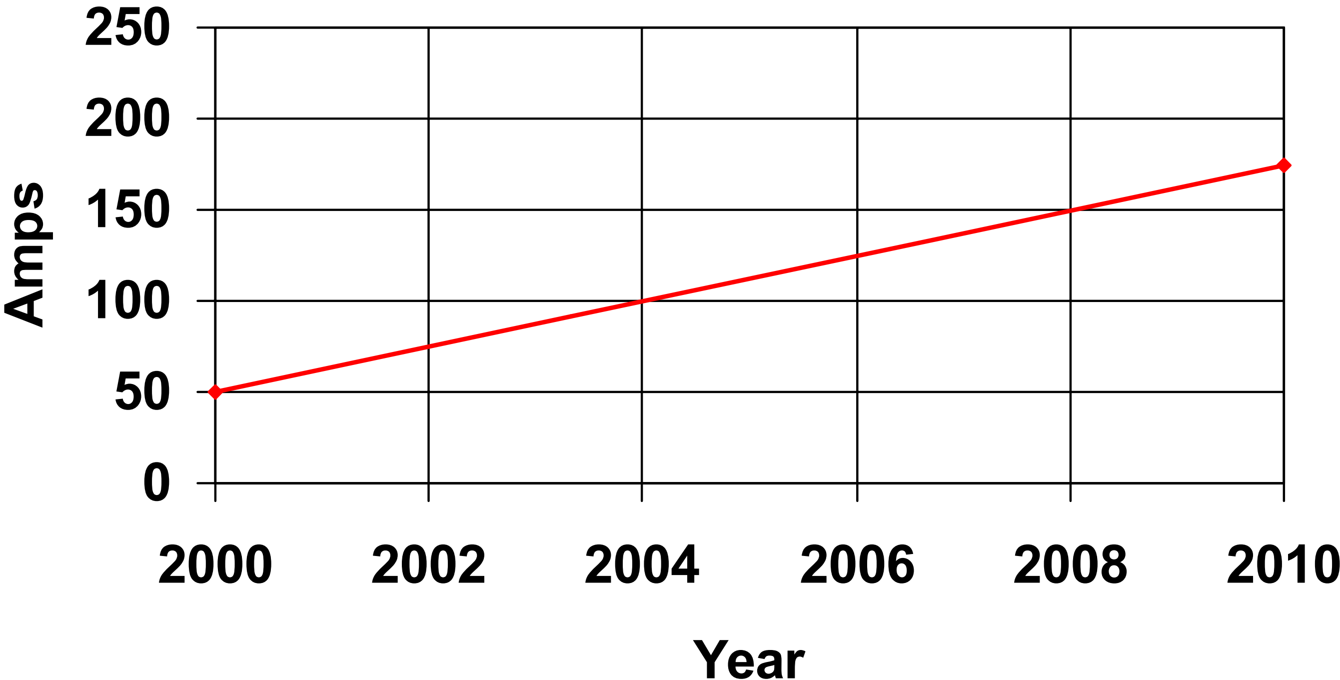
Digital CMOS Technology Migration



BY 2008, Vcc will fall from 1.3 to 0.8 volts and Icc will rise to 150 amps.

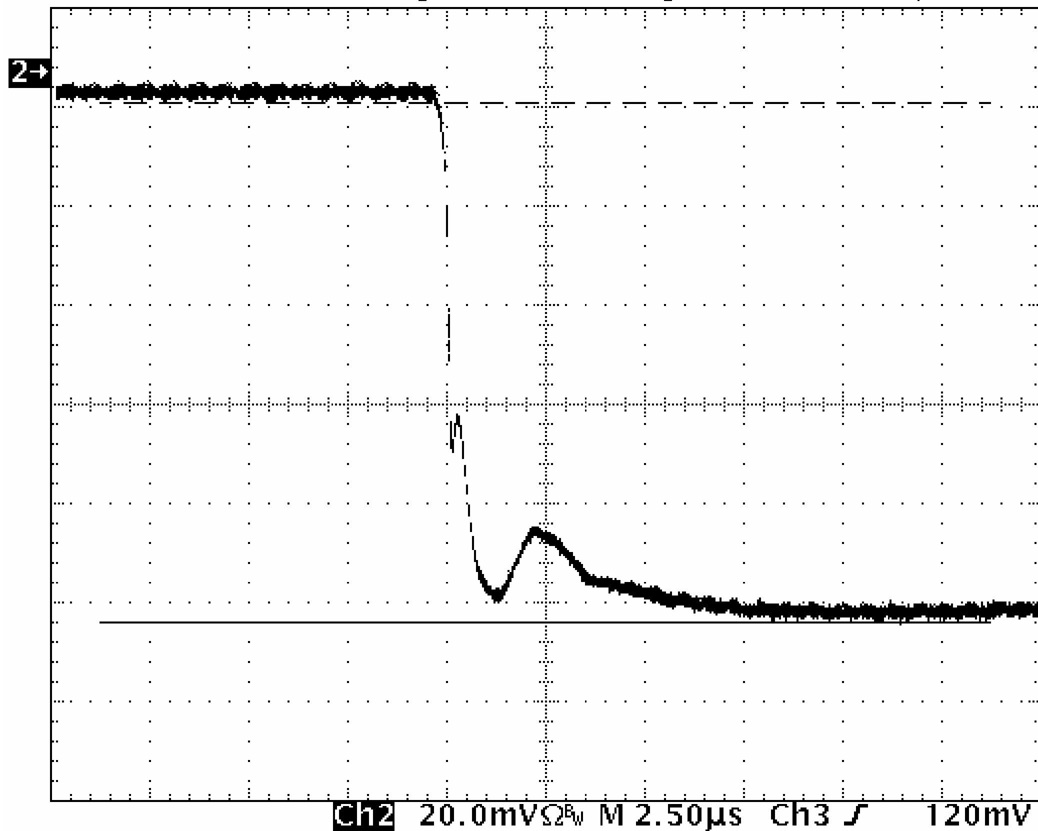
Load slew rates will dictate higher controller bandwidth & lower Zout

Desktop CPU Current Trend



Data from ITRS (International Technology Roadmap for Semiconductors)

60 Amp Transient Load Step

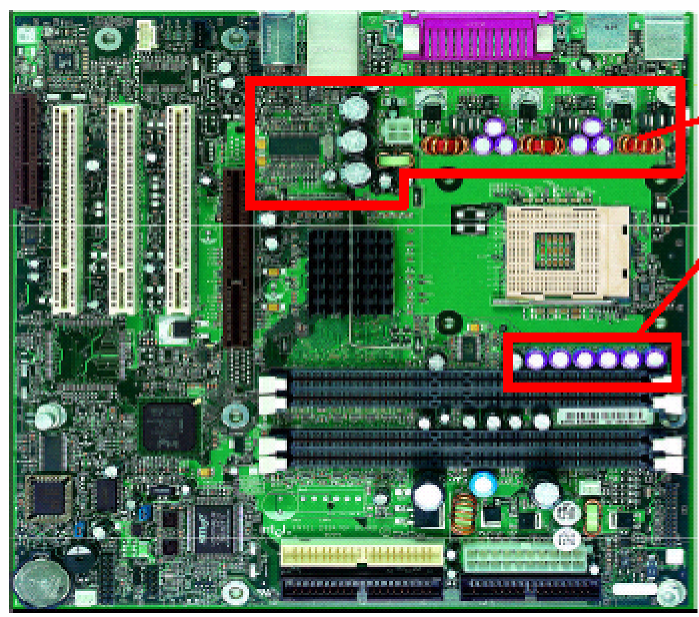


Step load from 10 to 70 amps

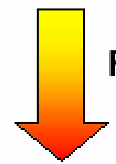
Load slew rate is approximately 150 amps / us

Three phase controller solution from Fred Lee's "High frequency solutions for 12 volt VR" CPES September, 2003

MB for Pentium IV uP



Today: 1.3V/70A
12% area of MB



Following Today's Approach

Future: 0.8V/150A
30% area of MB!!!

- ***New circuit techniques required as part of future solutions***

Power Industry Challenges

- Increased current requirements at ever lower voltages

  New power devices required

- Increased load transients caused by faster switching components.

  Faster power switching required

- Current circuit approaches untenable due space constraints

  New more space efficient circuit topology required.

Power solutions from this technology

- **Shorter channel lengths lead to:**
  - Improved $R_{DS(on)}$ cm^2
  - Improved cells per cm^2
- **Single and dual Resurf from improved process control drive:**
  - Higher voltage, higher cell density power devices
- **Copper metallization**
  - Lower thermal resistance
  - Lower parasitic resistance
- **Leadless packaging**
  - Improved thermal resistance

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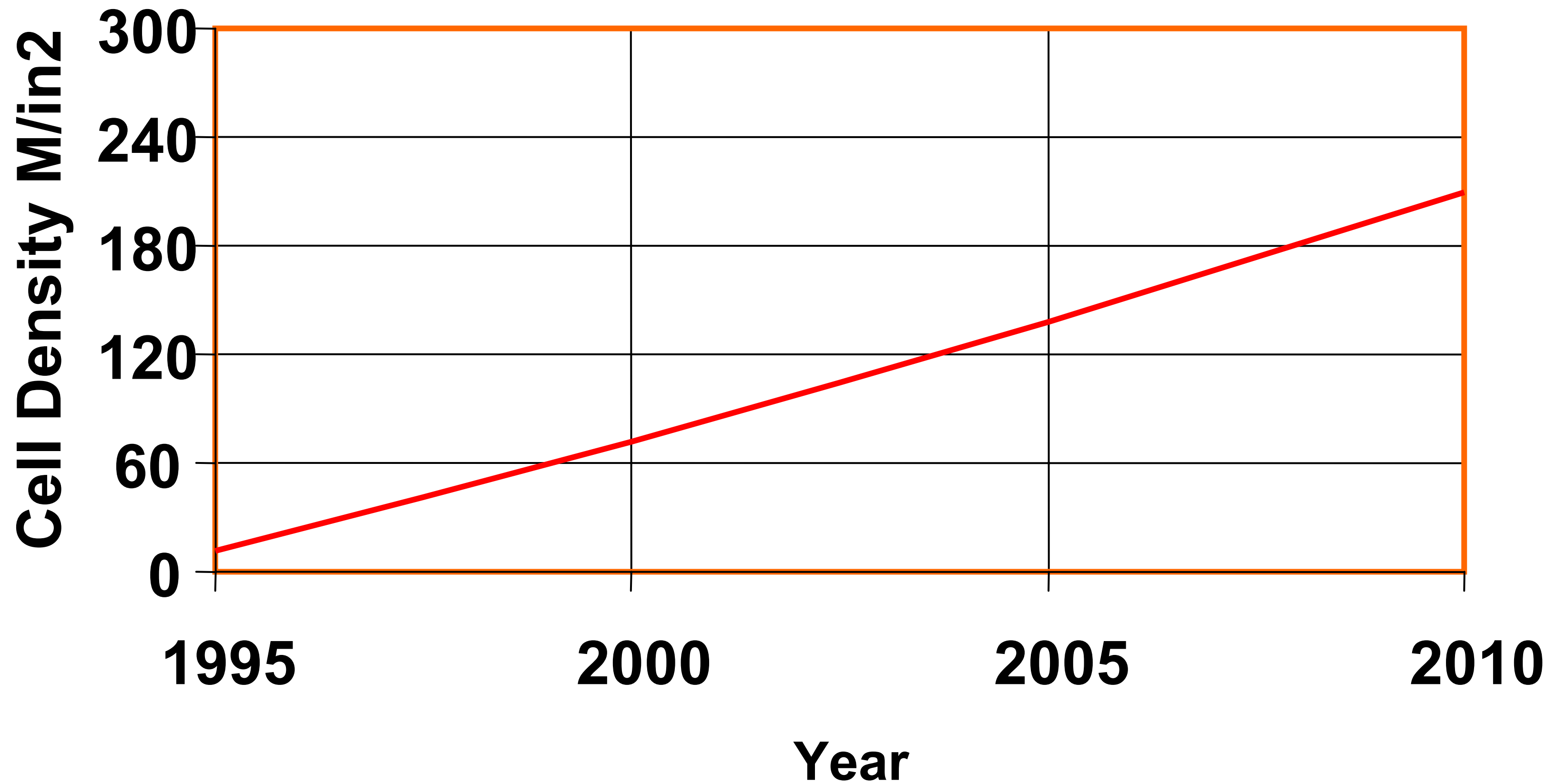
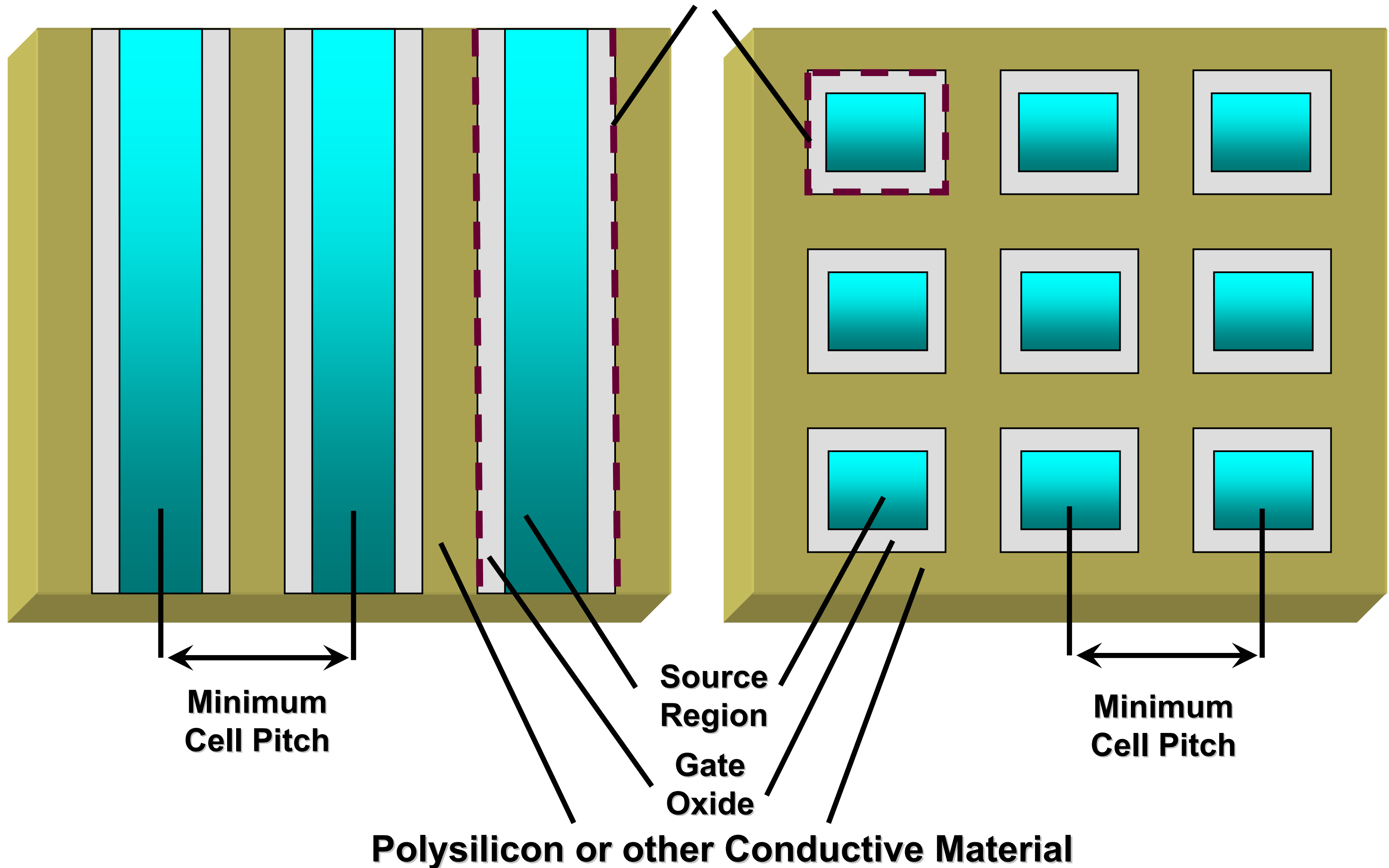
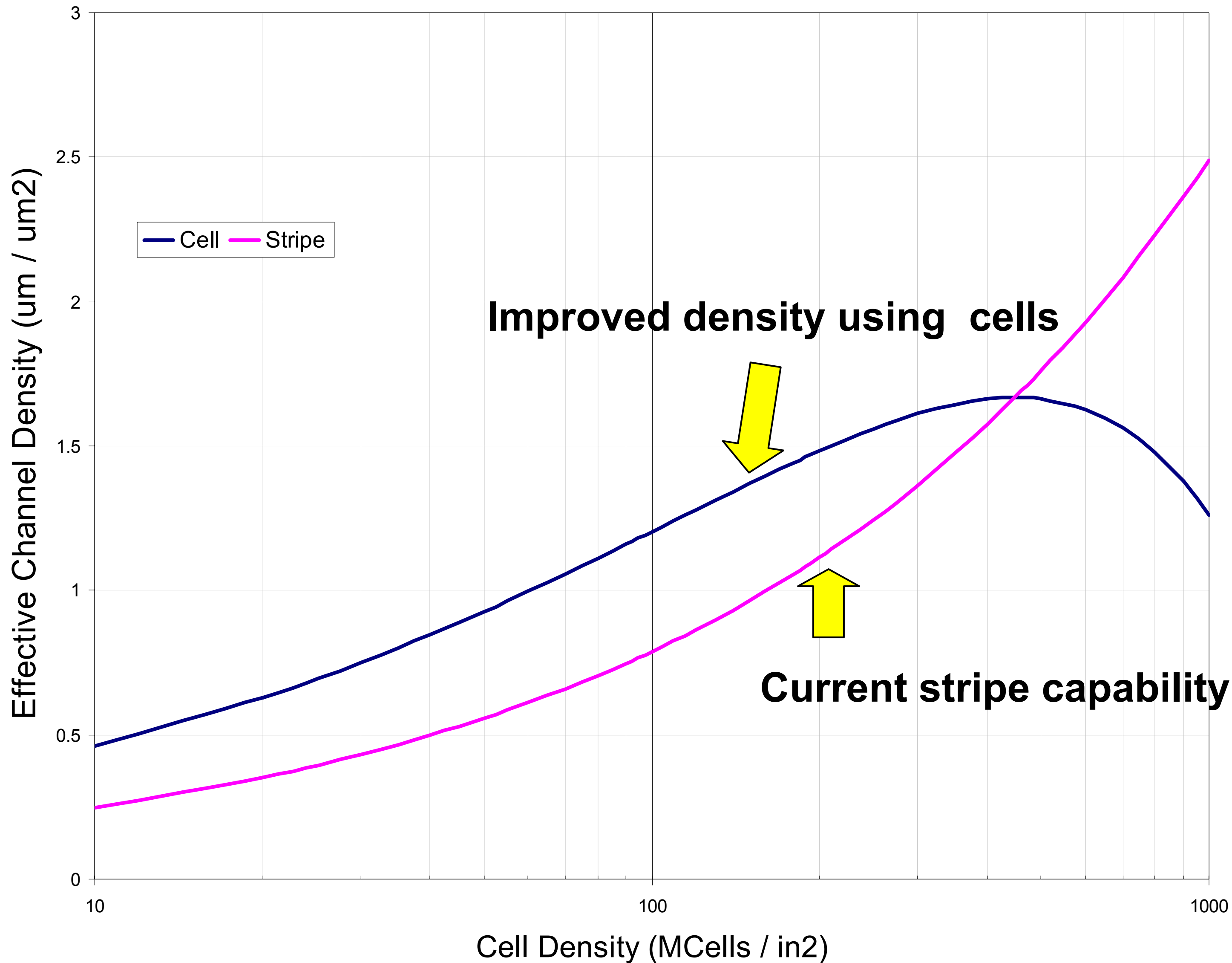
Projected Power MOS Cell Density



Current Conduction Channel Forms along the Gate Oxide Periphery

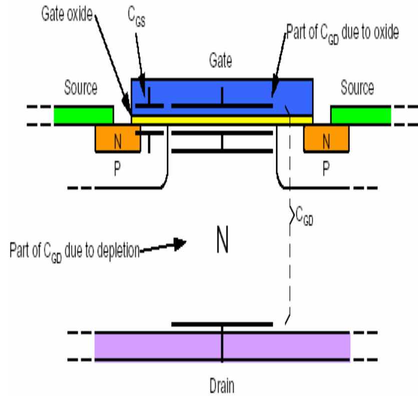


50% packing density improvement from strip to cell topology



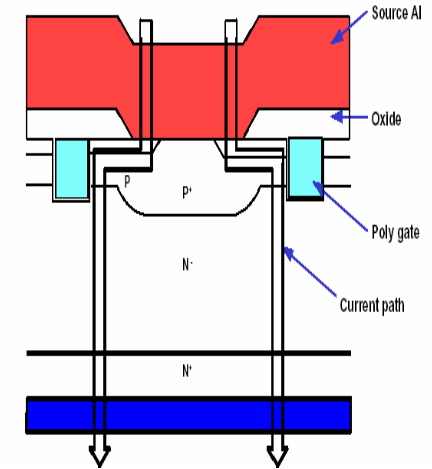
Effective Channel Density (um / um2)
Cell Density (MCells / in2)
Cell
Stripe
Improved density using cells
Current stripe capability
0
0.5
1
1.5
2
2.5
3
10
100
1000

Comparison of Trench and DMOS Structures

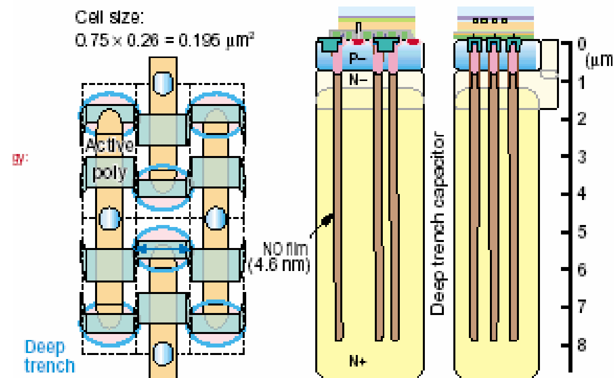


DMOS Structure

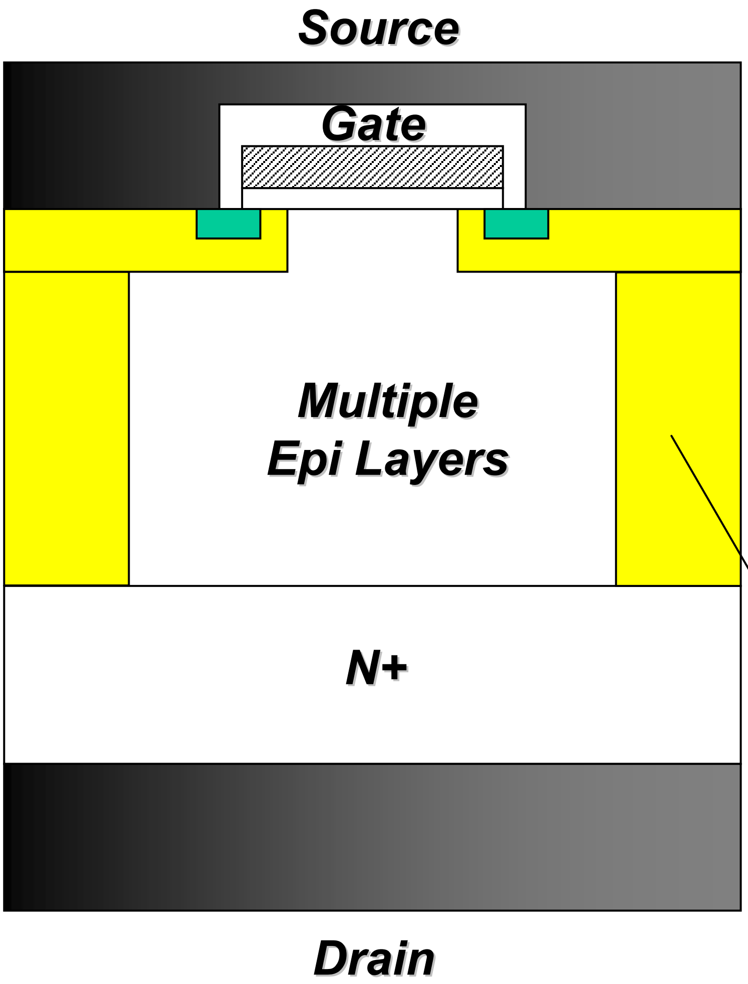
- **Trench solves JFET issue**
- **proves higher cell density**



Trench Structure



■ Figure 4 DRAM Structure



Existing Technology

Multiple Epi layers

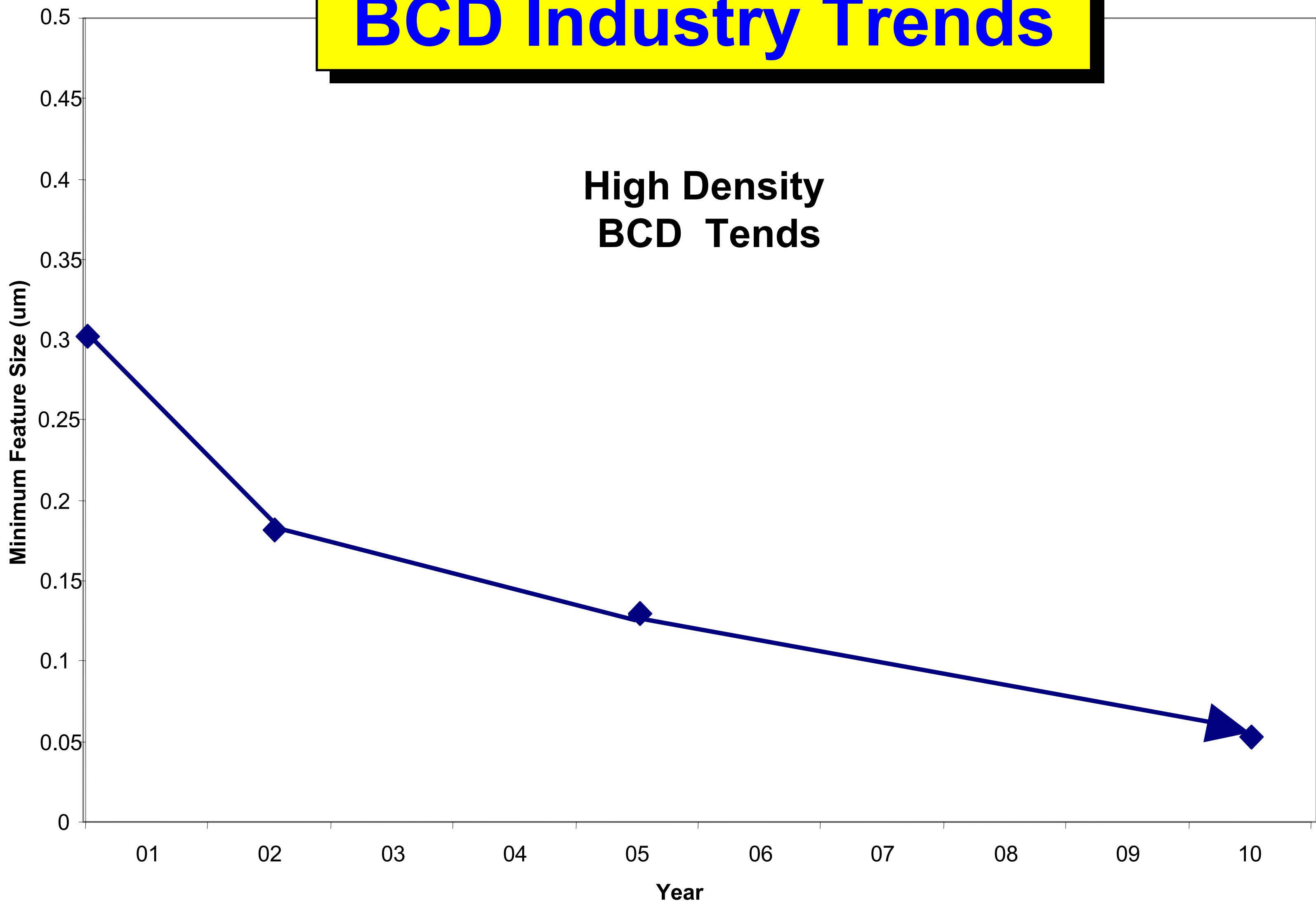
Multiple P implants

Future Technology

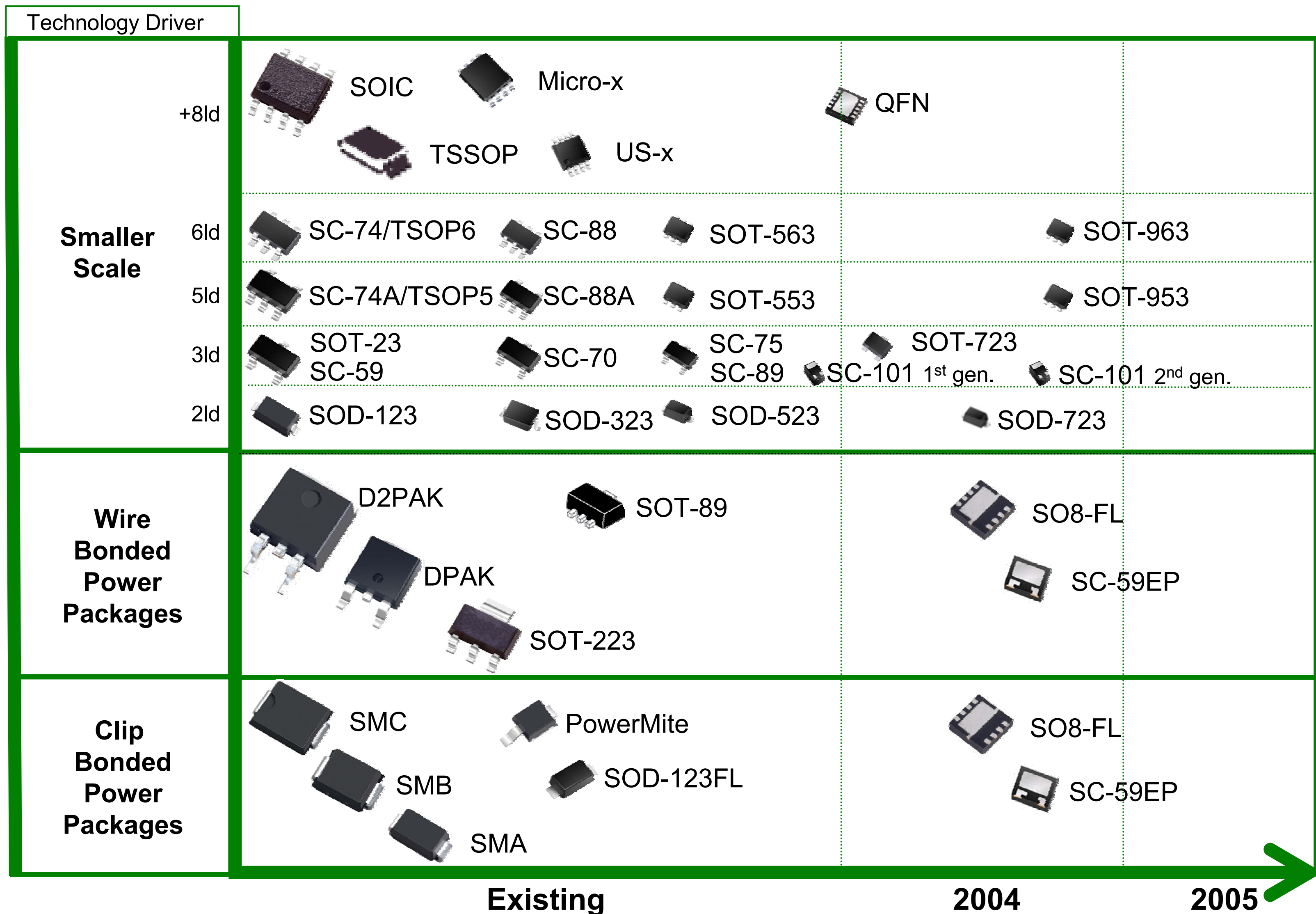
Trench generated P regions and single Epi layer to provide die size improvement

P Regions shape space charge widening and allows device to be smaller

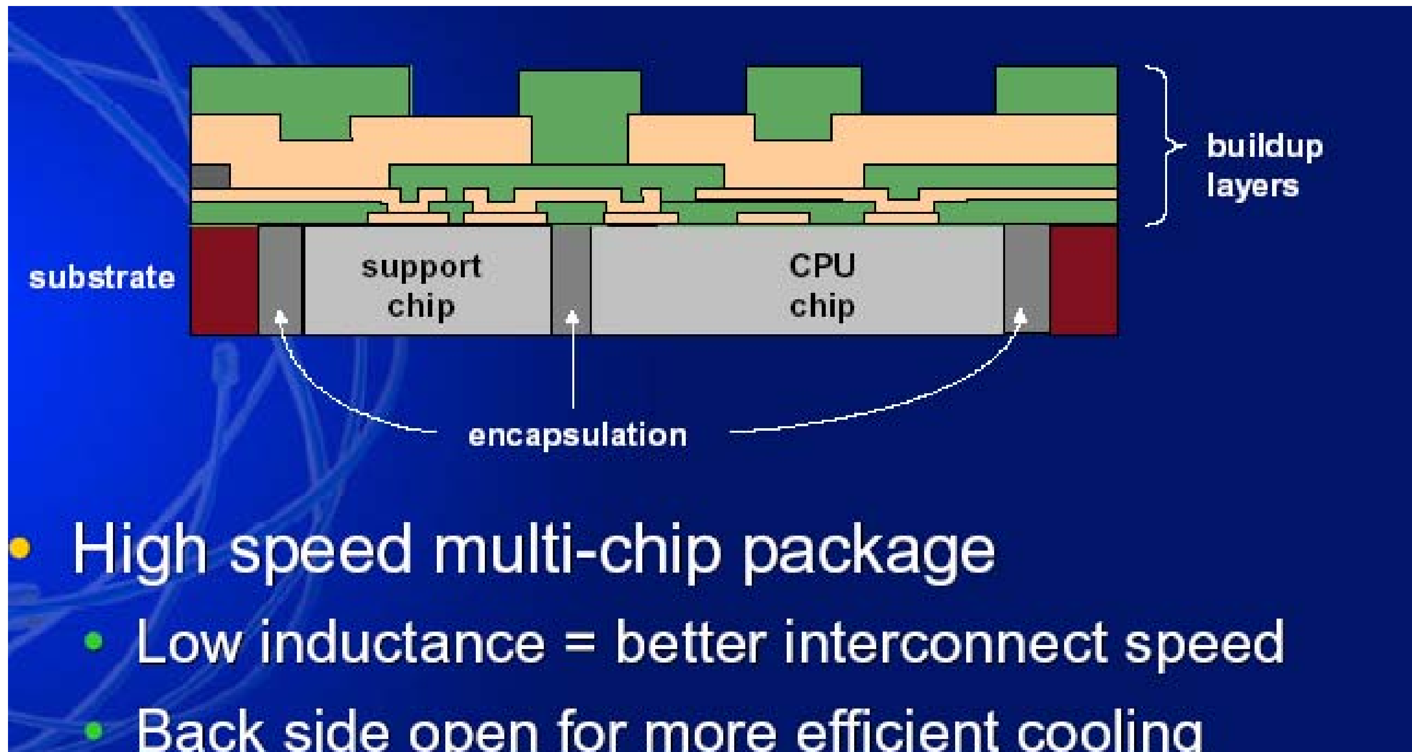
BCD Industry Trends



Packaging Technology…



Fully integrated IC and Power delivery System



From Intel Technology Symposium September 2003

High Power Notebook Adapter with PFC

- Today’s mainstream power solutions are dominated by “ugly” passives (cost driven)
- Challenge for semiconductor vendors is to reduce the passive real estate with “smarter” semiconductor solution kits – need optimum partitioning, advanced technologies

Power Trends Summary

- Insatiable demand for increased power density will drive innovative power designs to deliver
  - higher efficiency solutions.
  - low inductance thermally superior packaging.

- Higher frequency solutions will require higher levels of integration in lower inductance packages.