Product Overview

XPressArray®-II: 0.15μm Structured ASIC

Product Description

Targeted at medium-density, high-speed, 1.5V ASIC applications and high-density FPGA-to-ASIC conversions, the XPressArray-II (XPA-II) 0.15μm structured ASIC is an innovative next-generation technology platform that reduces time-to-market for system-on-chip (SoC) applications.

XPA-II offers a true drop-in replacement for Xilinx Virtex-II and Virtex-II Pro and Altera APEX-II and Stratix FPGAs, making it the industry’s lowest cost ASIC conversion solution. The result is a simplified route to cost reductions for OEMs looking to combine the flexibility of FPGA prototyping with a path to ASICs for final production.

Operating with system clock speeds up to 210MHz for 18x18 soft multipliers and available in a variety of package options, XPA-II 0.15μm devices deliver high performance, low power ASIC solutions with densities to 4.8M ASIC gates.

Configurable memory ranges from 258Kbits to 4.8Mbits, which increases up to 6.1Mbits of memory with the addition of distributed configurable memory, assuming 50 percent of the logic sites are used for memory.

Flexible I/O technology includes support for a comprehensive array of common standards and compatibility with 1.5V, 1.8V, 2.5V, and 3.3V I/O schemes. I/Os support DCI on-chip termination. DDR support for high-speed memory interface is built-in. High fault coverage is provided through integrated scan-test, memory BIST and JTAG support.

For FPGA conversions, rapid access to XPressArray (XPA) technology can be achieved via NETRANS™ FPGA-to-ASIC design flow from ON Semiconductor. Alternatively, the availability of XPA synthesis libraries for leading commercial synthesizers allows conversion of FPGA designs to ASICs by simply re-targeting from an FPGA library to an XPA library.

Features

- Next-generation 0.15μm structured ASIC platform for high performance 1.5V ASICs and FPGA-to-ASIC conversions
- Drop-in replacement for cost-reducing Xilinx® Virtex™-II and Virtex-II Pro and Altera® APEX-II and Stratix designs
- 511K to 4.8M ASIC gates
- System clock speeds up to 210MHz
- Low power consumption
  - 0.055μW/MHz/gate @ 1.575V
- 258Kbits to 4.8Mbits of block RAM memory
- 18Kbit initializable dual-port RAM blocks
- Up to 6.1Mbits of memory when 50 percent of the logic sites are used for distributed memory
- Initializable distributed memory
- Flexible I/O technology, any I/O standard assigned to any I/O pin
- Configurable signal, core and I/O power supply pin locations
- Supports LVTTL, LVCMOS, PCI33, PCI66, PCI-X 133, PCI-X 2.0, GTL+, HSTL class 1, 2, 3, and 4, SSTL2 class 1 and 2, LVPECL (input), and LVDS I/O standards
- 1.5V, 1.8V, 2.5V, and 3.3V capable I/O
- True 3.3V tolerance with no external resistor necessary
- Digital controlled impedance (DCI)
- Built-in dual data rate (DDR) support
- LVDS data rates to 622MB
- Up to 1360 user I/Os
- Comprehensive clock management cuitry
- Up to eight delay-locked loops (DLLs) and eight phase-locked loops (PLLs)
- Variety of package options
- Integrated high-fault coverage scan-test, memory BIST and JTAG
Product Overview - continued

**XPressArray®-II: 0.15μm Structured ASIC**

**Technology**

XPA-II technology is ideal for medium density ASIC applications requiring high performance and low power, with 1.5V operation. XPA-II devices are fabricated using a hybrid technology that integrates an established 0.15μm front-end process with a proven ON Semiconductor metal finishing technology, which is used to produce a customized back-end. The 0.15μm processing steps are common to multiple applications, reducing costs by allowing existing tooling to be utilized. At the same time, tooling and manufacturing costs are significantly lower for the metal finishing process than for traditional 0.15μm cell-based processes. The result is that XPA-II delivers reduced cycle times and significant reductions in terms of both NRE and unit cost through manufacturing utilizing structured ASIC technology.

There are nine bases in the ON Semiconductor XPA-II family. These bases offer between 511K and 4.8M gates and up to 4.8Mbits of block RAM. RAM may be configured as single or dual port with asymmetrical port widths. The architecture also supports RAM initialization. Flexible I/O technology includes fully configurable core and I/O power supply pads and support for one of the industry’s widest ranges of I/O standards including LVTTTL, LVCMOS, PCI33, PCI66, PCI-X 133, PCI-X 2.0, GTL+, HSTL class 1, 2, 3, and 4, SSTL2 class 1 and 2, LVPECL input, and LVDS. Comprehensive clock management circuitry features up to eight all digital DLLs and a maximum of eight PLLs.

Compared to equivalent FPGAs operating at the same voltage levels, XPA-II devices offer higher densities, better performance and lower power consumption. Low power consumption further contributes to cost savings as lower cost plastic packaging can be used in many cases. XPA-II products are designed for pin-for-pin replacement of Xilinx and Altera FPGAs and offer integration of multiple FPGAs into one ASIC. Package options include a wide range of Flip Chip BGAs in 1.00mm and 1.27mm pitches.

<table>
<thead>
<tr>
<th>XPA-II Base</th>
<th>User I/Os</th>
<th>DLLs</th>
<th>PLLs</th>
<th>18K Memory Blocks</th>
<th>No Distributed RAM</th>
<th>50% Distributed RAM</th>
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<td>Memory Bits (K)¹</td>
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(1) Usable 2RW RAM bits
(2) Usable 2-NAND equivalent logic gates

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