N-Sinker formation by Phosphorous Silicon Glass Diffusion

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***Abstract* — Drain current of Vertical DMOS transistors is collected in a buried layer and brought back to the silicon surface via highly doped path made along isolation trench by doping of the isolation trench sidewall. The present article compares two doping techniques for the formation of this highly doped path also called n-sinker. Both techniques use Phosphorous doped oxide as doping source. They differ by the way of forming the oxide layer, either using $POCl_3$ or PSG**

Index: Phosphorous Silicon Glass, $POCl_3$, n-sinker

I. Introduction

On Smart Power technologies, the drain current of the vertical transistors is collected in the buried layer and has to be brought back to the wafer surface. Highly n-doped paths (n-sinker) going from the wafer surface down to the buried layer are created in order to electrically connect the buried layer to the silicon surface, as depicted in Fig 1.

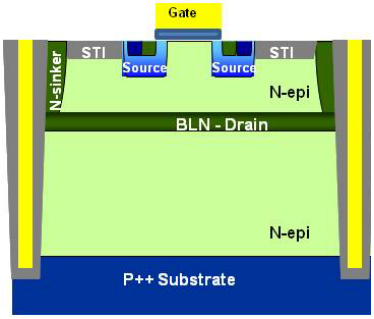

Figure 1: Schematic of a VLDMOS. Drain current is collected in the BLN and brought back to the surface via the n-sinker along the isolation trench.

These buried layer connection must have a very low resistivity in order to keep a low R_{on}, must consume the less Si area as possible and should be easy to integrate to the process flow. Low resistance is achieved by very high silicon doping; easy integration is achieved by combining the n-sinker and the isolation module [1], [2]. The n-sinker is thus processed together with the isolation module by doping silicon through the sidewall of the trench. By this way a low resistive path is built from the top surface top the buried layer. Due to the high aspect ratio of the trench, the only way to dope the silicon along the trench sidewall is by solid source diffusion. A conformal layer with a high Phosphorous content is deposited in the trench and a high thermal budget diffuses the Phosphorous in the silicon. N-sinker formation by means of two different layers acting as Phosphorous sources is demonstrated and comparison is made between Phosphorous glass made by $POCl_3$ oxidation and Phosphorous doped Silicon Glass (PSG) as doping source. Choice of the methods is finally driven by equipment availability.

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II. Doping Process

The Deep Isolation Trench / n-sinker module processing starts with the growth of an n- epi layer on top of a p^{++} substrate, forming a diode which ensures good planar junction isolation toward the substrate. An n+ buried layer (BLN) is formed by implantation and a second n- epi is grown to form the device layer. After TEOS hard mask deposition and lithography, a trench is etched down to the buried layer. The n-sinker is then created by phosphorus diffusion along the sidewall of the trench. Once the connection to the BLN has been made, trench etching is continued a few µm down into the substrate in order to achieve the lateral isolation between two adjacent pockets. The trench sidewall is then oxidized and the trench is sealed by polysilicon filling. The planarization of the trench after filling can be done by dry etch or CMP. Our work focuses on the sidewall doping, using $POCl_3$ or PSG.

A. $POCl_3$ doping

An N_2 carrier gas is saturated in $POCl_3$ by bubbling through a $POCl_3$ tank before entering a furnace. A Phosphorous glass is then formed though oxidation at a temperature of 970°C, according to the following equation:

$$4POCl_3 + 3O_2 \rightarrow P_4O_{10} + 6Cl_2$$

The furnace operates below atmospheric pressure to ensure a uniform and conformal deposition of the Phosphorous glass on the wafers and inside the trenches. Deposition is stopped by switching off the N_2 carrier and O_2 flows and Phosphorous is liberated from the glass as by-product from the oxido-reduction of the silicon by P_4O_{10} according to the following equation:

$$P_4O_{10} + 5Si \rightarrow 4P + 5SiO_2$$

This reaction occurs also at 970 °C under nitrogen ambient. The amount of available Phosphorous is determined by the time and temperature of the deposition step while the diffusion is controlled by the time and temperature of the drive-in step.

B. PSG doping

Phosphorous silicon glass is made by Atmospheric Pressure Chemical Vapor Deposition (APCVD) using SiH_4 as precursor gas and NO_2 as reactant. The Phosphorous content of the film is tuned by varying the PH_3 gas flow. Low pressure processing ensures a conformal deposition. Phosphorous is then diffused into the silicon sidewall thanks to an annealing step under N_2 ambient.

C. Phosphorous doped layer removal

After Phosphorous diffusion the highly phosphorous doped layer is removed by etching in lowly concentrated HF. A high selectivity towards hard mask TEOS film is required in order to minimize the CD increase of the hard mask which is later used to further etch the isolation trench.

III. Process Results

A. Deposition conformality

Due to the thick n- epi required to sustain high breakdown voltage for the high voltage transistors, isolation trenches must be deep but also as narrow as processing allows in order to save silicon area. It results in trenches with high aspect ratio, from which the sidewalls and bottom have to be uniformly doped. Conformality of the deposition is thus essential.

1) $POCl_3$

Fig. 2 shows a cross section of the trench after $POCl_3$ processing (deposition + drive-in step).

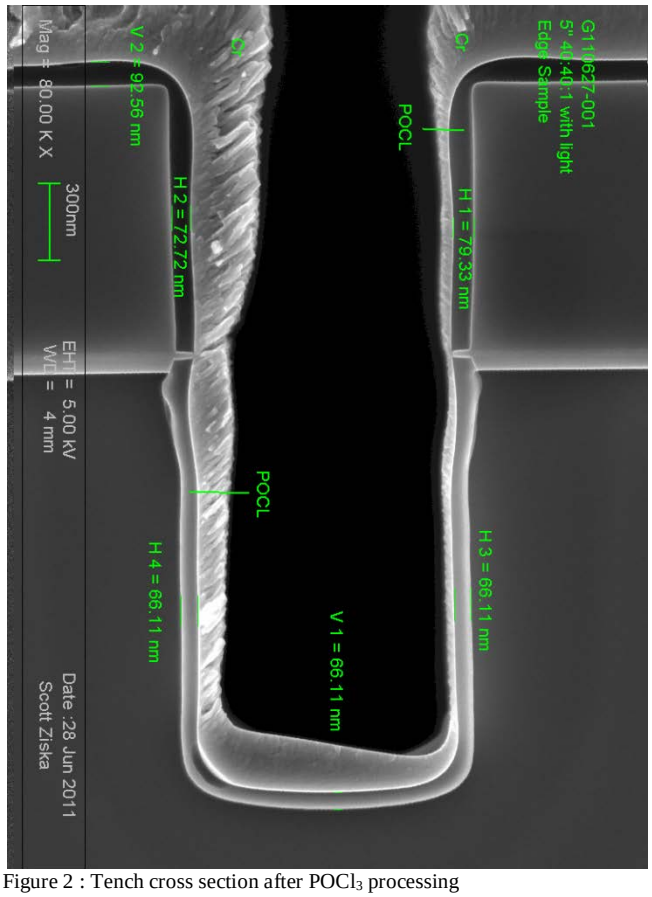

Figure 2 : Tench cross section after $POCl_3$ processing

The sample has been sputtered with Chromium before layer decoration. The Phosphorous glass deposition is very conformal. Thickness ranges from approximately 90 nm on the top surface down to 65 nm on the trench sidewall close to the trench bottom.

2) PSG

Fig. 3 shows a cross section of the PSG layer capped by a nitride layer. Here also the deposition is nicely conformal. For approximately 400 nm deposited on the top surface, roughly 250 nm are covering the sidewalls at the trench top and around 200 nm at the trench bottom, which will ensure a uniform doping of the trench sidewalls.

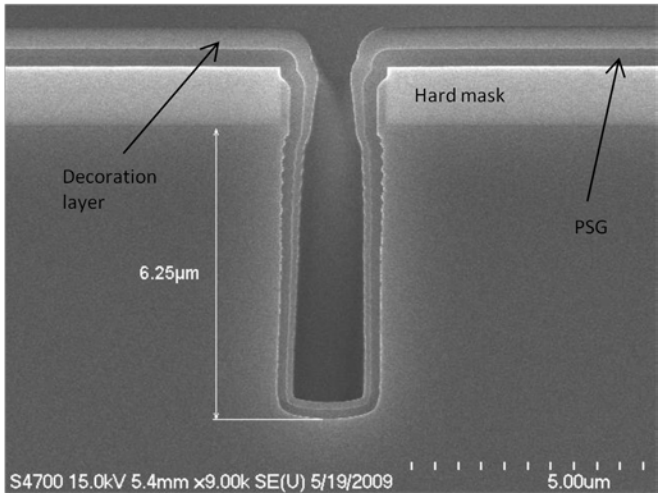

Figure 3: Conformal deposition of PSG

B. Diffusion depth and RSheet

In order to minimize the on-state resistance of the high voltage devices, the resistance of the n-sinker must be as low as possible. It is achieved by high doping of the silicon sidewalls. However, the Phosphorous must not diffuse too far away from the sidewall, in order to keep the size of the isolation / sinker module as small as possible.

1) $POCl_3$

Table 1 reports the various processing conditions which have been tested for $POCl_3$, as well as the resulting sheet resistance (Rsheet) measured on blanket silicon, immediately after doping process but also after a 1 kÅ wet oxidation.

Temperature	900	970	970	970	970	1000
Deposition time in min.	21	5	10	15	25	10
Diffusion time in min.	30	60	60	50	50	60
Rsheet after $POCl_3$ in Ω/sq	15.5	12.5	8	6.35	3.5	5.5
Rsheet after 1kÅ wet oxidation at 100O°C in Ω/sq	8.5	-	7.5	5.5	-	5.5

Table 1: $POCl_3$ deposition parameter and measured Rsheet

Long processing time and high temperature yield low Rsheet, confirming high Phosphorous content. There is a large drop in Rsheet after oxidation for the $POCl_3$ processed at 900 °C,

indicating that the Phosphor was further activated and diffused during oxidation.
Sheet Resistance Profile (SRP) from Fig. 4 shows the diffusion of the phosphorous into the silicon. Measurements were performed on blanket wafers.

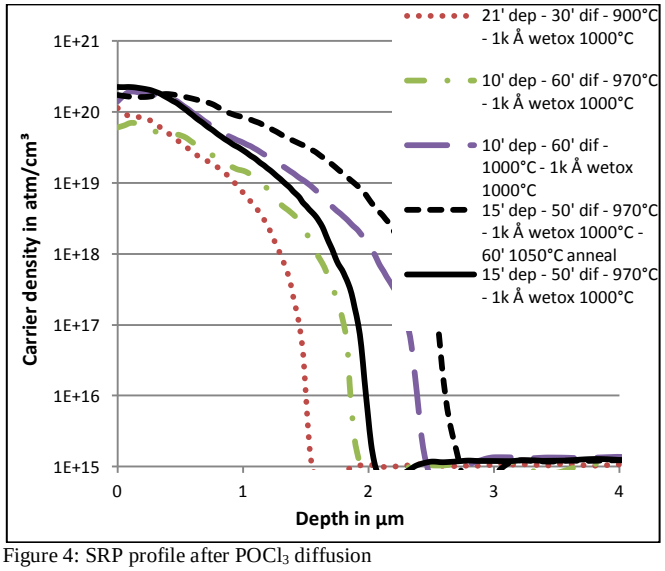

Figure 4: SRP profile after $POCl_3$ diffusion

Increasing the $POCl_3$ process temperature yields high surface concentration and deeper Phosphorous diffusion. Increasing the deposition time of the $POCl_3$ processing results mainly on an increased Phosphorous concentration close to the surface. An extra 60 min anneal at 1050°C increases the diffusion depth of roughly 800 nm.

2) PSG

Contrarily to $POCl_3$ processing for which the deposited layer has a fixed Phosphorous content, Phosphorous concentration of the PSG film can be tuned by playing with the PH_3 gas flow during deposition. Fig.5 shows the resulting silicon Rsheet obtained for various Phosphorous concentrations of the PSG films and diffusion time.

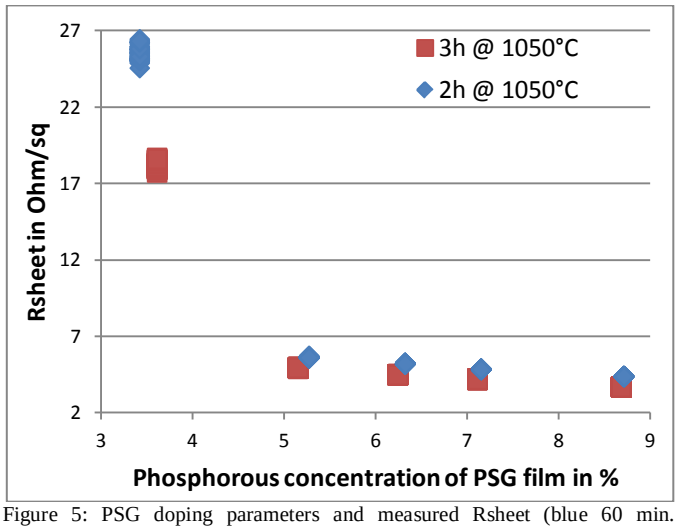

Figure 5: PSG doping parameters and measured Rsheet (blue 60 min. diffusion, black 120 min. diffusion at 1050°C in N_2)

Phosphorous concentration above 5 % allows reaching Rsheet of 5.6 Ω/sq after 120 min annealing at 1050°C. Increasing the Phosphorous content of the PSG film up to 8.5% has no significant impact on Rsheet, yielding a value of 4.5 Ω/sq for similar annealing conditions. Comparable Rsheet decrease can be obtained by extending the anneal time from 2 to 3 hours. However, increasing the anneal time will be made at the expense of the diffusion depth of the Phosphorous into the silicon as can be seen in Fig. 6.

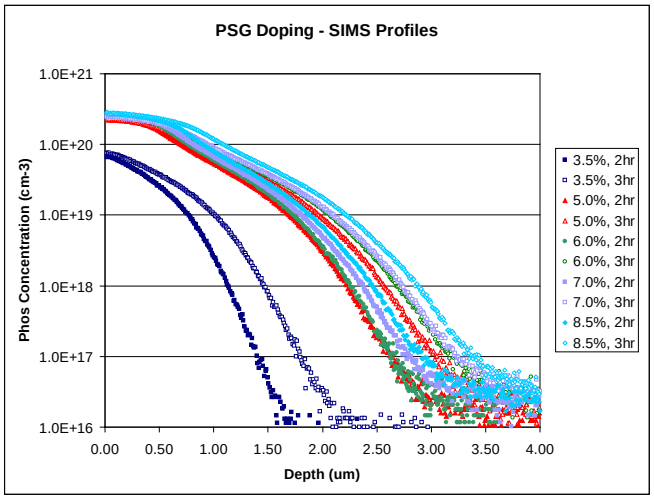

Figure 6: SIMS profile after PSG diffusion

As a consequence, if a low Rsheet is needed, high Phosphorous content of the PSG film rather than long diffusion time should be chosen. Moreover, in our integration scheme, thermal budget must be kept under control to avoid excessive diffusion of the buried layer.

3) Comparison

Both $POCl_3$ and PSG methods provide Phosphorous doped layer from which the Rsheet and diffusion depth is impacted by the thermal budget. Fig. 7 compares Rsheet and diffusion depth for $POCl_3$ processes.

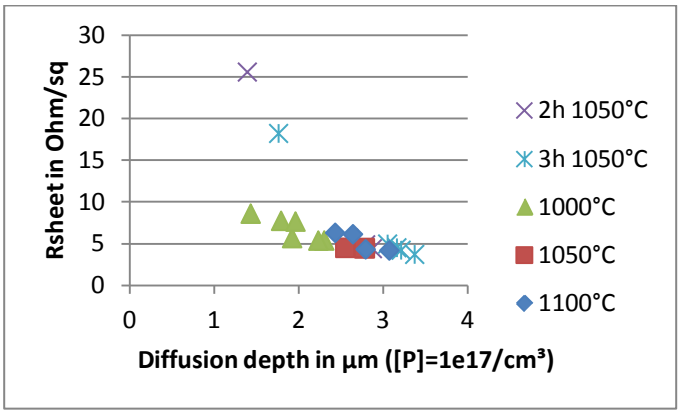

Figure 7: Diffusion depth vs Rsheet for POCl3 and PSG doping methods

Ideally, a low Rsheet combined with a low penetration depth is preferred to achieve a lowly resistive n-sinker while consuming as few as silicon as possible. For equivalent Rsheet, the splits having the lowest thermal budget show the less penetration depth of Phosphorous.

C. *Doping layer removal and selectivity towards TEOS*

Once Phosphorous has been out diffused from the doping layer, the p-glass or PSG must be removed. The critical point here is to limit the attack of the TEOS hard mask, which is later used for the 2nd trench etch.

1) *$POCl_3$*

The attack of TEOS exposed to $POCl_3$ step has been characterized in diluted HF. Fig. 8 plots the etched thickness in function of etch time in HF 0.34%

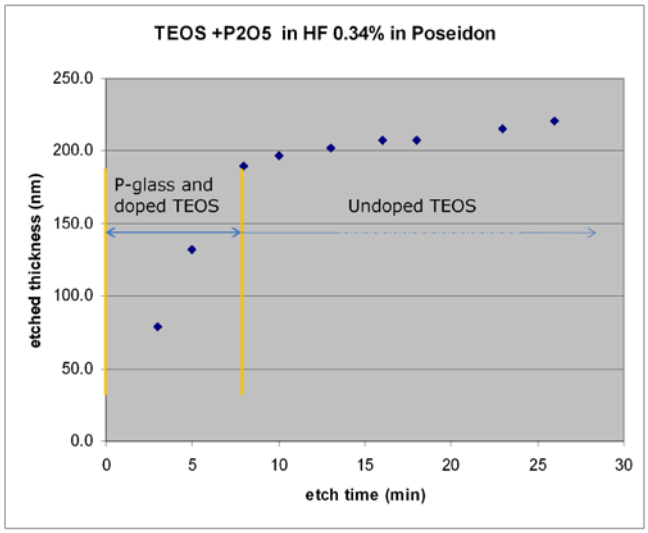

Figure 8: P-glass removal on TEOS

The first 180 nm are etched at a much faster rate than the remaining TEOS. It corresponds to the p-glass and doped TEOS. The etch rate of doped TEOS in HF 0.34% is 22 nm / min, versus 1.6 nm/min for the undoped TEOS. It ensures thus a limited CD increase of the TEOS hard mask, as seen on Fig.9.

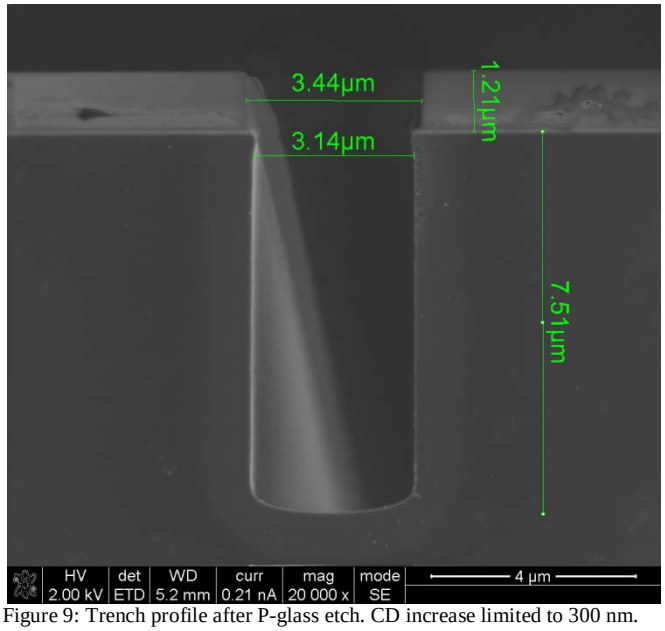

Figure 9: Trench profile after P-glass etch. CD increase limited to 300 nm.

2) *PSG*

Similar selectivity measurements have been performed between PSG and undoped HDP oxide and are shown in Fig. 10.

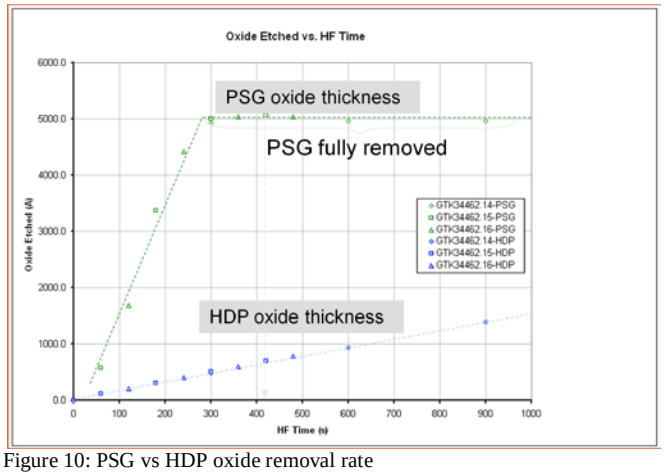

Figure 10: PSG vs HDP oxide removal rate

PSG is etched in at a rate of 98 nm/ min, while HDP oxide is etched at a rate of 4.7 nm/min. This selectivity of 20 ensures thus also a limited CD increase, as seen on Fig. 11.

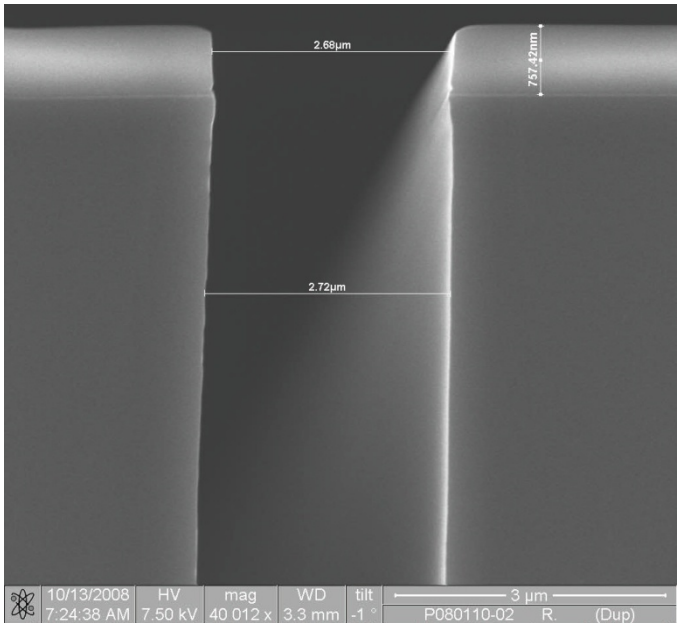

Figure 11: Trench profile after PSG removal

PSG and $POCl_3$ routes are similar in terms of integration complexity. Hard mask CD increase being limited for both routes, 2nd trench is processed without any issue.

D. *Impact on electrical properties of VDMOS*

Finally, the impact of Phosphorous lateral diffusion on VDMOS breakdown voltage has been characterized. Fig. 12 shows the VDMOS breakdown voltage decrease with the Phosphorous penetration depth.

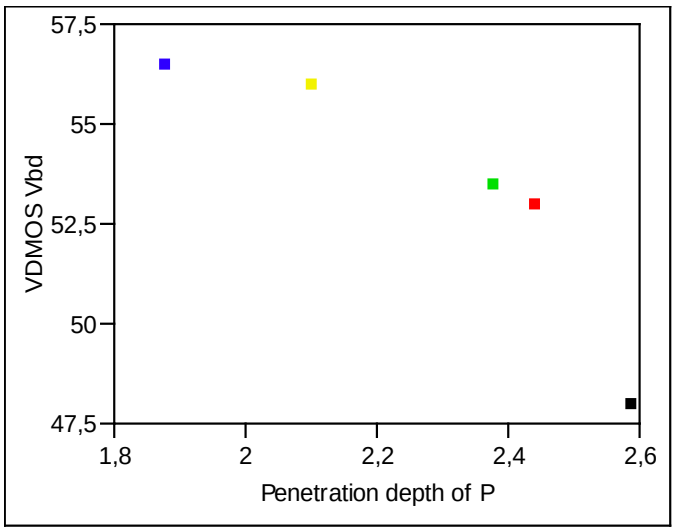

Figure 12: VDMOS breakdown voltage versus Phosphorous diffusion depth.

As can be seen in Fig. 13, in an ideal case P-drift and N-sinker regions are separated by lowly doped n- silicon. Excessive diffusion of the N-sinker, which get then too clause to the P-drift region of the VDMOS, will make the VDMOS break earlier than designed.

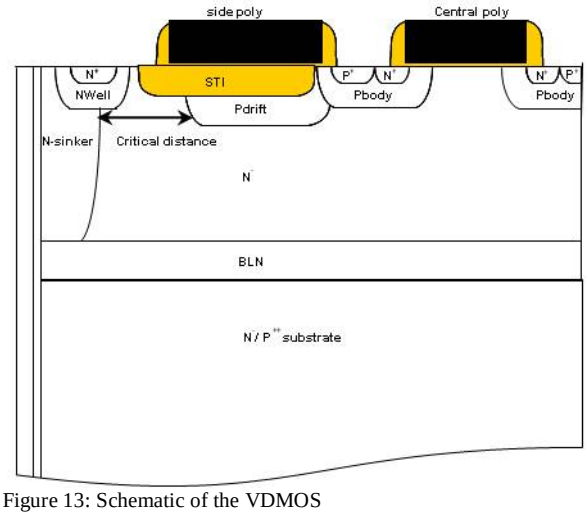

Figure 13: Schematic of the VDMOS

A critical distance between the P-Drift region and the N-sinker must then be respected in order to keep the breakdown voltage of the VDMOS transistor within specification. This can be achieved by keeping the thermal budget of the n-sinker diffusion under control, which has an impact on sinker sheet resistance, or by adjusting the design rule to keep the termination of the VDMOS sufficiently far away from the isolation, at the expense of the silicon area consumption.

IV. Conclusion

N sinker formations by PSG or $POCl_3$ diffusion were compared. The both techniques are equivalent in terms of process integration complexity. They both entail a deposition phase followed by a diffusion phase. The $POCl_3$ process presents a slight advantage since diffusion can be made in the same tube as the deposition tube. The removal of the doping layer is done in diluted HF with a good selectivity towards TEOS for both $POCl_3$ and PSG processing. The penetration depth of the Phosphorous, parameter which might impose as design rule a minimal distance between isolation trench and device termination is slightly higher for the PSG process than for the $POCl_3$, but might be tuned by playing with the thermal budget of the diffusion. Finally, both techniques are equivalent and choice of the one with respect to the other will be determined by equipment availability in fabrication line.

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[2] F. De Pestel, P. Coppens, H. De Vleeschouwer, P. Colson, S. Boonen, T. Colpaert, P. Moens, D. Bolognesi, G. Coudenys, M. Tack, “Deep Trench Isolation for a 50V 0.35 µm Based Smart Power Technology”, *ISPSD*, 2003, pp182-185.