Optimizing Low Side Gate Resistance for Damping Phase Node Ringing of Synchronous Buck Converter

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***Abstract*—This paper presents a method to optimize gate resistance of low side MOSFET in terms of damping phase node ringing for high efficiency synchronous buck converter. This method analyzes damping effect of low side gate resistance in the network of parasitic capacitances of MOSFET die and parasitic inductances of MOSFET package. Optimization equations for low side gate resistance are derived based on parasitic inductances and capacitances. Experiment proves the validity of this optimization design for low side gate resistance.**

I. INTRODUCTION

Phase node ringing of synchronous buck converter is caused by parasitic switching loop inductance and parasitic capacitance of power devices [1]. The ringing may lead to electrical over stress of high side and low side MOSFETs, shorting through, or failure of system in EMC regulation. Therefore, ringing of phase node in synchronous buck converter must be controlled.

Many methods have been developed to control phase node ringing for synchronous buck converter [2]. One method is using large high side gate resistance, so that turn-on of high side MOSFET is slowed down. This method could reduce phase node ringing effectively. However, it reduces efficiency of synchronous buck converter significantly due to significantly increased switching power loss of high side MOSFET. In the same idea, some other methods take advantages of source inductance of high side MOSFET or boost resistance of high side driver to slow down switching speed of high side MOSFET to control phase node ringing [3][4]. These methods all result in low converter efficiency. Another method is to use RC snubber connected between phase node and ground to damping phase node ringing. This is the method commonly used in high efficiency synchronous buck converter. However, RC snubber still consumes energy during switching. The higher capacitance is, the more energy consumed in the RC snubber.

In this paper, an optimized design of low side gate resistance is proposed in terms of damping phase node ringing. Analytic expressions are derived for low side gate resistance to damp phase node ringing, while maintain high converter efficiency. Analytic expressions for optimizing gate resistance are derived based on parasitic network of capacitance, C_{GS}, C_{GD}, and $C_{DS,}$ and parasitic package inductance, L_D, L_G and $L_{S,}$ Experiment proves the optimized gate resistance helps damping phase node ringing, while maintain high converter efficiency.

II. OPTIMIZING LOW SIDE GATE RESISTANCE IN SYNCHRONOUS BUCK CONVERTER

Figure 1 shows a synchronous buck converter with parasitics in both high side and low side MOSFET switches.

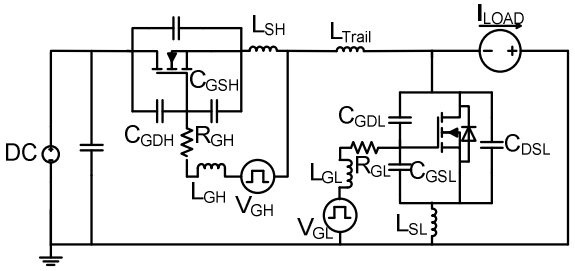

Figure 1 Synchronous buck converter with parasitic capacitances and inductances

L_{SH} and L_{SL} are package source inductance at high side and low side MOSFET [5]. Usually package inductance at drain side is much smaller than source inductance. Therefore, drain inductance is neglected in this paper. L_{trail} is inductance of PCB trail in switching loop.

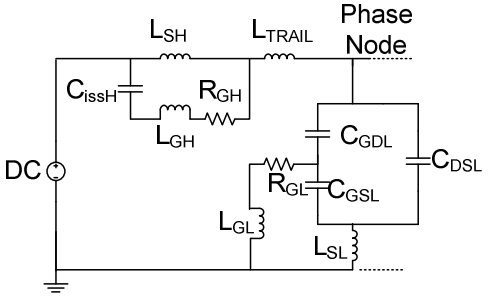

Figure 2 Turn-on Ringing Circuit of Synchronous buck converter

Figure 2 shows equivalent turn-on ringing circuit of synchronous buck converter. In high efficiency

synchronous buck converter, on-state resistance of high side MOSFET is usually less than 10mΩ, which is too small to damping any phase node ringing. Therefore, on-state resistance is not shown in Figure 2. In fact, the real damping resistance of phase node ringing is gate resistance of high side MOSFET and low side MOSFET. To optimize damping effect of phase node ringing, it is equivalent to maximizing ratio of current flowing through gate resistance to total ringing current. For the reason that high side gate resistance has strong effect on efficiency of synchronous buck converter, only gate resistance of low side MOSFET is optimized in terms of damping phase node ringing in this paper.

In Figure 2, gate branch of high side MOSFET has three components, R_{GH}, L_{GH},and C_{issh}. Impedance of gate branch of high side MOSFET is shown in equation (1).

$$X_{GH} = R_{GH} + j\left(\omega \cdot L_{GH} - \frac{1}{\omega \cdot C_{ISSH}}\right) \tag{1}$$

Here, ringing frequency is expressed by equation (2).

$$\omega \approx \frac{1}{\sqrt{(L_{SH} + L_{SL} + L_{TRAIL}) \cdot (C_{GDL} + C_{DSL})}} \tag{2}$$

Then the total impedance of high side MOSFET is expressed by equation (3).

$$X_H = \frac{X_{GH} \cdot \omega \cdot L_{SH} \cdot j}{X_{GH} + \omega \cdot L_{SH} \cdot j} \tag{3}$$

The equivalent damping resistance of high side gate resistance R_{eqH} is determined by the ratio of current passing through R_{GH} to total ringing current. The higher ratio of current pass through R_{GH}, the higher ratio of R_G contributes to total damping resistance. The equivalent damping resistance of high side gate resistance R_{GH} is derived and expressed by equation (4).

$$R_{eqH} = R_{GH} \times \left(\frac{\left| \frac{1}{X_{GH}} \right|}{\left| \frac{1}{X_H} \right|} \right)^2 = R_{GH} \cdot \left(\left| \frac{j\omega L_{SH}}{X_{GH} + j\omega L_{SH}} \right| \right)^2 \tag{4}$$

Here, $|X|$ means absolute value of a complex number.

In order to have equivalent damping resistance of gate resistance in low side MOSFET, delta connected parasitic capacitances, C_{GSL}, C_{GDL}, C_{DSL}, are first transformed to star connection capacitances C_{GL}, C_{DL}, C_{SL}. Turn-on ringing circuit of low side MOSFET is then transformed into circuit in Figure 3. Impedances of C_{GL}, C_{SL}, and C_{DL} in Figure 3 are expressed by equation (5).

$$X_{C_{GL}} = \frac{X_{C_{GSL}} \cdot X_{C_{GDL}}}{X_{C_{GSL}} + X_{C_{GDL}} + X_{C_{DSL}}} \tag{5}$$

$$X_{C_{DL}} = \frac{X_{C_{DSL}} \cdot X_{C_{GDL}}}{X_{C_{GSL}} + X_{C_{GDL}} + X_{C_{DSL}}}$$

$$X_{C_{SL}} = \frac{X_{C_{DSL}} \cdot X_{C_{GSL}}}{X_{C_{GSL}} + X_{C_{GDL}} + X_{C_{DSL}}}$$

Here, $X_{C_i} = \frac{1}{\omega \cdot C_i}$, i=GL, DL, SL, GSL, DSL, GDL.

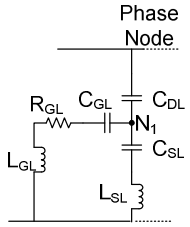

Figure 3 Equivalent Turn-on Ringing Circuit of low side MOSFET

Equivalent damping resistance of low side R_{eqL} is determined also by ratio of current passing through R_{GL} to total ringing current. Impedance of gate branch C_{GL}, L_{GL} and R_{GL} and source branch C_{SL} and L_{SL} in Figure 3 are expressed by equation (6) and (7).

$$X_{GL} = R_{GL} + j\left(\omega \cdot L_{GL} - \frac{1}{\omega \cdot C_{GL}}\right) \tag{6}$$

$$X_{SL} = j\left(\omega \cdot L_{SL} - \frac{1}{\omega \cdot C_{SL}}\right) \tag{7}$$

Then the total impedance from N1 to ground is expressed by equation (8).

$$X_{N1} = \frac{X_{GL} \cdot X_{SL}}{X_{GL} + X_{SL}} \tag{8}$$

The equivalent damping resistance of low side MOSFET is therefore expressed by equation (9).

$$R_{eq} = R_{GL} \cdot \left(\frac{\left| \frac{1}{X_{GL}} \right|}{\left| \frac{1}{X_{N1}} \right|} \right)^2 = R_{GL} \cdot \left(\left| \frac{X_{SL}}{X_{GL} + X_{SL}} \right| \right)^2$$

$$= \frac{\left(\omega \cdot L_{SL} - \frac{1}{\omega \cdot C_{SL}} \right)^2}{R_{GL} + \frac{\left[\omega \cdot L_{GL} - \frac{1}{\omega \cdot C_{GL}} + \omega \cdot L_{SL} - \frac{1}{\omega \cdot C_{SL}} \right]^2}{R_{GL}}} \tag{9}$$

Final equivalent ringing circuit of synchronous buck converter at high side turn-on is shown in Figure 4.

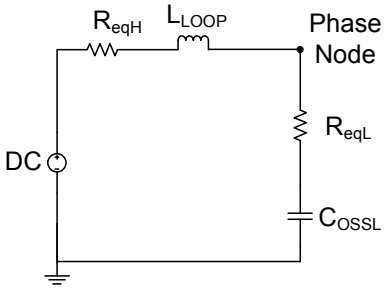

Figure 4 Equivalent turn-on Ringing Circuit

Here, C_{OSSL} is output capacitance of low side MOSFET. Loop inductance L_{LOOP} is expressed by equation (10).

$$L_{LOOP} \approx L_{SH} + L_{SL} + L_{TRAIL} \tag{10}$$

Damping time constant of circuit in Figure 4 is expressed by equation (11).

$$\tau \approx \frac{2 \cdot L_{TRAIL}}{R_{eqH} + R_{eqL}} \tag{11}$$

A. Maximize equivalent damping resistance

Obviously, the equivalent damping resistant in equation (9) has maximum value at the condition expressed by equation (12).

$$R_{GL} = \left| \omega \cdot L_{GL} - \frac{1}{\omega \cdot C_{GL}} + \omega \cdot L_{SL} - \frac{1}{\omega \cdot C_{SL}} \right| \tag{12}$$

Under the condition of equation (12), the maximum equivalent damping resistance is expressed by equation (13).

$$R_{eqL-\max} = \frac{\left(\omega \cdot L_{SL} - \frac{1}{\omega \cdot C_{SL}} \right)^2}{2 \cdot \left| \omega \cdot L_{GL} - \frac{1}{\omega \cdot C_{GL}} + \omega \cdot L_{SL} - \frac{1}{\omega \cdot C_{SL}} \right|} \tag{13}$$

To build in a gate resistance for low side MOSFET in terms of suppressing phase node ringing, the value of gate resistor must not exceed the value given by equation (12). Otherwise, gate resistance will reduce damping characteristics of phase node ringing and reduce converter efficiency due to slower turn-on and turn-off of low side MOSFET. Even worse, large gate resistance of low side gate resistance may turn-on low side MOSFET because of phase node ringing, which results in shorting through. Or large gate resistance of low side MOSFET may take long time to turn-off low side MOSFET, which may results in low side MOSFET is still on when high side MOSFET is turned-on.

III. EXPRRINMENT RESULTS AND DISCUSSIONS

Experiments are conducted to validate the damping characteristics of low side MOSFET and optimized damping resistance. Here the test setup has three parts: mother board, test board and driver board. Mother board provides stable input power and output power to synchronous buck converter; test board is the synchronous buck converter under test; driver board is driver for high side and low side MOSFETs. Here, the driver is NCP5901 with 12V driving voltage, which is a commonly used driver for application in computing devices.

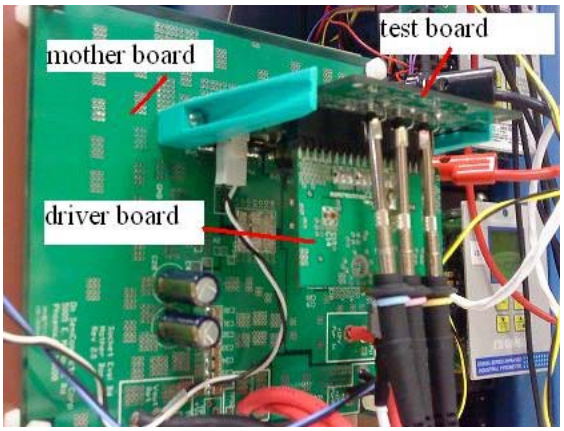

Figure 5 experiment setup for measuring phase node ringing

Schematic circuit of the experiment setup is shown in Figure 6. Here, all the parasitic capacitances and inductances, like gate inductance and source inductance, are included in package of high side and low side MOSFET. Gate resistance of high side and low side MOSFET are also built in MOSFET package. In experiment, the minimum gate resistance is the built-in gate resistance.

In order to verify the optimized equivalent damping resistance, waveform of phase node is first measured without any external gate resistance using driver NCP5901. Then 0.2Ω external gate resistance is connected in series with built-in gate resistance, so that the equivalent damping resistance is varied from its original value. As a consequence, the damping time constant of phase node ringing would be increased, if equivalent damping resistance is reduced, or be decreased, if equivalent damping resistance is increased. In the third step, a small capacitance is connected between gate and source of low side MOSFET, so that the driver sinking resistance is reduced by the external gate source capacitance. This method varies equivalent damping resistance and damping time constant of phase node ringing too.

The specific values of parameters in Figure 6 are: LL=1nH, RLL=2mΩ, Cout=88uF, Vout=1.2V, Vin=12V, fs=500kHz. In experiment, high side MOSFET is NTMFS4941 for all measurements and low side MOSFETs are NTMFS4836, NTMFS4835 and NTMFS4834 respectively.

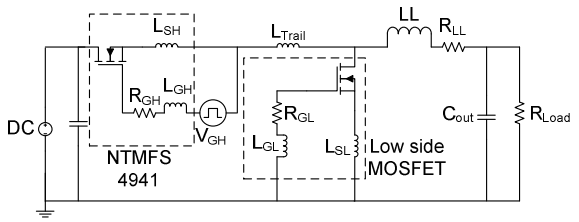

Figure 6 circuit of experiment setup

All the switching waveforms are measured using the same board and all the devices have the same package. Therefore, switching loop inductance is about the same for all the experiments. From ringing period, the switching loop inductance is calculated to be 2~2.5nH.

Parasitic capacitances and inductances of MOSFETs, NTMFS4941, NTMFS4836, NTMFS4835 and NTMFS4834, are listed in Table I.

TABLE I PARASITIC CAPACITANCES AND INDUCTANCES OF NTMFS4836, NTMFS4835, NTMFS4834 AND NTMFS4941

	NTMFS 4936	NTMFS 4835	NTMFS 4834	NTMFS 4941
C_{ISS}(PF)	*2677*	*3100*	*4500*	*1650*
C_{OSS}(PF)	*565*	*670*	*960*	*570*
C_{RSS}(PF)	*307*	*360*	*500*	*17*
L_S(nH)	*0.65*	*0.65*	*0.65*	*0.93*
L_G(nH)	*1.84*	*1.84*	*1.84*	*1.84*
Built-in Rg (Ω)	*1.2*	*1.3*	*1.4*	*1.1*

Based on ringing frequency and parasitic inductance and capacitances in Table I, equivalent damping resistance of low side MOSFETs, NTMFS4836, NTMFS4935 and NTMFS4834, are plotted in Figure 7 based on equation (**9**). Obviously, equivalent damping resistance of low side MOSFET is maximized when gate resistance is around 2Ω. Gate resistance of low side MOSFET greater than 2Ω does not help damping phase node ringing.

Because of sinking resistance of low side driver, which is typically around 0.8Ω for NCP5901, gate resistance of low side MOSFET is the sum of built-in gate resistance of MOSFET and driver sinking resistance. Also, the gate inductance of low side is the sum of parasitic gate inductance of low side MOSFET and inductance of PCB trail connecting low side driver and MOSFET. The PCB trail inductance of driver board is limited around 0.1~0.3nH because of optimized multilayer design.

Specific data for damping resistance for MOSFET pairs, NTMFS4941+NTMFS4836, NTMFS4941+ NTMFS4835, NTMFS4941+NTMFS4834, are calculated in Table II, Table III, and Table IV.

Equivalent damping resistance of NTMFS4941 in Table II, Table III, and Table IV are calculated from equation (4). Equivalent damping resistance of NTMFS4941 does not change when gate resistance of low side MOSFET varies. It changes only when ringing frequency changes.

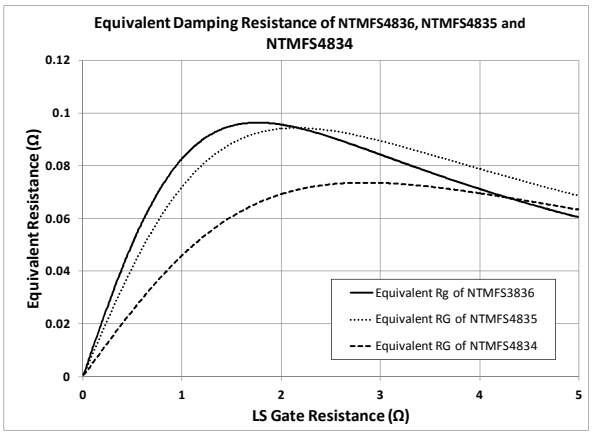

Figure 7 Equivalent damping resistance of NTMFS4836 at various gate resistance

TABLE II EQUIVALENT DAMPING RESISTANCE OF NTMFS4941+NTMFS4836 PAIR

	RG=1.2Ω	RG=2.0Ω	RG=2.2Ω
NTMFS4941 Req (Ω)	*0.065*	*0.065*	*0.065*
NTMFS4836 Req (Ω)	*0.09*	*0.096*	*0.094*
Total Req (Ω)	*0.155*	*0.161*	*0.159*
Damping Time constant (ns)	*28.3*	*27.3*	*27.6*

Here, gate resistance of low side MOSFET is changed varied from 1.2Ω to 2.2Ω. Phase node damping time constant is first decreased from 28.3ns to 27.3ns, and after that, damping time constant increases from 27.3ns to 27.6ns, which means that equivalent damping resistance of low side MOSFET first increase and later decreases.

TABLE III EQUIVALENT DAMPING RESISTANCE OF NTMFS4941+NTMFS4835 PAIR

	RG=1.3Ω	RG=2.1Ω	RG=2.3Ω
NTMFS4941 Req (Ω)	*0.069*	*0.069*	*0.069*
NTMFS4835 Req (Ω)	*0.084*	*0.094*	*0.094*
Total Req (Ω)	*0.153*	*0.163*	*0.163*
Damping Time constant (ns)	*28.70*	*27.00*	*27.00*

Here, gate resistance of NTMFS4835 is increased from 1.3Ω to 2.3Ω. Equivalent damping resistance of NTMFS4835 increases first then stays stable, which means that 2.3Ω gate resistance is the optimized gate resistance for NTMFS4835. If gate resistance is higher than 2.3Ω, damping effect of NTMFS4835 would be decreased.

TABLE IV EQUIVALENT DAMPING RESISTANCE OF NTMFS4941+NTMFS4834 PAIR

	RG=1.4Ω	RG=2.2Ω
NTMFS4941 Req (Ω)	*0.089*	*0.089*
NTMFS4834 Req (Ω)	*0.058*	*0.071*
Total Req (Ω)	*0.147*	*0.16*
Damping Time constant (ns)	*33.00*	*30.00*

Here, gate resistance of NTMFS4834 is increased from 1.4Ω to 2.2Ω. Equivalent damping resistance is increased. Experiment of NTMFS4834 at gate resistance higher than 2.2Ω is not shown for the reason that shorting through is observed in experiment in this condition.

Figure 8 to Figure 14 are experiment phase node waveforms with high side MOSFET NTMFS4941 and low side MOSFET NTMFS4836, NTMFS4835, and NTMFS4834 respectively. These three low side devices have significant ringing in phase node during high side turn-on. Exponential damping curves with damping time constant in Table II, Table III, and Table IV are plotted in Figure 8 to Figure 14. It is clearly shown that the predicted damping constants precisely fit experiment data.

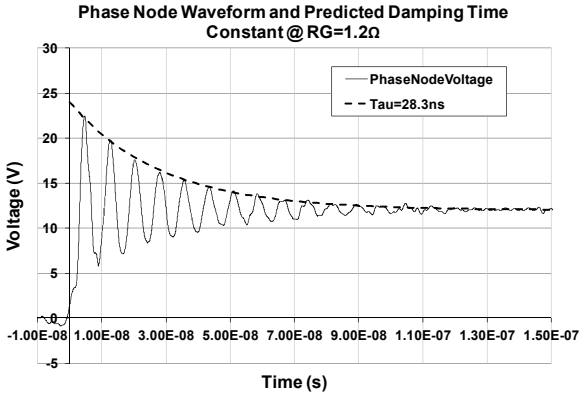

Figure 8 phase node waveform of NTMFS4941+NTMFS4836 and predicted damping time constant @ RG=1.2Ω

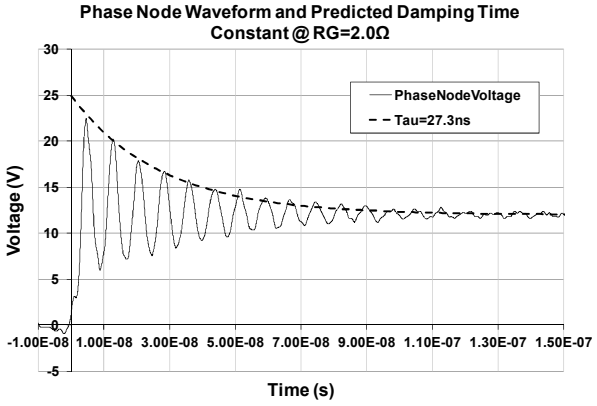

Figure 9 phase node waveform of NTMFS4941+NTMFS4836 and predicted damping time constant @ RG=2.0

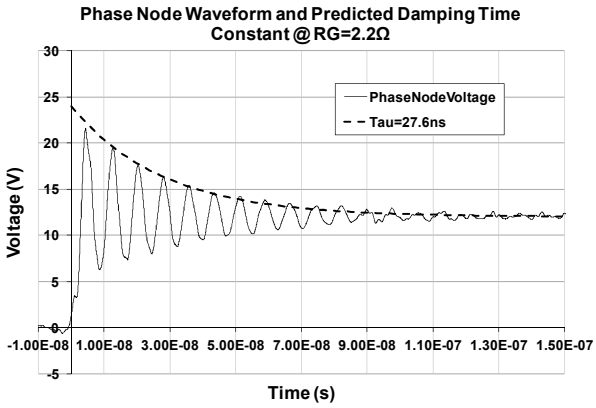

Figure 10 phase node waveform of NTMFS4941+NTMFS4836 and predicted damping time constant at gate resistance @ RG=2.2Ω

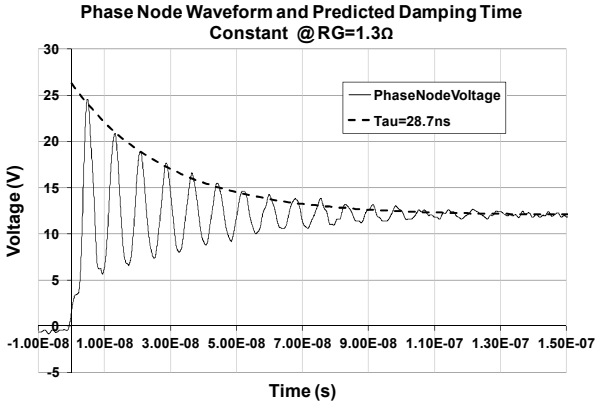

Figure 11 phase node waveform of NTMFS4941+NTMFS4835 and predicted damping time constant at gate resistance @ RG=1.3Ω

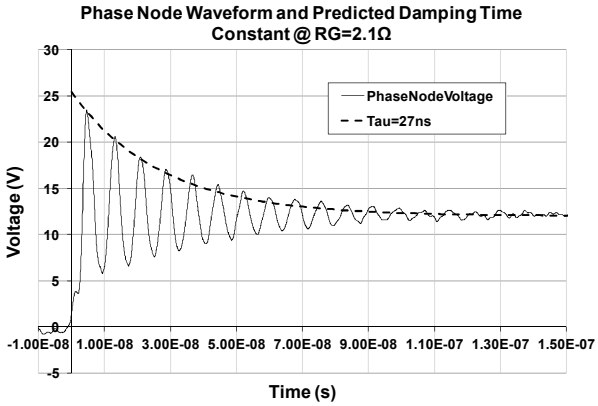

Figure 12 phase node waveform of NTMFS4941+NTMFS4835 and predicted damping time constant at gate resistance @ RG=2.1Ω

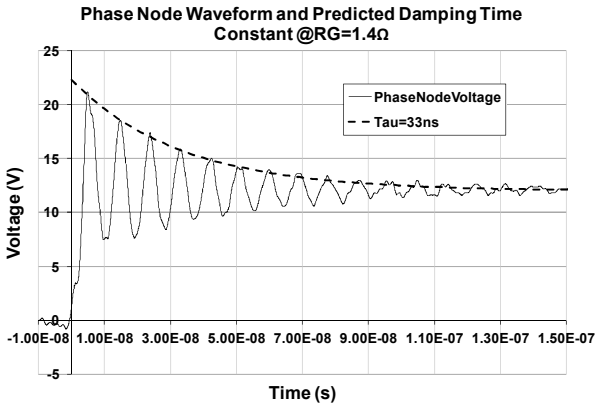

Figure 13 phase node waveform of NTMFS4941+NTMFS4834 and predicted damping time constant at gate resistance@ RG=1.4Ω

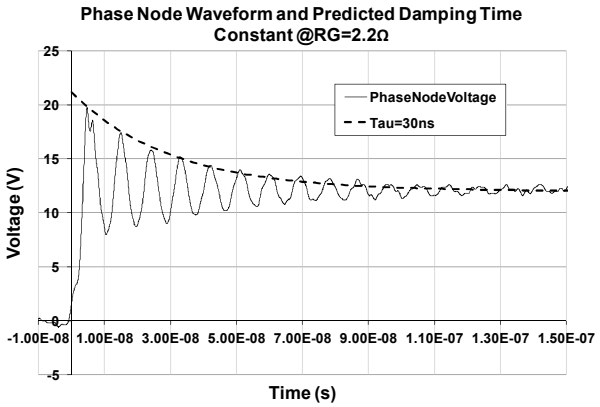

Figure 14 phase node waveform of NTMFS4941+NTMFS4834 and predicted damping time constant at gate resistance @ RG=2.2Ω

Efficiency of synchronous buck converter with various low side gate resistances of NTMFS4836 is measured by a benchmark of acquisition and reliability testing system. Gate resistance of NTMFS4836 is 1.2Ω, 2.0Ω and 2.2Ω, respectively. Efficiency measurement condition is the same with the condition measuring phase node ringing. The system measures the input power output power and driver power. Efficiency is calculated by output power divided by the sum of input power of synchronous buck converter and driver power. Load current is swept from 1A load current to 25A load current, which is a commonly load current range.

Experiment results show that efficiency curves of synchronous buck converter is not sensitive to low side gate resistance. This is because that switching of low side MOSFET is mainly zero voltage switching. The slightly difference in efficiency curves is in light load condition, where output power is low and, therefore, slight difference in driver loss and switching loss of low side MOSFET could make difference in total efficiency curves.

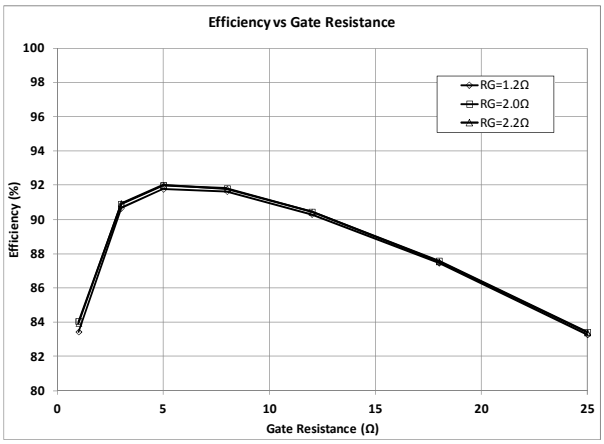

Figure 15 Efficiency curves of NTMFS4836 at various gate resistance

IV. CONCLUSION

An optimized design of low side gate resistance is proposed in terms of damping phase node ringing for synchronous buck converter. Analytic optimization expressions are derived for low side gate resistance in terms of damp phase node ringing. Experiment proves the optimized gate resistance helps improve damping phase node ringing, while maintain high converter efficiency

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