ONC25

Process Technology

ONC25: 0.25 μm Process Technology

ON Semiconductor®

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Overview

The ONC25 process family from ON Semiconductor is an ideal 0.25 mm low cost solution to **mixed−signal designs**. ONC25 is designed for 2.5, 3.3, 5.0 V single−gate or 2.5 / 3.3 V or 2.5 / 5 V dual−gate operation with high−performance / low−power and mixed−signal 2.5 V or 5.0 V digital libraries, and mixed−signal features such as MIM capacitors, Schottky diodes, zener diodes, high resistivity poly, deep N−well for P−well isolation and under N−well in the digital blocks to optimize packing density. ONC25 provides the flexibility to implement a variety of mixed−signal applications.

Features

- Gate Oxide Voltages: 2.5, 3.3, 5.0 V
- 2 to 5 Metal Layers
- Top Metal Option Thicknesses: 1.0, 1.5, 3.0 μm
- MIM Capacitor: 1.0 fF/μm^2 Located Below Top Metal
- Schottky Diodes
- Zener Diodes: 5.15, 5.5, 6.2 and 7.4 V
- High Sheet Resistance (1.5 kW) Polysilicon Resistor
- Low Temperature Coefficient Polysilicon Resistor
- Salicide Process with Optional Blocking
- Deep N−well for P−well Isolation, NPNs, and also May be Used Under N−well in the Digital Blocks to Optimize Packing Density

PROCESS CHARACTERISTICS

Operating Voltage	2.5, 3.3, 5 V
Substrate Material	200 mm P−Type, EPI
Drawn Transistor Length	0.25 μm (2.5 V CMOS)
Gate Oxide Thickness	50, 70, 125 nm
Contact/Via Size Drawn	0.3 μm / 0.36 μm
Top Metal Thickness	1.0, 1.5, and 3.0 μm
Contacted Metal Pitch	
Metal 1	0.64 μm
Metal 2−5	0.94 μm
Metal Composition	Al(0.5% Cu)

SAMPLE PROCESS OPTIONS

	Mask Layers
Single Gate, 2 Metal	16
Dual Gate, 2 Metal	22
Single Gate, 5 Metal	22
Dual Gate, 5 Metal	28

DEVICE CHARACTERISTICS

All Values Typical at 25°C

2.5 V TRANSISTORS

N−Channel	Typical Value	Units
V_t	0.53	V
I_{dsat}	490	μA/μm
P−Channel	**Typical Value**	**Units**
V_t	−0.53	V
I_{dsat}	−240	μA/μm

3.3 V TRANSISTORS

N−Channel	Typical Value	Units
V_t	0.58	V
I_{dsat}	520	μA/μm
P−Channel	**Typical Value**	**Units**
V_t	−0.79	V
I_{dsat}	−265	μA/μm

5.0 V TRANSISTORS

N−Channel	Typical Value	Units
V_t	0.82	V
I_{dsat}	500	μA/μm
P−Channel	**Typical Value**	**Units**
V_t	−0.88	V
I_{dsat}	−240	μA/μm

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RESISTORS

Resistors	Typical Value	Units
N−well under STI	1400	Ω/square
	3600	ppm/°C
P+poly unsilicided	280	Ω/square
	−75	ppm/°C
Low Tempco Poly unsilicided	335	Ω/square
	−34.2	ppm/°C
High Resistance Poly unsilicided	1500	Ω/square
	1200	ppm/°C

CAPACITORS

	Typical Value	Units
MIM (15 V max)	1	fF/μm^2
CPNW2V (2 V gate oxide to NW) V_{gs} = 2.5 V	5.28	fF/μm^2
CPNW3V (3 V gate oxide to NW) V_{gs} = 3.0 V	4.42	fF/μm^2
CPNW5V (5 V gate oxide to NW) V_{gs} = 5.0 V	2.46	fF/μm^2

DIODES

	Typical Value	Units
Pimp−to−NW diode BV (1 μA/μm)	8.07	V
Leakage (Vac = BV/2)	0.01	pA

BJT

	B_{vcen} ($\|I_c\|$ = 1 μA, $\|I_b\|$ = 1 nA)	Beta ($\|I_e\|$ = 5 μA, V_{cb} = 0)
NPN	8.2 V	15
PNP	19.3 V	2.5

LIBRARIES

Front−End Digital Design	
Digital	Synthesis Libraries
	Simulation Libraries
Analog	Design Rules
	Parametrized Layout Cells
	Spectre Models
Standard Cell	
5 V Core Shell	398 total cells
	1−layer metal and 2−layer metal pwr rail option
	33.1 k gates/mm^2 (Routed @ 75% util)
	0.122 ns prop delay (2−input NAND, fanout = 2)
2.5 V Core Shell	398 total cells
	1−layer metal and 2−layer metal pwr rail option
	33.1 k gates/mm^2 (Routed @ 75% util)
	0.056 ns prop delay (2−input NAND, fanout = 2)

MEMORY OPTIONS

OTP	
2.5 V Poly Fuse	32 −256 bit in 32 bit increments
5 V Poly Fuse	32 − 256 bit in 32 bit increments

CAD TOOL COMPATIBILITY

Digital Design	Synopsys Design Compiler
	Cadence RTL Compiler
	Mentor Graphics FastScan (DFT)
Analog/Mixed−Signal Design	Cadence Virtuoso, VirtuosoXL, Spectre and Eldo
	Mentor Graphics Design Architect IC, IC Station and Eldo
Place and Route	Cadence Encounter
	Synopsys Apollo
Physical Verification	Mentor Graphics Calibre

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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