



ON Semiconductor

Development and advantages of an integrated technology monitor.

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Introduction and motivation.

During the development of a new technology several test chips are made to check and optimize individual modules of the technology. Although these test chips contain a lot of structures that are no longer needed once the technology is released to production, they often are used to monitor the technology for several years after the production release. At the end of technology development yield enhancement monitors are built to support continuous yield improvement programs. When the technology reaches volume production, cost reduction programs and expanding production capacity require full process material to qualify optimized processes and new equipments. Time schedules of these projects are often negatively affected by the unavailability of full process qualification material. Combining all the structures needed to monitor the technology, support yield enhancement and equipment and process releases early in the technology life is a cost saving action

Description of approach and techniques.

For our 0.35 μ m technology we have integrated most of the quality monitors, defect enhancement structures and reliability structures into one test chip. The test chip contains a 1 Mbit RAM, gate oxide monitor structures, MIMC monitor structures, trench isolation monitor structures, electromigration structures as well as a small product.

On a weekly basis a 6 wafer lot is started to obtain a weekly monitoring of the most important technology and quality parameters. In-line electrical test is applied for the gate oxide defect density monitor to make the feedback loop as short as possible.

The wafers get defect inspections on about 15 stages, allowing us to monitor visual defects and estimate the impact of changes. Once out of the fab all structures are measured, and wafer sort and bitmap testing is performed on the RAM. The defect inspection results get overlaid with the bitmap results and the contribution of the in-line detected defects to the yieldloss is calculated. This information allows us to focus defect improvement programs on killer defects. Additional information of the other monitor structures can be used to optimize the yield model. Deviations from the model can be detected and the bitmap results allow an efficient failure analysis to detect none-visual yield killers.

The weekly lots are also used in case new processes or equipments need to be evaluated. This has reduced qualification cycles significantly. The product incorporated in the monitor allows us to have feedback on the impact on sort and final test yield and, if needed, product material is available for reliability evaluation.

Results/Conclusions/perspectives.

By combining monitor structures and yield enhancement structures as well as a product on 1 test chip, we succeeded in reducing the technology monitor cost significantly and at the same time in speeding up new process and equipment introductions. The same method can be applied to other technologies.