Components for WIRELESS Applications – To Integrate or Not Integrate

Jacques Lavernhe, System Engineering Manager at ON Semiconductor, looks at the design considerations when engineering portable devices

CONSUMERS ARE ALWAYS looking for a smaller but more feature-rich handset that integrates more functionality. However, they are reluctant to sacrifice battery life and, in fact, have longer duty cycles high on their wish list.

Battery technology is not advancing as quickly as the development of new functionality and its integration into the handset. And so semiconductor technology has to provide handset designers with more sophisticated power management solutions in order that battery duty cycles are not truncated to an unacceptable level. One of the trends is to integrate more functions into increasingly complex Power Management ICs (PMICs) with many voltage regulators, DC-DC converters, as well as other power management related functions. System-wise, it can also make sense to integrate audio CODEC and amplifiers plus other non-RF related analogue functions.

This approach can result in a three-chip highly-integrated solution, comprising the RF chip, baseband digital signal processor and application processor, and PMIC. Although this solution may require external components such as extra memory, the core of the system is highly integrated. The main advantages of this solution are a low component count, reduced cost bill of materials and highly reliable manufacturing.

Although the benefits of integrating several components and elements of functionality into a single IC seems a logical approach to save space and cost, there is a question mark over whether it is always feasible. Several potential drawbacks that may lead designers to adopt different integration schemes have to be considered.

Besides power consumption and power dissipation, other potential issues linked to integration include the layout of power rails and the optimal localization of power management and power generation functions on the PCB.

From a marketing and sales standpoint, the most important parameters are fast design cycle times and platform flexibility to enable the release of derivatives as soon as the market demands them. Clearly, highly integrated solutions are not flexible enough to accommodate new feature-rich functional modifications that may be required by fast changing market trends. They also may not always satisfy the demand for short design cycle times.

Integration Considerations

Lithium Ion batteries (Li-Ion) are the most popular source of power in the large majority of consumer and professional portable devices. These cells have a typical voltage of 3.6V but they can reach 4.2V when fully charged and drop down to 2.8V~3.0V when fully depleted. Usually, the device powered by the cell switches off when the voltage drops down to about 3.3V, to keep enough headroom and avoid safety issues associated with highly depleted batteries. To offset the relatively slow advances in battery technology, the logical and straightforward way to increase battery life in an application would be to increase their size. But, of course, this would also directly impact the overall size of the piece of portable equipment; something that would be totally unacceptable to consumers.

Another option designers can consider is to extend the battery operating range by reducing the low voltage safety margin and operating the system at a voltage lower than 3.3V. Some new battery technologies are expected to be able to support this approach. However, this leads to a need for more sophisticated power management techniques, higher control granularity and an increase in the amount of power

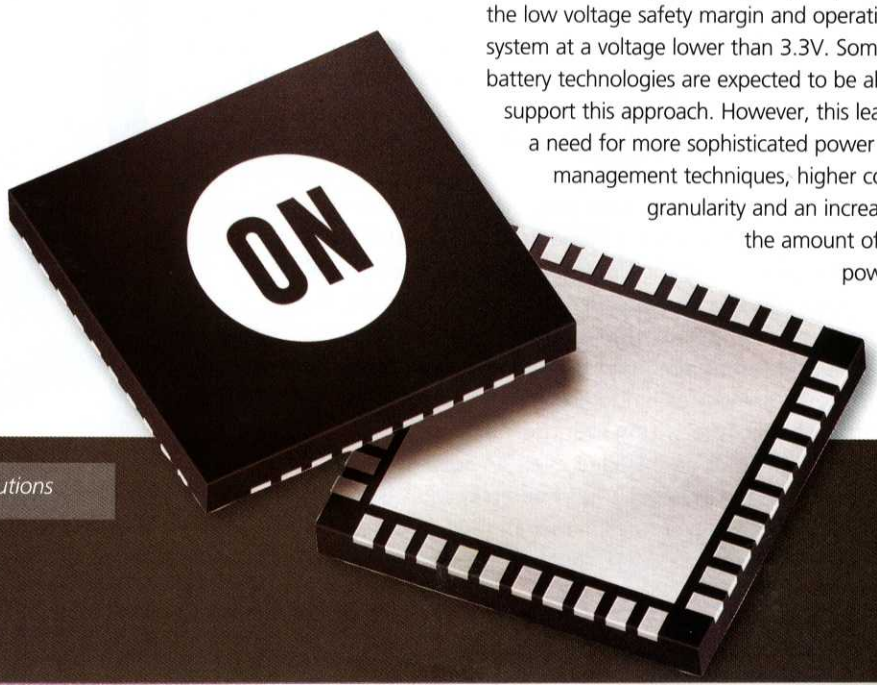

Figure 1: *Highly-integrated RF solutions*

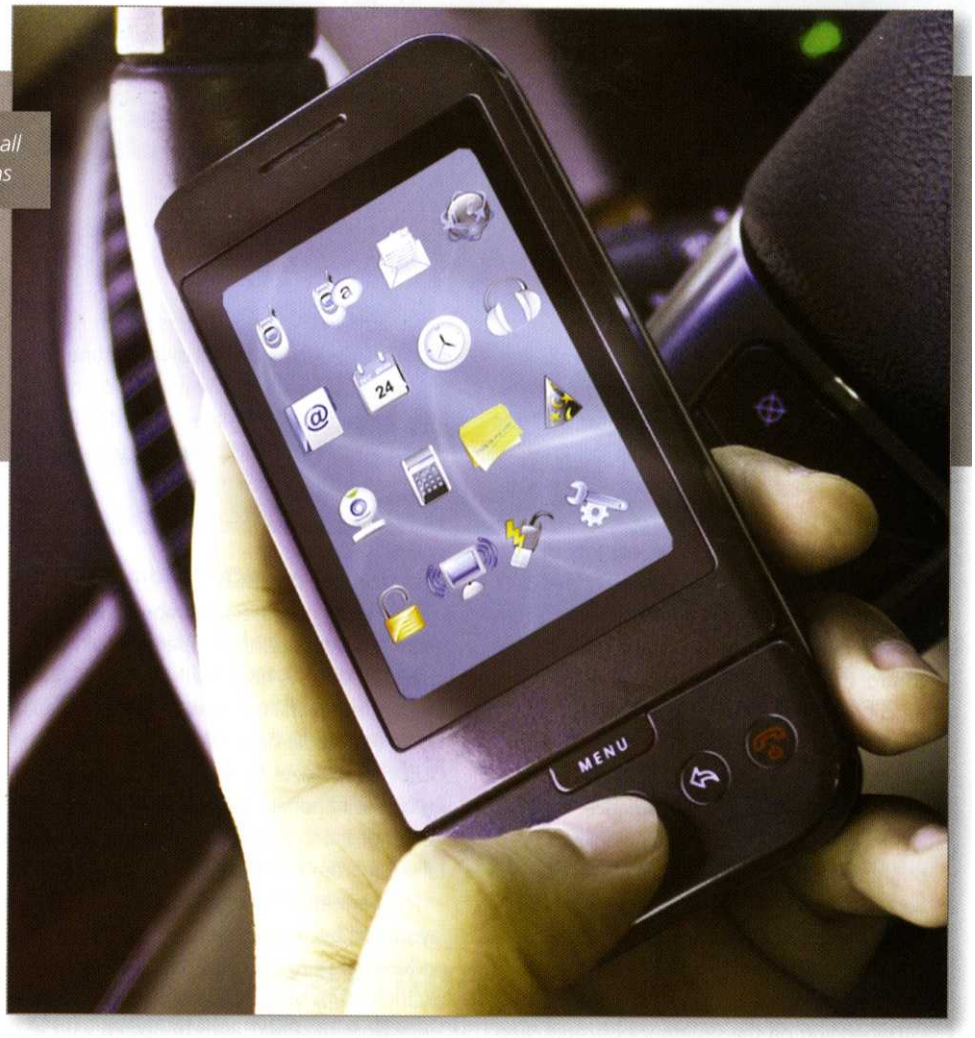

Figure 2: *Modern handsets require all types of specific design considerations*

domains in which the electronics will work. This can be achieved but at the price of higher complexity and higher cost, especially if implemented with off-the-shelf highly integrated PMICs.

An example wireless application powered by a Li-Ion cell may feature a processor controlling main functionality, memory extensions, peripherals such as display, keyboard, connectivity (USB, Bluetooth, Wi-Fi, WiMAX), a baseband processor controlling voice communication and also analogue functions such as RF, audio, video and battery charging. Each function of this system is optimised to operate from a different power supply rail and has to be controlled, enabled and disabled separately. Digital functions such as baseband and processors may require at least two supplies each: low voltage for core and higher voltage for I/Os to interface with other devices. Each analogue function and display may need higher voltage to provide powerful enough drivers.

Constraints, such as available PCB real estate, cost and manufacturing considerations could drive designers to use very highly integrated ICs. However, this approach brings up additional design challenges such as thermal management and signal routing issues. These may lead to the use of a separate IC on top of the main PMIC, or perhaps a different level of integration with a sub-system partitioning approach.

Thermal Management

When using very high integration level ICs with several regulators, DC-DC converters and other analogue functions, designers should be aware that the maximum power dissipation of the package is much lower than the potential power the silicon may have to evacuate in order to remain within an acceptable operating temperature range when all regulators are operating at their maximum current.

For instance, let's consider a handset application with the main power functions supplied by a highly integrated PMIC. In this example application, the PMIC integrates two 90% average efficiency DC-DC converters, five LDOs and a white LED driving a dedicated boost converter, able to supply five LEDs in series with 85% average efficiency, plus other functions such as DC-DC converters or regulators for extra functions, battery charging, audio ADC/DAC and power stages. If we consider that the example application is powered by a typical Li-Ion 3.6V cell, it is possible to evaluate the IC dissipation when the power supply functions are switched on and the battery charger and audio functions are turned off. **Table 1** summarises the power supply system, whilst **Table 2** considers the power dissipated in each element of the PMIC.

Most highly-integrated PMICs are supplied in either BGA or QFN packages. The central area of the package is usually interfaced to the PCB ground plane in order to conduct as much heat as possible away from the device and keep the silicon at an acceptable temperature. In the case of a BGA, approximately 1/3 of the balls located in the centre of the matrix are utilized as ground connections. QFN packages have a large exposed metal pad located in the centre of the device that occupies more than 2/3 of the package area that can be 'connected' to the PCB using a suitable, thermally efficient, interface material.

These approaches provide a low thermal impedance path to ground, allowing good heat drain from the package. With this technique and an optimised PCB layout, the package thermal resistance ($R\theta JA$) can be as low as 40°C/W.

If we consider the previous example, with just the main processor regulators operating at maximum current, we can expect to see a silicon temperature elevation of approximately 90°C, bringing the silicon up to a maximum operating condition for an ambient temperature of 35°C. Although 25°C is a typical operating temperature, the internal temperature of a densely populated portable design might reasonably be expected to reach 35°C.

A high temperature operating mode will jeopardize portable device reliability and, at worst, lead to system failure. The need for

thermal management increases design complexity, requiring the designer to calculate and monitor, for each system power domain, the maximum current each regulator will have to supply and the maximum heat the PMIC will have to dissipate. This influences PCB layout and component placement as thermal failure may affect the operation and integrity of nearby components.

Even if the thermal management concerns are taken into consideration and kept under control by the designer, IC power supply functions may still dissipate too much heat. In this situation, other functions should be either switched off or at least switched into a 'heat save' mode with lower performance. For instance, during video playing, display brightness and audio sound level can be decreased to drop the PMIC temperature. Whilst main functions such as video, audio decoding and streaming performance are kept running as normal.

Depending on the system specification and architecture, one solution to help in solving thermal issues is the splitting of a large PMIC into several smaller ICs, or at least separating high dissipation regulators and putting them into a sub-PMIC. From a system standpoint this can make sense with each separate IC being dedicated to a given function. For a mobile phone that also integrates video and gaming functions, the designer may find benefit in supplying each module of functionality as an independent sub-PMIC controlled by the main processor.

If the main PMIC power dissipation is still too high, designers can consider putting other analogue user-interface related functions, for instance audio power stages and ADC/DAC, display supply and backlight, in a separate 'heat safe' sub-system IC to make sure they always operate at maximum performance.

Location on the PCB

In order to give users an improved video or gaming experience, the size and viewing quality of displays has greatly improved during the last few years. It is now possible to watch TV on a portable device with an Active Matrix OLED. As the sizes increase, the space available inside the handheld device increases and the geographical location of functions can be quite far away from the main PMIC.

The parasitic components related to the PCB layout will become more predominant. Let's consider the DC-DC converters in the previous example, supplying a processor located 50mm away from the PMIC and connected with a 5mΩ/mm track. The parasitic resistance will be 50mm x 5 = 250mΩ. Assuming that the thermal concerns are under control, the voltage drop in the parasitic resistance will be 250mV under 1A and 125mV under 500mA.

If we now consider the processor core power-supply range being 1.2V ±5%, as a worst case to operate at maximum clock frequency, 125mV drop in the tracks corresponds to about 10% of the operating voltage. This means that even for half of the maximum current, the voltage at the processor edge will be out of its operating range.

To overcome this issue, the designer has several options, these are:

1. Set the DC-DC converter output voltage higher than processor typical operating range to compensate for the drop. Considering dispersion between components; this is risky as the voltage will be uncontrolled and will depend on the processor operating mode and current.
2. Connect the converter feedback node as close as possible to the processor. In this case, the drop will be automatically compensated. However, the feedback pin is high impedance input, so input current will be very small (several nA) and the track could pick up a lot of noise. This can be overcome by careful attention to layout, but this is not always possible due to the track density.
3. Use of a separate sub-PMIC to supply this processor as well as related hardware. This makes design more flexible and simplifies layout.

Of course, this third option increases the Bill of Material (BOM) and the manufacturing costs slightly, but it may lead to higher reliability, a simpler design and improved design flexibility.

Other Considerations: Flexibility and Time-to-Market

In order to help illustrate this topic, we have discussed the advantages and drawbacks of a highly integrated PMIC versus a less integrated approach using sub-PMICs. This demonstration can be easily extended to other functions in the handset device, introducing a

CONVERTER	VOLTAGE (V)	CURRENT (MA)	COMMENTS
DC-DC 1	1.8V	800	Processor I/O
DC-DC 2	1.2V	1000	Processor Core
LDO 1	2.8	300	Analogue functions group 1
LDO 2	2.8	300	Analogue functions Group 2
LDO 3	1.8	200	Digital peripheral functions group 1
LDO 4	1.8	200	Digital peripheral functions group 2
LDO 5	2.5	200	Peripheral
WLED Boost	15V	20	5 LED with 3V forward voltage at 20mA

Table 1: *Summary of the power supply systems*

different level of integration with different partitioning in sub-systems.

With a highly integrated solution, any modification of system requirements identified by marketing will lead to heavy design modifications to each level of the design, including the software and hardware. Additionally, the modifications may affect the core of the system and make it risky from a business perspective.

Using a less integrated approach may lead to a more modular core design that is easier to maintain, modify and release with different options in a short timeframe. In today's very fast moving market, modular design might be a key factor to success and there is significant value in being the first to market with new, high value-added features.

CONVERTERS		POWER DISSIPATED (MW)
DC-DC 1	(1.8* 0.8)*((1/η0 – 1)	160
DC-DC 2	(1.2* 1)*((1/η0 – 1)	133
LDO 1 / 2	2 * (3.6 - 2.8) * 0.3	480
LDO 3 / 4	2 * (3.6 - 1.8) * 0.2	720
LDO 5	(3.6 - 2.5) * 0.2	220
WLED Driver	(15 * 0.2)*((1/η0 – 1)	530
TOTAL DISSIPATED POWER		**2243**

Table 2: *The power dissipated in each element of the PMIC*

A High Number of Options

In the handset, we cannot get away from using a highly integrated system for the core functions. The solutions described combine high levels of integration with high efficiency in a simple cost-effective design. However, in the feature-rich high-end handset market, other considerations such as reliability, heat dissipation or long PCB tracks may make the benefits of integration less clear. In addition, poor flexibility, long IC and chipset development cycle times, compared to the fast 'churn' rate of new handset designs, may make separate sub-systems a good alternative. They combine the advantages of integration and simple design with high flexibility and improved reliability. Assuming that the silicon vendors can provide cost-effective, size-effective and high-efficiency solutions, the handset designers will have a number of options when selecting the most appropriate solution. ■