LOOK BEFORE YOU LEAP INTO DIGITAL

Innovative Current Controlled Frequency Foldback enables analogue PFC controllers to deliver high efficiency across the load range, in addition to known strengths such as fast transient response and simplified circuit design

Tough ecodesign legislation such as the EU's Energy-related Products (ErP) directive demands extremely high energy efficiency for everyday items such as televisions, laptop and desktop PCs, fluorescent ballasts and LED-lighting drivers. To secure necessary approvals at the product level, such as the mandatory CE mark for goods sold in the European Union, new designs must meet targets for efficiency over a load range encompassing standby, partial and full-load conditions.

Moreover, designers are also under pressure to meet market demands for high standards of performance at a competitive price. Increasing feature integration in ICs controlling Power Factor Correction (PFC), which is mandatory in applications over 70W, can help to meet this requirement by cutting down on the number of power supply parts and reducing reliance on bulky over-specified components such as capacitors.

Active PFC compensates for the line current harmonic distortion otherwise caused by power supplies, which acts to increase heating and disturbances within the electrical network. As concern over energy efficiency has extended to cover operations not only in standby and reduced-power modes, but as well as at full power, the shortcomings of conventional PFC control operation have come under scrutiny. Traditional PFC controllers that operate in Critical-conduction Mode (CrM) tend to lose efficiency when the power supply is operating at light loads, such as when the appliance is in a standby mode.

Going digital. Or not

Some chip manufacturers have positioned digital PFC controllers to overcome this limitation. By converting the sensed analogue voltages into the digital domain and then applying signal processing algorithms, the digital controller is not constrained by linear behaviour and can synthesise an optimal output waveform for any load condition. The efficiency in various modes is dependent on the quality of the algorithms developed by the chip makers. Digital PFC controllers recently introduced to the market have also integrated features such as diagnostics and user programmability, enabled via a standardised connection such as I2C.

However, rumours of analogue's demise in favour of digital alternatives have proved to be exaggerated in the past. In this case, it may yet be too early to write off some key advantages of traditional analogue PFC controllers. Although manufacturers claim cost advantages over analogue controllers, particularly when considered at a system level, analogue controllers are available at a lower price than the latest digital alternatives. Prices within some digital device families have actually risen since first-generation products were introduced. In addition, integrated features such as protection circuitry and brownout detection in the latest analogue parts enable a competitively priced design using few additional external components.

The latest generations of analogue PFC controllers can deliver enhanced efficiency through innovations such as Current Controlled Frequency Foldback (CCFF), a new operating mode implemented in the ON Semiconductor NCP1611 and NCP1612. CCFF enables the PFC controller to maintain high efficiency over a wide load range, including light-load and standby operation in addition to higher load conditions. These controllers also implement enhanced features that improve fault handling and transient response and provide extra flexibility for designers by supporting different biasing scenarios.

Enhancing efficiency at all loads

In CCFF, the circuit operates in Critical-conduction Mode (CrM) under high-current

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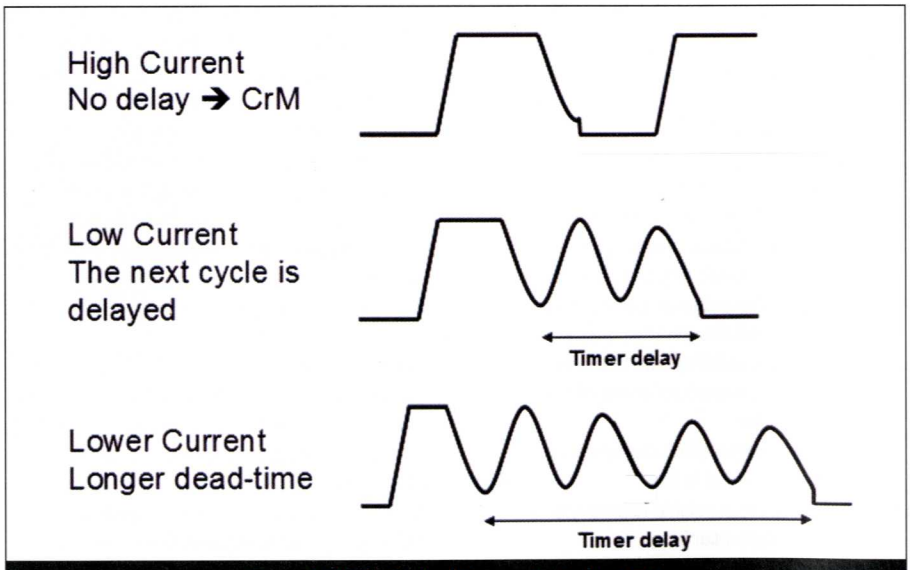

Figure 1. CCFF with dead time controlled by timer

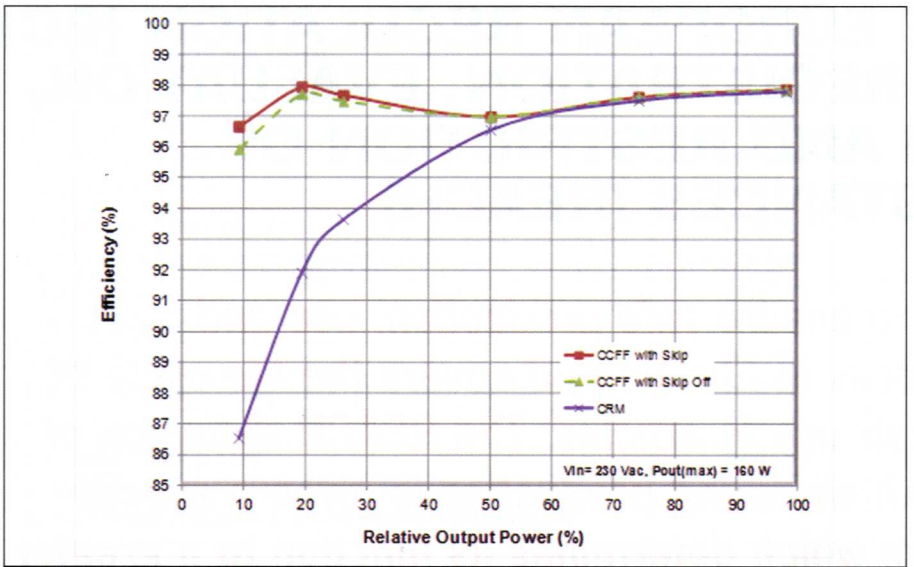

Figure 2. Efficiency comparison across load range, for CCFF and CrM controllers

conditions. At low current levels, which occur near the line zero crossing under heavy load and across the entire sine wave under light load, the controller enters a controlled-frequency discontinuous operation. A timer delays the start of the next cycle by inserting dead time until the time necessary for a ramp to rise from a sensed voltage representative of the input current up to an internally generated precision 2.5V "ramp threshold" has elapsed. Hence the dead time is longer for a lower input current. Figure 1 illustrates the principle of CCFF by showing the voltage across the boost MOSFET under varying load conditions.

The timer controls the dead time, rather than the switching period/off time. The foldback frequency is limited to a minimum of 20kHz when the current is zero. In this way, the controller is able to maximise efficiency at both nominal and light load. In particular, stand-by losses are reduced to a minimum. A further reduction in losses is achieved by delaying the point at which the MOSFET turns on until the drain–source voltage is at its valley. Valley switching also minimises generation of electromagnetic interference (EMI). A further advantage is that the system does not stall between valleys. Since the dead time is not affected by variations of the current-cycle duration, valley turn-on happens without hesitation.

The CCFF mode of operation contrasts with the conventional CrM, where the switching frequency increases with reducing load. At very light loads, a conventional CrM controller may enter a burst mode, producing audible noise. In contrast, the lower frequency of the CCFF controller is clamped above the audible frequency range, thereby preventing generation of acoustic noise.

Similar to the operation of Frequency-Controlled Critical Conduction Mode (FCCrM) controllers, internal circuitry allows near-unity power factor even when the switching frequency is reduced. In addition, a skip mode enables the PFC to achieve optimal efficiency at very light loads by skipping cycles near the line zero crossing when the current is very low. This avoids circuit operation when the power transfer is particularly inefficient. It should be noted that this mode introduces some distortion to the current waveform. For this reason, the skip mode can be inhibited for applications requiring superior power factor. Figure 2 compares the efficiency of a CCFF controller in skip and non-skip modes against conventional CrM control.

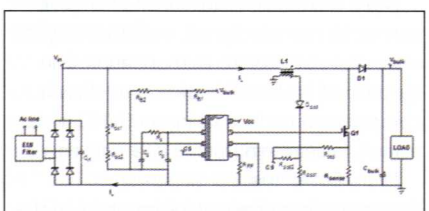

Figure 3. Boost PFC with CCFF controller

Enhanced controller features

Integrated fast line/load transient compensation further enhances PFC performance by avoiding excessive over- or undershoot caused by abrupt changes in the load or input voltage, such as at start-up. This problem is common in conventional PFC stages, owing to generally low loop bandwidth. In contrast, the NCP1611 dramatically speeds up the regulation loop when the output voltage falls below 95.5% of its regulation level. This function is enabled only after the PFC stage has started up to allow normal soft-start operation to occur. If the output voltage exceeds 105% of its desired level, Soft Over-Voltage Protection (Soft OVP) linearly decays the power delivery to zero. If the output continues to rise, the circuit immediately interrupts the power delivery when the output voltage reaches 107% of the desired level.

In addition, the controller is available in two versions, allowing designers to optimise the startup current depending on the operating voltage range. The "B" variant, which has a supply-voltage range up to 17V, is ideal for self-biased applications. It has low startup current allowing the use of high-impedance startup resistors, avoids the need for a large VCC capacitor, and helps shorten startup time. The alternative, "A" version has a low maximum startup level of 11.5V and can be powered from a 12V rail. It provides soft-start capability and is preferred in applications where the circuit is fed by an external power source such as an auxiliary power supply or downstream converter.

Also provided on-chip are a number of important protection functions, which can save the need for discrete protection circuitry. Integrated protection functions include a 2-level current limiting with the ability to turn off the power switch or enter a reduced duty-cycle mode if the bypass or the boost diode is shorted . Under-voltage protection, brown-out detection and thermal shutdown are also implemented.

The output stage contains a totem pole optimised to minimise the cross-conduction current during high-frequency operation. The high drive capability of the output circuitry allows the controller to be connected directly to power MOSFETs that have a large value of gate charge (Qg). Figure 3 shows a basic application schematic for a boost-PFC circuit controlled by the NCP1611.

Conclusion

Going digital is one way to optimise PFC efficiency for a wide range of load conditions. On the other hand, innovative PFC controllers taking advantage of proven analogue techniques can offer designers an easier and potentially more cost-effective solution. It's another good industry example of working smarter not harder when designing your PFC solutions. You don't need to be digital to be more efficient, you just need to be smarter.

TIM KASKE, ON Semiconductor