Diagnostics and troubleshooting of High Density Plasma Process issue causing MIM-Capacitors electrical failures occurred in an automotive ASIC.

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Introduction and motivation.
This work presents results of electrical failure analysis and troubleshooting in an automotive ASIC. An unusual pattern of yield drop-out at sort test occurred suddenly on product which has been in manufacturing for years; no other products were affected by the problem.
The pattern indicated strong wafer odd-even effect within a batch with up to 20% yield loss on the “bad” wafers and donut-shaped on the yield maps. Such wafers considered as underperforming for this particular automotive application and could not be sold to the customers. Therefore the gross yield dropped down to 49%. The failure analysis and 8D team were launched immediately to tackle the problem.

Description of approach and techniques.
The FA indicated that the yield loss was due to Metal-Insulator-Metal Capacitor (MIMC) electrical shorts. The reverse engineering analysis revealed that the shorts are associated with top MIMC plate metal recess – the local thinning of the AlCu – when coincided with VIA holes and causing MIMC dielectric punch through during VIA etch process. The effect was enhanced by the ASIC specific design using small MIMC area.
The “bad” wafers were statistically correlated then with particular HDP oxide deposition chamber (commercially available dual chamber HDP oxide deposition tool) which is used during the inter-metal dielectric formation on top of MIMC module. The chamber was instantly isolated from production and further troubleshooting was concentrated around the chamber and the HDP process, although, there was no direct indication regarding the process drift from the in-line SPC monitoring or after thorough hardware check.
According to the literature High-Density-Plasma-Chemical-Vapor-Deposition process (HDP-CVD) become a key process due to gap filling capability and provides high density low energy ions and higher quality films. Relatively high density of the plasma results in significant wafer heating during deposition step. Therefore wafer backside cooling with He is a must. Even He-cooled the temperatures as high as 400ºC have been reported along with distortion of the metal features.
To find out the “bad” HDP chamber mismatch and troubleshoot the process it was necessary to compare *the effective* wafer temperature in both good and bad chambers. Unfortunately, in this type of HDP tool wafer temperature control is not available – this is the major disadvantage for all users of the tool.
Based on our previous experience the “thermal sensitive film stack” consisting of Ti and AlCu films deposited on Si substrate covered with SiO2 has been applied to do the in-process wafer temperature estimate by means of sheet resistivity change.
The diagnostic wafers were subjected to HDP deposition process in each chamber. The calculated average of *the effective* temperature in the “bad” chamber was found at ~ 510ºC, this makes it ~30ºC above the “good” chamber, also Rsh range (thermal field uniformity) was 3 times higher. Further experiments confirmed that the major parameter to improve the thermal field uniformity in the chamber is cooling He pressure balance in the inner and outer zone - these are two independently controlled circuits. Standard BKM settings have been working fine for both chambers in the past. But because of an unknown hardware drift the pressure in the inner zone needed to be increased by ~ 20% in order to achieve uniform cooling.
Since the change has been implemented in the recipe the effective temperature matching and uniformity improve between the chambers and uniformity improvement has been achieved.

Results/Conclusions/perspectives.

To resolve a complex yield issue which was found related to the Inter-Metal-Dielectric HDP processing we have found the method to detect and troubleshoot the chambers process mismatch using wafers with thermal sensitive film stack. Thermal field gradient across the wafers appeared to be another important parameter and when not well controlled may cause significant films stress mismatch leading to AlCu film stress-induced defects and, in this case, MIMC electrical shorts.

The method, suitable for HDP or another process temperature diagnostics, and MIMC failure mechanisms are being discussed.