Handling ESD in USB 3.0

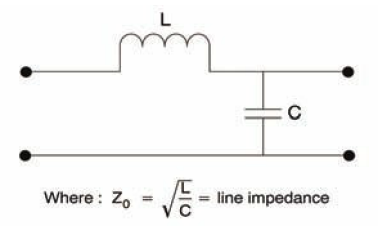
Jeremy Correale at **ON Semiconductor** looks at ESD protection and impedance matching for USB 3.0 interfaces for high-speed data transfer

USB 3.0 can achieve data transfer rates that reach 5Gbit/s - over 10 times faster than USB 2.0. This is helping to satisfy the massively increasing consumer demand to access and to share high-quality content, such as video, music and photos. The chipsets that support USB 3.0 interfaces have shrinking process geometries and package sizes so the data rates can be met while also enabling the development of smaller, lower power, feature-rich portable media products. The combination of super-fast data lines and small geometry devices significantly increases product susceptibility to electro-static discharge (ESD).

In order for USB 3.0 to support a 5Gbit/s data rate, two differential data pairs (SuperSpeed Tx and Rx) have been added to the legacy USB 2.0 data pair (D+ and D–). In addition, the chipsets supporting USB 3.0 are based on semiconductor processes as low as 22nm. The increase in frequency, compared to USB 2.0 transmission, creates a strict impedance matching window that must be met when placing an external ESD protection device on the SuperSpeed lines.

Any small amount of capacitance added to the signal line can change its impedance and thus degrade the overall signal integrity of the transmission. Figure.1 shows a circuit representation of a lossless transmission line where the nominal impedance is represented by Z0.

$Z0 = \sqrt{(L / C)}$ = line impedance



This transmission line model can be applied to a data line present in almost any modern high-speed serial interface. The model can also be used to evaluate the effect of placing an ESD protection device onto the data line (or lines). In its most basic form, an ESD protection device can be viewed in the form of a Zener diode placed on the data line it is to protect.

This diode has an associated junction capacitance, along with a small amount of series inductance from the internal bond wires in the package, which become parasitic to the data line as shown in Figure 2. Since the inductance of a typical wire bond in an ESD protection device is typically ≤1 nH and the capacitance of the ESD protection element must be ≤1 pF, the impedance of the inductors in Figure 2 will be well below the impedance of the capacitances for a 2.5GHz USB 3.0 signal, inductance can be ignored in this discussion.

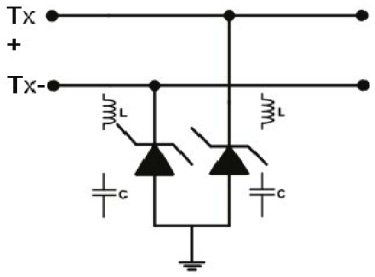


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Figure.1 (left): Lossless Transmission Line - Equivalent Circuit

Figure.2 (right): ESD Protection Device Parasitic Model

As voltage on the data line changes, a small amount of current is needed for charging the parasitic capacitor. At high frequencies, where the voltage on the signal line is changing rapidly, this extra charging current can be considerable, thus reducing current flow along the data line. This reduction causes a slight change in impedance of the signal line and affects the amount of power it transfers.

If the power transfer loss is excessive, degradation in the data line signal integrity will occur. The USB 3.0 specification permits a 1.1 pF maximum for parasitic capacitance (this includes any capacitance in the system that is external to the USB controller).

ESD protection devices represent only a fraction of the external capacitance in the system. Therefore, when choosing such devices, the engineer should always keep in mind that lower capacitance of the protection device not only preserves signal integrity on the data lines, but also allows a greater capacitance budget to be worked with in the downstream system.

Almost all ESD protection device suppliers specify the junction capacitance at 1MHz. However, a few will do this for higher frequencies too. A capacitance measurement across a range of frequencies should be considered in order to get a good representation of the actual device capacitance in a high-speed application. In USB 3.0, this equates to a measurement at the fundamental frequency of 2.5GHz and its third harmonic frequency of 7.5GHz.

As with any capacitor, its capacitance will vary over the frequency at which it is used due to its own parasitic resistance, called the equivalent series resistance (ESR). The impedance of the capacitor will stay capacitive with low ESR at lower frequencies and continue to decrease until the capacitors resonance frequency is reached. Once resonance is reached, the impedance of the capacitor becomes inductive as the ESR increases.

Signal loss due to reflection at the protection element is another important parameter - this is often expressed in terms of return loss. Return loss measures how much energy loss is incurred by the incident wave reflecting off of the device under test. The lower the ESD protection device's return loss is, the fewer reflections will be witnessed - translating into more of the signal being transmitted. Many ESD protection devices on the market will be subject to a dramatic increase in parasitic capacitance above 5GHz, due to the impedance reaching resonance and going inductive.

It is critical for engineers to understand the key parameters of ESD protection devices that have an influence on the impedance path of the data line. The combination of advanced ESD protection devices with good board layout techniques allows engineers to benefit from incorporating protected USB 3.0 interfaces into their designs without compromising signal integrity.

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