Description
AIP302s is a Single Event Latch-Up (SEL) Immune Digital Gate Library implemented in ON Semiconductor ONC18 process technology. ONC18 provides 180nm 1.8V CMOS with a number of variants to support analog, mixed-signal and dual gate oxide. The library is usable in most ON Semiconductor ONC18 process variants extending the library’s use to a large number of applications.

The library utilizes radiation hardened by design (RHBD) layout techniques (both well and substrate ties) to ensure latch-up immunity. For the best density possible, the library does not utilize RHBD techniques for the NMOS poly gate. Therefore, the AIP302s library does not increase total ionizing dose (TID) beyond the capabilities of the ON Semiconductor process technology. Anatrix does offer a digital gate library, AIP301, with TID performance beyond 300KRad.

The library contains the following views: schematic, symbol, layout, verilog, .lib, .lef and netlist.

Features
- Single Event Latch-Up Immune
- 1.5X area penalty vs standard gates
- Place and Route Capable
- 250pS Clock to Q DFF

Logic Gates Included
1X, 2X and 4X drive:
  - AND2, AND3, AND4
  - NAND2, NAND3, NAND4
  - OR2, OR3, OR4,
  - NOR2, NOR3, NOR4
  - XOR2, XNOR2
  - MUX2
  - AOI22
  - OAI22
  - ADDH, ADDF
  - DFF, DFFR, DFFSB, DFFE

1X, 2X, 3X, 4X, 6X, 8X, 12X, 16X, 20X drive:
  - INV
  - BUF

Support Cells:
  - Antenna diode
  - TieHigh, TieLow
  - FILLER (1, 2, 4, 8, 16, 32, 64 track widths)
  - CAP_FILLER (2, 3, 4, 8, 16, 32, 64 track widths)

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