IMPACT OF VIA INTERACTIONS AND METAL SLOTTING ON STRESS INDUCED VOIDING

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ABSTRACT

Stress induced voiding was investigated for a 0.13 um Cu/low-k interconnect process. The focus of our study was on the "hump" failure mode using a statistical approach to both the design of the vehicle and the data analysis. The TTF was studied with respect to geometrical aspects of the lower metal level, insertion of a dummy via, via arrays and metal slotting for long via chains.

[*Keywords*: Stress Induced voiding, SIV, vacancy diffusion, diffusive buffer, via array, metal slots, dummy vias, geometry]

INTRODUCTION

Stress induced voiding continues to be one of the top reliability concerns for interconnects. The reliability of 0.13 μm node Cu/low-k interconnects was studied with a focus on the early mode of stress induced voiding (SIV) failures for vias making contact to wide bottom metal patterns. In previous studies, SIV has been observed under vias connected to wide bottom Cu metal lines [1], and within vias connecting to wide top metal [2]. The two different modes of failure depend on the location of a "reservoir" of available vacancies for voiding: Wide top metal which leads to via "pull out" failures [3], and wide bottom metal which leads to the "hump void" [1], [2], [4]. For this study, the latter failure mode was chosen.

In dual-damascene technology, the combined effects of the absence of a conductive shunt layer at the via-bottom/Cu/SiC intersection, the high Cu diffusivity path at the SiC/Cu interface, stress gradients under the via [5], and a small critical void volume for failure [6], can enable voids to nucleate below the via and easily grow to a fatal size. When identical test structures are serially connected, the time-to-failure (TTF) is driven by the earliest failure mode and the TTF distribution is known to follow "weakest-link" statistics [7].

The SIV failure mode studied in this paper is due to the nucleation and diffusion limited growth of voids underneath the via. As such, the geometry of the structures is expected to have an impact on the TTF through the self-diffusion length of Cu given by $L = 2\sqrt{Kt}$, where $K = DB\Omega/k_BT$, and D is the atomic diffusivity, B is the effective modulus of the Cu dual-damascene stack, Ω is the atomic volume, k_B is Boltzmann's constant, and T is the local temperature [8], [9]. Some early initial work on the geometrical dependency of SIV failure has been done by von Glasow *et al* [4], including via CD dependence, block area, and via extension. In these studies, a different interconnect integration was stressed at higher (lower stress) temperatures. Similar geometries were used in our study of the 0.13 μm Cu dual-damascene low-k interconnect stack.

Addition of redundant vias is the current industry practice for improving the reliability of Cu interconnects for both SIV and EM failure. Previous work has shown that, indeed, additional vias do improve the reliability [10]–[12]. However, no study has investigated the physical impact of the redundant via on the reliability over and above the simple electrical parallel redundancy effect. Some initial modeling of the stress impact of additional vias has been reported by Huang *et al* [13], however, no experimental confirmation was provided. This study provides experimental data which shows the reliability impact of a non-trivial interaction between vias.

EXPERIMENTAL

A wafer level test vehicle was subjected to thermal stress, applied through high temperature storage (HTS). The temperature dependence of the TTF was confirmed by HTS at 12.5°C increments from 150°C to 300°C (not shown here) to establish the maximum acceleration-stress temperature of 175°C, and all further HTS treatments and TTF data was obtained using 175°C. Wafers were subjected to HTS with each cycle following a electrical probe readout, with a total of five to eight cycles for most experiments. Failure Analysis (FA) was employed after HTS was complete, and SEMs verified the under-via "hump" void characteristic of early failure.

The test vehicle was designed to determine the failure rate for a via relative to interconnect geometries, returning a part per million failure rate level for each of the sixty four via chain structures in a fabrication cycle. In order to accurately predict the low statistical failure rate that may be encountered for reasonable HTS times, a very large via chain length was used. A typical chain incorporated 3500 - 300,000 vias, which led to an average of greater than 5 million vias per experimental data-point. Each segment of the via chain structure consisted of a 0.2μm (minimum width) upper metal line connected to a consistent type of lower metal structure. For this study, five different basic lower metal patterns were chosen to study: a horizontal metal block, a vertical metal block, a square block, and an "H"-shaped structure. Extensions were added to both sides of the horizontal, vertical and square block to connect the via to the block body. A design of experiments (DOE) approach was utilized to choose variations that were applied to each of the five geometrical structures (as shown in Fig. 1: The extension width (EW), extension length (EL), end of line overlap (EOL), block width (BW) and block length (BL) of the lower metal.

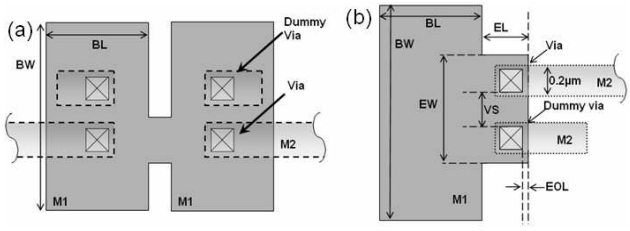

Fig. 1. Stress induced voiding test structures consist of two types of via/M1 interface. (a) Via landing in center of large metal block, and (b) via contained within extension. For type (a), the structure used in this paper is an "H" shaped structure. For type (b) many different configurations of BL, BW, EL, EW, EOL, and VS were investigated.

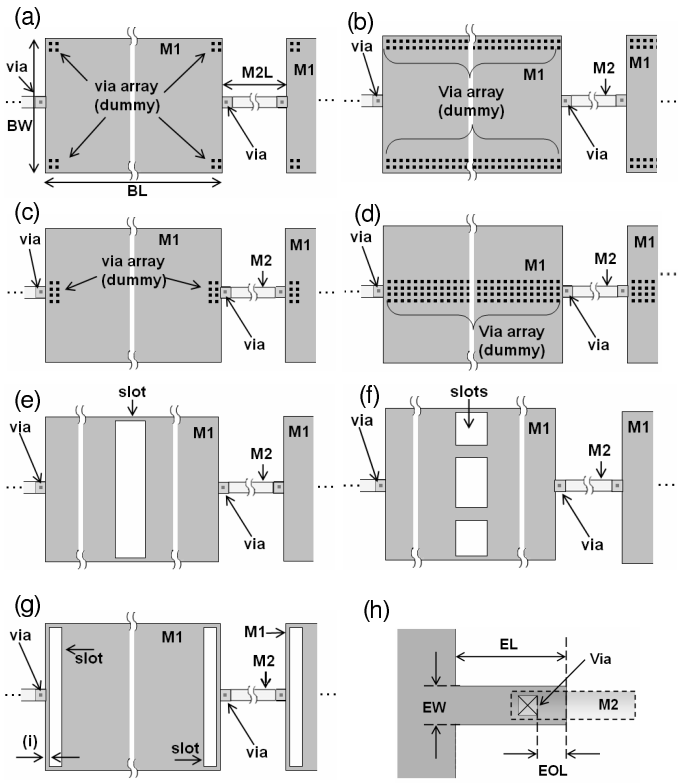

Fig. 2. Via array and slotting structures: (a) small four via array at the outside edges, (b) large via array spanning the entire length of the block, (c) small eight via array in front of the active via, (d) large via array in front of the active via, (e) square segmented slots in the center of the block, (f) rectangular slot in the center of the block, (g) long rectangular slots in front of the active via, (h) schematic of the via-extension parameters: extension width (EW), extension length (EL), and end-of-line overlap (EOL). Also indicated is (i) the width of the resultant M1 line due to the long slot near the via.

A separate via mask was used to study the effects of a redundant dummy via at the minimum shunting distance from the electrically connected via. Other via masks were used to apply either a large or a small via array in conjunction with the single via in a horizontal block. The via array combinations as shown in Fig. 2(a-d) were either placed at the edges of the block or directly in front of the electrically active via. The small via array consisted of four vias while the large via array spanned the entire length of the horizontal block.

To study the effects of lower metal slots on the via failure rate additional lower level metal masks were used to introduce either a long rectangular or a series of small square slots into the horizontal block structure. The position of the slots relative to the electrically active via are shown in Fig. 2(e-g). In one case either the long rectangular or square segmented slot was place in the center of the block away from the active via. For comparative purposes the long rectangular slot was also placed directly in front of the electrically active via.

To emulate the typical mechanical stresses encountered in Cu/low-k BEOL stack, the test vehicle process flow included the formation of low-k interconnect dielectric layer above and below the via chain metal levels under study, as well as upper dummy metal layers. Final passivation layers were included along with the Al bond pad formation steps in order to provide electrical readout of the test structures. The design of the test structures was of a Kelvin type in order to accurately measure and verify failures.

TABLE I
TTF (10%) FOR VARIOUS GEOMETERIES

Area (μm^2)	TTF (hrs) for 10% ($t_{0.1}$)	EL (μm)	EW (μm)	BL (μm)	BW (μm)
1	2.5×10^4	0.29	0.2	1.0	1.0
1	2.4×10^3	1.00	0.2	1.0	1.0
106	157	1.15	0.2	10.3	10.3
360	79	0.70	0.2	30.0	12.0
360	66	0.50	0.2	30.0	12.0
360	9	0.29	0.2	30.0	12.0
360	no fails	4.50	0.2	30.0	12.0
360	48	0.29	1.4	30.0	12.0
360	49	0.50	1.4	30.0	12.0
360	no fails	4.50	1.4	30.0	12.0

Data Analysis Methodology

Failure criteria and test structure design play concomitant roles in revealing the mode of failure. Long via chains, or long metal lines can be coupled with an open-circuit failure criteria, a resistance shift ΔR, or an absolute resistance change. Long metal lines, or via chains with small bottom metal can be coupled with a ΔR failure criteria, revealing the long term risk due to void growth within the line in conjunction with weak points under the via, both of which can lead to large resistances. On the other hand, long via chains with wide bottom metal are insensitive to homogeneous voiding within the metal and are dominated by under-via voiding which leads to an abrupt open circuit. In addition, long lines increase the probability that there exist "defects" within the structures that can act as void nucleation and growth points (triple-points, "contamination patches" [14], initial voids, etc.). Thus, long via chains sample the worst-case-scenario, and open-circuit failures follow statistics given by the weakest-link or Weibull statistics [7], [15], [16]. Thus, the failure criteria used in this study was an open-circuit failure. Also, all results are presented on a Weibull scale, with 95% confidence intervals calculated using standard methods [15].

RESULTS

As shown in Table 1, the impact of the block area on the SIV failure rate is dependent also on the dimensions of the block and via extension (EL, EW, BL, and BW). For small areas ($\sim$ 1 μm^2), $t_{0.1}$ can be varied by an order of magnitude by extending the via from the block. For an intermediate and larger block area (106 - 360 μm^2), but similar extension, $t_{0.1}$ is further reduced. EOL and VS (as indicated in Fig.1(b)) did not have an experimentally discernable impact on the TTF of structures studied in this paper. A block area of 360 μm with a shorter extension (EL = 0.29 μm) is very sensitive to void nucleation and growth and is used for further studies of other geometrical modifications.

Fig.3 shows the CDF of a "horizontal block" structure with dimensions (BL=30, BW=12, EL=0.29, EW=1.4, EOL=0.055) with via position as shown in Fig.1(b), comparing single via ($\diamond$), to dual dummy via ($\circ$). Approximate Weibull distribution fits of the earlier failures are shown with dotted lines. As can be seen, the CDF shows a flattening at higher HTS times ($>$ 168 hrs), which is roughly

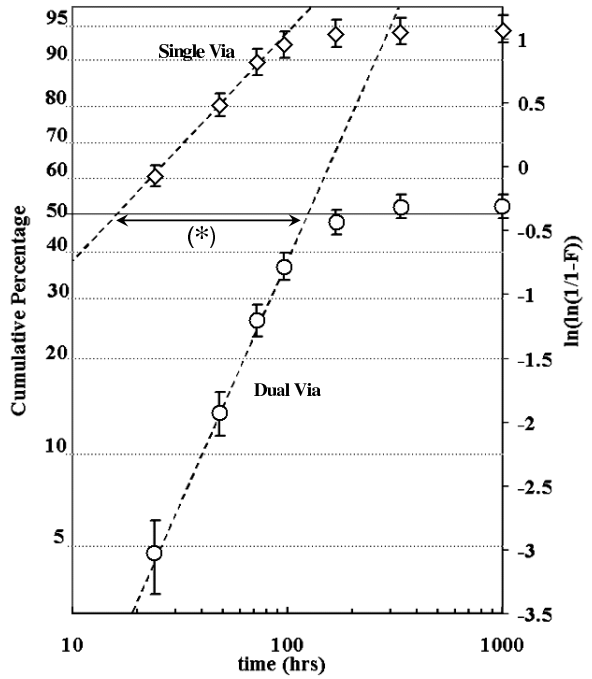

Fig. 3. CDF plot of structure with dimensions BL = 30, BW = 12, EL =0.29, EW = 1.4, and EOL =0.055, comparing single via (⋄), to dual dummy via (○). Dotted lines are approximate Weibull fits to the early failure data. Note the pronounced decrease in the failure rate at about 168 hrs. The difference in MTTF ($t_{0.5}$) is shown (∗), which is on the order of 90 hrs.

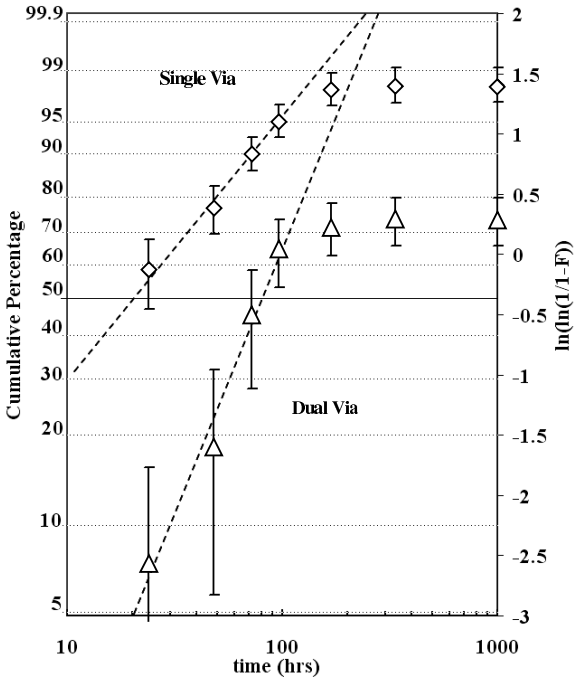

Fig. 4. CDF plot of H-shaped structure (BL =2.5, BH=20), comparing single via (⋄), to dual dummy via (△). Dotted lines are approximate Weibull fits to the early failure data. Note the pronounced decrease in the failure rate at about 168 hrs.

equivalent for both structures. The slopes for the linear portion of the CDF are not equivalent. Extrapolation to $t_{0.5}$ reveals a difference $(*)$ of roughly 90 hrs.

The CDF for an "H"-shaped structure is shown in Fig.4, with dimensions (BL = 2.5, BW = 20), and layout shown in Fig.1(a), comparing single via (⋄), to dual dummy via (△). Again the dual via structure shows an increase in the TTF as compared to single via. Approximate Weibull fits to the earlier failures are shown. Note the flattening of the CDF at times larger the 168 hrs, similar to the result in Fig.3. The saturation levels for the single via in each case are similar within experimental errors, however, the dual via shows a difference in the saturation level. The difference in $t_{0.5}$ for the "H"-shaped structure is less than for the "horizonal block."

In Fig.5, the results from various via array configurations is shown. The control sample of single via with no array is shown (⋄), along with the small array in the corners of the block (○), the long via array that spans outside edge of the block (△), and the small (8) via array directly in front of the electrically active via. The large via array that spans the center of the block (as shown in Fig.2(d)) is not shown due to zero failures during all intervals of testing (up to 1000 hrs). All via array structures have identical dimensions in microns (BL=30, BW =12, EL =0.29, EW = 1.4, EOL =0.055). Failure rates for all structures begin to saturate after the 20 hr readout, with 168 and 500 hr readouts being similar in magnitude.

CDF plots exhibited in Fig.6 are for Metal slotting configurations shown in Fig.2(e-g). The sample (⋄) with no slot has the highest failure rate, followed by segmented slots in center of block (○), long slot in center of block (△), and long slot at edge of block near the via (□). Absence of curvature is due to early termination of the HTS experiment at 20 hrs (all HTS readout points are $<$ 168 hrs). The dimensions of the structure studied here (BL=30, BW =12, EL =0.29, EW =0.2, EOL =0.055) has a narrower EW, as compared to the via array test structure. The failure rate for the control sample with the same dimensions as the via array structure was determined to be identical in magnitude. This sample, however, did not show the difference in performance with respect to slotting due to high initial failure rates.

DISCUSSION

Currently accepted models of SIV treat the TTF as dependent on the diffusion of material away from the via, not accounting for the energy of void nucleation or dynamic stress relaxation [1], [13], [17], [18]. The results shown here reveal that the process of SIV failure is much more complicated, and these features can be probed with the alteration of geometrical factors. As cited, the addition of a redundant via can act as a stress modifier of the original via [13], which will reduce the vacancy diffusion to the via. However, the reduction in stress can also modify the void nucleation probability. Also, currently accepted models for SIV in Cu do not take into account the effect of additional void nucleation elsewhere within the local area of the via, and the impact this will have on the failure dynamics.

Void Nucleation and Growth

The process of void nucleation for SIV is not well understood. It is believed that processing variations [19], microstructure, oxidation or "contamination patches" [14], [20], [21], local delamination [22], initial plastic deformation [23], grain-boundary sliding, all play a role in the probability for void nuclei. In the ideal case (no processing "defects") one possibility that still remains for a polygranular interconnect is stress concentration due to triple point grain boundary intersection with interfaces. Nevertheless, in general, void nucleation

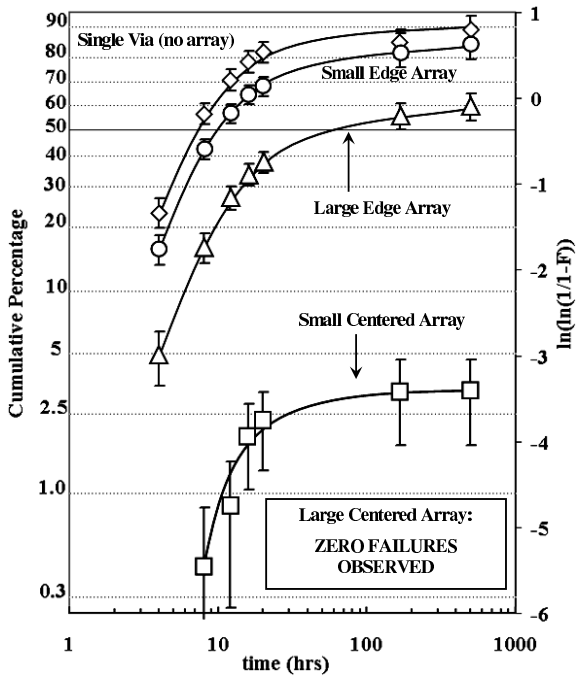

Fig. 5. CDF plot of via array data: Single with no array (⋄), small array in the corners of the M1 block (○), large via array on outside edge of M1 block (△), and small via array in front of electrically active via (□). The large via array spanning the center had zero failures during experiment. All structures had dimensions (BL=30, BH=12, EL=0.29, EW=1.4, EOL=0.055). Note the decreasing failure rate as a function of time. Trend lines have been added for clarity.

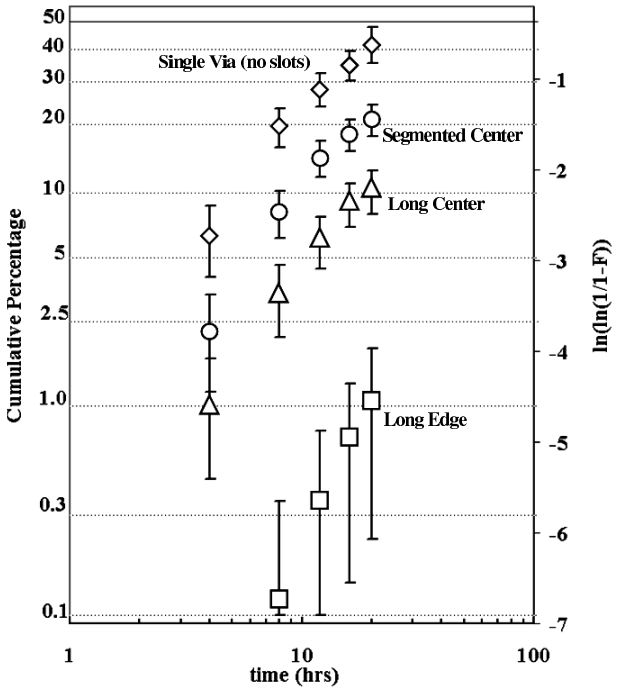

Fig. 6. CDF plot of experiment with metal slots. Control sample (⋄) with no slot has the highest failure rate, followed by segmented slots in center of block (○), long slot in center of block (△), and long slot at edge of block near the via (□). Absence of curvature is due to early termination of experiment (all HTS readout points are $<$ 168 hrs).

is driven by the competition of the tensile stress with the surface-stress and surface energy of the void embryo [24]–[27], leading to a critical stress threshold for void nucleation. It has been assumed that the presence of flaws within the polygranular interconnect may lower this threshold to the point where void nucleation is instantaneous for practical considerations for a high enough stress. In Fig.5 we can see the extinguishing of the SIV mechanism through the addition of the large dummy via array in the center. Also, observations of the ΔR showed no appreciable shifts during the period of HTS testing which would be indicative of partial via voiding. This can only be explained by the lowering of the stress to the point of being below the critical stress for void nucleation.

The impact of void nucleation on the failure rate should be seen in the wafer to wafer variance for structures that exhibit stresses near the critical threshold for void nucleation. Structures well above this threshold should nucleate quickly, early in the HTS cycle. Structures well below this threshold should remain robust to SIV failures. In the intermediate stress regime, the devices should be very sensitive to fluctuations in the particular microstructural conditions which affect the nucleation rate. When considering SIV nucleation for modeling purposes, the nucleation rate must be convoluted with the void growth rate to obtain an expression for the total population of critical voids in an experimental sample. This additional factor should be manifest in the DTTF and TTF, when various geometrical and processing factors are varied in experiment.

The solution of the diffusion equation for a single void under the via is given by Zhai & Blish [9], for different interconnect geometries. In their model, the TTF is dependent only on the boundary conditions of the interconnect, and the experimental variance in the TTF is only dependent on the critical void volume through variations in via diameter, and other material parameters (effective modulus, effective diffusion constant etc.). As time progresses, the void growth slows due to the relaxation of stress and equivalently, the depletion of vacancies, with a final void saturation point being reached at long times. Void saturation does not impact the TTF for hump voids, however, since after a critical void size is reached, the saturation of the void growth is not experimentally detectible. This result, however, does show the variance related to initial via diameter, and boundary conditions. The impact of via diameter has also been discussed by Ogawa et al [1], as having an impact on the TTF through the stress-gradient modification due to larger diameter via.

The experimental reduction in failure rate as a function of time, as seen in Figs. 3-5, is most likely due to the interaction of the diffusion of vacancies with other stress fields due to additional vias, or voiding in the interconnect and the subsequent stress relaxation. It is well established that void nucleation will occur at high triaxial tensile stress regions more-or-less evenly distributed in wide lines [28]. For the via structure in Fig. 3, the addition of the via acts as a stress modifier. In the absence of a stress modification, the additional via would "share" the vacancy volume of the block with the electrically active via during the period of void growth. The expected difference (as indicated by $(*)$ in Fig.3) in the TTF would be on the order of a factor of 2 increase. In fact, the increase in the TTF is actually much larger, indicating that the stress is markedly reduced by placing the dummy via next to the electrically active via.

The void growth process is shown schematically in Fig.7. The void is a site of flux divergence, that is, material flows away from the void and is deposited elsewhere in the interconnect. If the interface

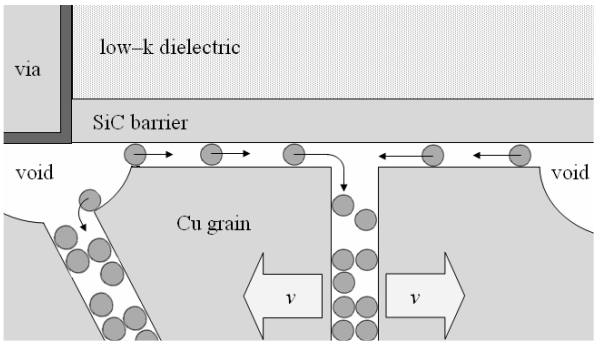

Fig. 7. Stress relaxation is facilitated by flux divergence, and subsequent redistribution of Cu throughout the interconnect. Interfaces between the SiC cap provide high diffusivity paths for material to deposit in grain boundaries. A reduction in stress due to the "jacking velocity", v, is one possible mechanism for stress relaxation

diffusion is high compared to the grain-boundary diffusion, the rate limiting factor in stress relaxation lies in the grain boundary diffusivity [29]–[31]. Thus, material from the void region can be deposited far from the via in order to relax the tensile stress. The rate at which this stress is reduced is called the jacking velocity, v, which is the rate at which material is plated on the grain boundary [27]. This process is assisted by flux-divergence due to other sources, such as additional voids in the interconnect. Cu may also plate on the SiC/Cu and Ta/TaN interfaces also reducing the stress in the interconnect.

Multiple Vias

For via arrays, the additional vias act as nucleation sites for voiding, which will reduce the stress in the block and therefore the vacancy concentration available for void growth. The via arrays will also effect the stress gradient near the electrically active via, slowing the void nucleation and growth rates. The additional vias will also simply act as stress reducers for void nucleation as shown by the complete elimination of failure for the large via array in the center of the block. The delay of the onset of failure can be caused by the reduction in stress from void nucleation or stress reduction far from the electrically active via. This can be seen in the failure rates of configurations (a) and (b) shown in Fig.2, with CDF in Fig.5. The most striking example is the reduction in the failure rate between the large outside array and the control sample (single via).

The small array (Fig.2(c)) placed in front of the electrically active via does not sufficiently suppress the void nucleation and growth rate. This indicates that the redundant vias do not act as diffusive "blockers" to the source of vacancies within the block. Also, the presence of the additional vias does not act as a sufficient stress reduction for void nucleation. If the number of vias is increased past a certain threshold, however, the failure is extinguished. Due to the fact that there are zero failures, it is not believed that the via array acts as a preferential site for void nucleation (and hence a "vacancy sink") since with the large sample sizes at least one failure should have been seen in 500 hrs of HTS.

Metal Slotting

Metal slotting results show a different behavior than the dual via and via array. The presence of a long slot in front of the via does not completely suppress the void nucleation and growth for the block areas studied (360 μm). This indicates that the local vacancy volume is high enough for SIV in spite of the diffusive blocking action of the long slot. The slots in the center of the block also have an effect on the TTF, through the modifications of the boundary conditions for SIV. In one case, for the long slot in the center (Fig.2(e)), the total vacancy volume is reduced and the TTF is increased (See Fig.6, the long center slot ($\triangle$)). For the case where the segmented slot is introduced to the center (shown schematically in Fig.2(f)), the failure rate is significantly higher due either to the increase in the volume of vacancies or a higher degree of stress within the block. As compared to the single slot, the additional "straps" of Cu may provide additional tension to the block.

Statistics of Failure

The differences in the shape parameter (slope of Weibull plots in Fig. 3, and Fig. 4) between the single and dual via is not well understood. This discrepancy could be simply due to the fact that the first readout point did not capture the earliest single via failures which would indicate a larger slope. Nevertheless, all of the results show that a simple Weibull is not sufficient to model the statistics of SIV failures due to the curvature and eventual saturation of the failure rate.

Often, curvature in the Weibull plot is attributed to a limited failure population (LFP) model, which states that a limited sub-population of the units are susceptible to failure, while the remaining units are more robust. In order to investigate this behavior, sub-populations based on initial resistance, via diameter, and wafer level binning, were performed to find a correlation with a susceptible sub-population. It was discovered that for every sub-population considered, the failure rate decreased as a function of time for times greater than 168 hrs. Also, within the sub-population, the long lasting units were evenly distributed across the sub-population. Also, the HTS was performed at different times for different experiments indicating that the curvature is not a systematic artifact of the HTS setup. The reduction of the failure rate as a function of time appears to be a universal feature of the data. This curvature can be taken into account in a formulation of the Weibull which has a time-dependent scale parameter $\eta(t) = \eta_0 f(t)$ indicating a change in the generalized "stress" leading to failure [32]. The precise form of $\eta(t)$ depends on the via interactions, void saturation, and other factors.

SIV failure rates are highly sensitive to process variation, experimental variations, and inherent randomness due to microstructure and material defects. Most of these variations "average" over experimental splits, and conditions. However, a few considerations must be made in the data analysis to account for variations that do have a strong impact on the TTF. A primary source of variation in the TTF is the initial via cross-section at the point of failure. Larger via cross-sections imply a larger critical void size, and a smaller initial resistance. In order to account for this wafer-level variation, via chains within experimental partitions were subdivided into populations with similar initial resistances.

Another, slightly less crucial, source of variation is the temperature variation in the accelerated test. The relative change in the MTTF with respect to to temperature, $\delta(TTF)/\delta T$, can be large depending on what temperature the HTS test is performed. That is, near the maximum acceleration temperature, the gradient is small, however, at points off of this maximum, the gradient can become very large leading to large experimental fluctuations in the TTF. Also, due to the stress relaxation in the metal film stack that occurs during the test, this maximum stress temperature will actually change with time. As the

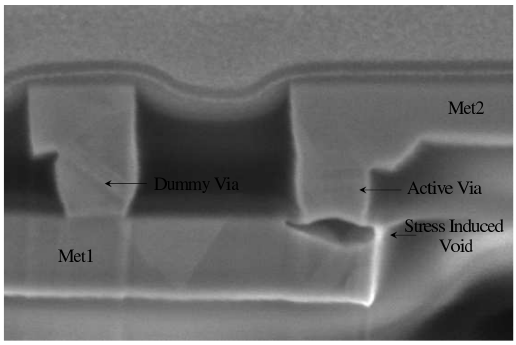

Fig. 8. SEM image of a stress induced void from experiment. Dummy via, and electrically active via are shown. Characteristic "hump" void seen under electrically active via. This is the failure mode associated with abrupt open failure.

stress relaxes due to diffusion, the maximum acceleration temperature moves to lower values.

Failure Analysis

Passive voltage contrast was used to establish the location of the void, and FIB cross-sectional analysis was done to confirm the morphology of the failure mode. In Fig. 8 a typical SIV failure is shown.

CONCLUSION

Our work shows that there is a significant interaction between the vias with respect to SIV that cannot be simply represented by the combined reliability of each single via. Furthermore, the interaction may be manifest in the sharing of vacancy volume, a stress modification, or a probabilistic void nucleation and subsequent sink for vacancies. Also, vias do not act as diffusive "blocks" for void growth. Additionally, our work shows that slots do not act as vacancy attractors or sinks but merely as diffusive blocks.

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