ON Semiconductor

PRODUCT BULLETIN
Generic Copy

16-AUG-2005

SUBJECT: ON Semiconductor Product Bulletin #15001

TITLE: Standoff Height Dimension Change for the 16 Lead SOICW EPAD Package

EFFECTIVE DATE: 16-AUG-2005

AFFECTED PRODUCT DIVISION: Analog Power Products

FOR ANY QUESTIONS CONCERNING THIS NOTIFICATION:
Contact your local ON Semiconductor sales office or Peter Neumann
<jtmwdj@onsemi.com>

NOTIFICATION TYPE:
ON Semiconductor considers this change approved unless specific conditions of acceptance are provided in writing. To do so, contact your local ON Semiconductor sales office.

DESCRIPTION AND PURPOSE:

ON Semiconductor will be reducing the standoff height dimension to 0.00 - 0.10 mm, of the 16 lead SOICW EPAD package to improve solderability. This is in accordance with industry practices. Device reliability and performance will not change.

AFFECTED DEVICE LIST

PART
NCV51411PWR2
NCV8501PDW100
NCV8501PDW100R2
NCV8501PDW25
NCV8501PDW25R2
NCV8501PDW33
NCV8501PDW33R2
NCV8501PDW50
NCV8501PDW50R2
NCV8501PDW80
NCV8501PDW80R2
NCV8501PDWADJ
NCV8501PDWADJR2
NCV8502PDW100
NCV8502PDW100R2
NCV8502PDW25
NCV8502PDW25R2
NCV8502PDW33
NCV8502PDW33R2
NCV8502PDW50
NCV8502PDW50R2
NCV8502PDW80
NCV8502PDW80R2
NCV8502PDWADJ
NCV8502PDWADJR2
NCV8503PW25
NCV8503PW25R2
NCV8503PW33
NCV8503PW33R2
NCV8503PW50
NCV8503PW50R2
NCV8503PWADJ
NCV8503PWADJR2
NCV8504PW25
NCV8504PW25R2
NCV8504PW33
NCV8504PW33R2
NCV8504PW50
NCV8504PW50R2
NCV8504PWADJ
NCV8504PWADJR2
NCV8509PDW18

NCV8509PDW18R2
NCV8509PDW25
NCV8509PDW25R2
NCV8509PDW26
NCV8509PDW26R2

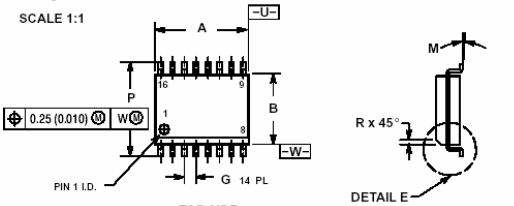
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

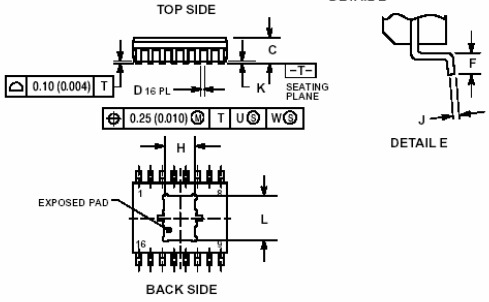
ON Semiconductor

SOIC 16 LEAD WIDE BODY, EXPOSED PAD
CASE 751R−02
ISSUE B

DATE 30 JUN 2005

SCALE 1:1





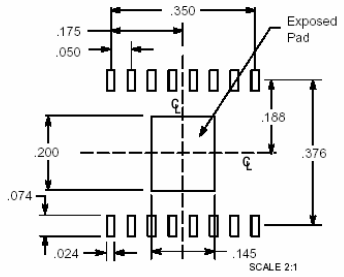
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751R-01 OBSOLETE, NEW STANDARD 751R-02.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
H	3.31	3.51	0.130	0.138
J	0.25	0.32	0.010	0.012
K	0.00	0.10	0.000	0.004
L	4.58	4.78	0.180	0.188
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

MARKING DIAGRAM

xxx = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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STATUS:	ON SEMICONDUCTOR STANDARD		
NEW STANDARD:			
DESCRIPTION:	SOIC−16, WB EXPOSED PAD		PAGE 1 OF 2