ON Semiconductor

PRODUCT/PROCESS CHANGE NOTIFICATION
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15-NOV-2000

SUBJECT: ON Semiconductor Change Notification 10399

TITLE: Wafer fab technology change for selected ECLinPS devices

EFFECTIVE DATE: 26-Feb-2001

AFFECTED CHANGE CATEGORY(S):

WAFER PROCESS
SUBCONTRACTOR FAB SITE
DIE SHRINK
DESIGN CHANGE

AFFECTED PRODUCT DIVISION(S):

LOGIC PRODUCTS DIV

ADDITIONAL RELIABILITY DATA: Available
Contact your local ON Semiconductor Sales Office.
or DAVID ERHART, <S20824@onsemi.com>

SAMPLES: Contact Below
Contact your local ON Semiconductor Sales Office.
Technical Information Center, <NA@onsemi.com>

FOR ANY QUESTIONS CONCERNING THIS NOTIFICATION:
Contact Sales Office or TIM GURNETT, <R13617@onsemi.com>

DISCLAIMER:

ON Semiconductor will consider this change approved unless specific conditions of acceptance are provided in writing within 30 days of receipt of this notice. To do so, contact your local ON Semiconductor sales office.

DESCRIPTION AND PURPOSE:

In order to better serve our customers, ON Semiconductor will increase wafer capacity by redesigning selected ECLinPS and ECLinPS-Lite devices from MOSAIC3 to MOSAIC5. The devices will continue to meet the same data sheet specifications. MOSAIC5 is a more advanced wafer fabrication process technology on which all ECLinPS Plus devices are currently produced. MOSAIC5 is a trench isolated, double epi, double poly, multi-layer metal, bipolar process similar to MOSAIC3, but has a minimum photolithography feature size of 0.7 um, as compared to MOSAIC3 which has a minimum photolithography feature size of 2 um. Additionally, MOSAIC5 utilizes an industry standard inorganic interlayer dielectric layer as compared to MOSAIC3 which has an organic polyimide interlayer dielectric layer.

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The MOS6 wafer Fab, located in Phoenix, Arizona, has been qualified to run ECLinPS Plus devices using the same arrays on the MOSAIC5 process for approximately 2 years. The MOSAIC5 process at MOS6 has been qualified to run production wafers since 1994.

The device parameters will continue to meet all data book specifications. Device reliability will continue to meet ON Semiconductor standards. These device types will be available on MOSAIC 3 during the transition period in order to provide customers an opportunity to evaluate the MOSAIC5 devices in their applications. The MOSAIC5 device types will be denoted with an additional letter, "F", as the first character of the datecode marking while MOSAIC3 devices will continue to be marked with the current marking code. Customers are invited to request samples to examine for any performance variations in their applications.

The following device types have been selected:
MC10EL11D, MC100EL11D, MC100LVEL11D, MC10EL16D, MC100EL16D, MC100LVEL16D, MC100EL14DW, MC100LVEL14DW, MC10E111FN, MC100E111FN, MC100LVE111FN.

Samples of the MC10EL11D will be available by January 16, 2001.
Samples of the MC100EL11D will be available by January 16, 2001.
Samples of the MC100LVEL11D will be available by January 19, 2001.

Samples of the MC10EL16D will be available by October 15, 2000.
Samples of the MC100EL16D will be available by November 6, 2000.
Samples of the MC100LVEL16D will be available by January 19, 2001.

Samples of the MC100EL14DW will be available by November 15, 2000.
Samples of the MC100LVEL14DW will be available by November 17, 2000.

Samples of the MC10E111FN will be available by December 18, 2000.
Samples of the MC100E111FN will be available by December 27, 2000.
Samples of the MC100LVE111FN will be available by November 6, 2000.

Contact the (TIC) Technical Information Center @ 1-800-282-9855 regarding sample dates for each of the device types listed above. The PCN will expire 100 days after the sample date per device type. Please contact the Technical Information Center for assistance in qualifying these device types.

QUALIFICATION PLAN:

The Mosaic 5 Qual reports available are:
- MC100EP139DW 0143 2000
- MC10P01D PJJA001 1999
- MC10P05D PJJA002 1999
- MC10EP56DT 0178 2000

RELIABILITY DATA SUMMARY:

The MOSAIC 5 arrays H26R and J58R processed in MOS 6 Fab are fully qualified.

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ELECTRICAL CHARACTERISTIC SUMMARY:

Please see below the summary comparing the BMC control lot to the MOSAIC 5 lot. All tpd, rise and fall time variance was less than 5%. The sigma for all of the MOSAIC 5 parameters were tighter than the control lot, as shown below.

MS3 to MS5 Redesign - Prelminary AC/DC Summary at Nominal (-5.2 Volts)

10EL16 - Quint Differential Line Receiver

Voltage -5.2 V Matrix Lot used 40 units UPDATED TG 10/13/00
Temp 25 C Control Lot used 40 units

MEASUREMENT INFO		CONTROL LOT		MOSAIC 5 LOT		LIMITS			VARIATION	
Test Name	Units	Mean	S	Mean	S	Lo limit	Typ	Hi Limit	Mean	Sigma
IEE	mA	15.3	0.2	18.8	0.3	DNC	18	22	10.3%	20.0%
VBB	mV	-1297	8	-1306	6	-1350		-1250	0.3%	14.3%
IIL D	uA	35.1	1.6	55.3	1	0.5		DNC	22.3%	23.1%
IIH D	uA	35.2	1.6	74.4	1.2	DNC		150	35.8%	14.3%
VOL Q	mV	-1725	11	-1822	10	-1950		-1630	2.7%	4.8%
VOH Q	mV	-882	11	-897	3	-980		-810	0.8%	57.1%
DIFF TPD XPT (++)	Ps	231	6	247	4	175	250	325	3.3%	20.0%
DIFF TPD XPT (- -)	Ps	243	6	252	3	175	250	325	1.8%	33.3%
SE TPD XPT (++)	Ps	255	8	263	4	125	250	375	1.5%	33.3%
SE TPD XPT (- -)	Ps	262	6	267	4	125	250	375	0.9%	20.0%
RISE TIME Q	Ps	153	4	155	6	100	225	350	0.6%	20.0%
RISE TIME Qbar	Ps	154	7	144	5	100	225	350	3.4%	16.7%
FALL TIME Q	Ps	147	5	158	5	100	225	350	3.6%	0.0%
FALL TIME Qbar	Ps	143	5	144	5	100	225	350	0.3%	0.0%

CALC = ABS((X-Y)/(X+Y)

Summary: The major AC issues, Prop delays and Rise & Fall times match the control lot produced from the BMC Fab.
The current (IEE) is slightly higher than control lot, but match data book typical and is under the 22 mA max limit.
The MOSAIC 5 process sigma was much tighter than the control lot in most cases.

CHANGED PART IDENTIFICATION:

The trace code will have the FAB option enabled for the new parts on the MOSAIC 5 process.

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AFFECTED DEVICE LIST:

PART
MC100E111FN
MC100EL11D
MC100EL14DW
MC100EL16D
MC100LVE111FN
MC100LVEL11D
MC100LVEL14DW
MC100LVEL16D
MC10E111FN
MC10EL11D
MC10EL16D