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PRODUCT BULLETIN
Generic Copy

04-OCT-2000

SUBJECT: ON Semiconductor Product Bulletin 10318

TITLE: SC74 PACKAGE STANDARDIZATION AND LEADFRAME CHANGE

EFFECTIVE DATE: 05-Oct-2000

AFFECTED CHANGE CATEGORY(S):

None

AFFECTED PRODUCT DIVISION(S):

BIPOLAR DISCRETES PRODUCTS DIV

ADDITIONAL RELIABILITY DATA: Available
Contact your local ON Semiconductor Sales Office.

SAMPLES: No

FOR ANY QUESTIONS CONCERNING THIS NOTIFICATION:
Contact(PAUL LEM, FFBFBM@onsemi.com)

DISCLAIMER:

ON Semiconductor considers this change approved unless specific conditions of acceptance are provided in writing. To do so, contact your local ON Semiconductor sales office.

DESCRIPTION AND PURPOSE:

This change involves package dimension standardization and the elimination of the internal Silver-stripe from the lead frame in all devices in SC74 package assembled in Seremban, Malaysia.

SC74 Package Dimension Standardization:
Package dimension standardization consists of changes in the package length (dim. A), package height (dim C.) and the lead width (dim. D). Please refer to Table A for dimensional changes.

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Figure 1: SC74 Case Outline

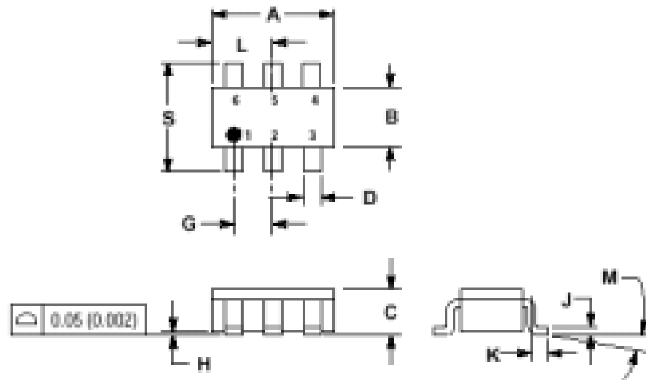

TABLE A - SC74 DIMENSION STANDARDIZATION

DIM.	OLD DIMENSION		NEW DIMENSION		JEDEC STANDARD	
	Min:	Max:	Min:	Max:	Min:	Max:
A	0.1063"	0.1220"	0.1142"*	0.1220"*	0.1083"	0.1201"
C	0.0394"	0.0511"	0.0354"	0.0433"	NA *	0.0433"
D	0.0138"	0.0196"	0.0098"*	0.0197"	0.0118"	0.0197"

NA - Not available
 * - Dimension complies with EIAJ standards.

This standardization better aligns our package dimensions with the industry and competitor packages.

The ON Semiconductor SC-74 package is comparable to many competitor packages. Rohm and Phillips Semiconductor SC74 package dimensions are compared to ON Semiconductor's SC-74 package on Table B. Please note Figure 1 for dimensional notation, i.e. Package length noted by 'A'.

TABLE B - DIMENSIONAL COMPARISON OF ON SC74 TO ROHM AND PHILIPS SEMICONDUCTOR

All Dimensions are in inches, except M which is in degrees.

DIM.	ON SEMI.		ROHM (SEE NOTE 1)		PHILIPS SEMICONDUCTOR (SEE NOTE 1)		JEDEC (SEE NOTE 1)	
	Min	Max		Dimensions	Min	Max	Min	Max
A	0.1142"	0.1220"*		0.1142"	0.1063"	0.1220"	0.1083"	0.1201"
B	0.0512"*	0.0689"	--	0.0630"	0.0512"	0.0669"	0.0571"	0.0689"
C	0.0354"	0.0433"	--	0.0433"	0.0354"	0.0433"	--	0.0433"
D	0.0098"*	0.0197"	--	0.0118"	0.0098"	0.0157"	0.0118"	0.0197"
G	0.0335"	0.0413"	--	0.0374"	--	0.0374"	0.0295"	0.0453"
H	0.005"	0.0039"	--	0.0040"	0.0005"	0.0039"	0	0.0039"
J	0.0040"	0.0102"*	--	0.0059"	0.0039"	0.0102"	0.0031"	0.0079"
K	0.0079"*	0.0236"		0.0118" to 0.0236"	0.0079"	0.0236"	0.0118"	0.0236"
L	0.00493"	0.0610"	--	--	--	--	--	--
M	0	10	--	--	--	--	--	8
S	0.0985"*	0.1181"	--	0.1102"	0.0984"	0.1181"	0.1004"	0.1201"

-- = Not available
Note 1: Competitor and JEDEC dimensions were extracted from and are shown at their respective websites.

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* = Dimension complies with EIAJ standards.

SC74 Silver-stripe elimination from leadframe

In alignment with ON Semiconductor's industry standardization of small package platforms, the Silver-stripe on the SC74 lead-frame will be eliminated. This change has already been qualified on ON Semiconductor SOT23/SOD123 small package platforms and has been the standard production leadframe since 1996.

These changes will take effect beginning WW40 (workweek 40), October 2nd, 2000.

Device markings will not change. Current device markings on Seremban, Malaysia assembled devices are the following:

DEV M

Where:
DEV = Device Marking
M = Date code (no rotation of orientation)

RELIABILITY DATA SUMMARY:

RELIABILITY DATA FOR SOT-23, NO SILVER (Ag) STRIPE
DATA REPRESENTS FOUR (4) SEPARATE MANUFACTURING LOTS

DEVICE - MMBTH10LT1

AUTOCLAVE
(TA = +121 Deg C, RH = 100%, PSIG = 15, 96 Hours)
0/336 Rejects

AUTOCLAVE W/PRECONDITION
(TA = +121 Deg C, RH = 100%, PSIG = 15, 96 Hours)
0/336 Rejects

BOND PULL - (Cond. C or D; pre- or post mold)
0/60 Rejects

BOND SHEAR - (Cond. C or D; pre- or post mold)
0/60 Rejects

DESTRUCTIVE PHYSICAL ANALYSIS (DPA)
Random Sample of Good H3TRB devices per
CDF-AEC-Q101-004 Section 4
0/12 Rejects

DESTRUCTIVE PHYSICAL ANALYSIS (DPA)
Random Sample of Good Temp Cycle devices per
CDF-AEC-Q101-004 Section 4,
0/12 Rejects

DIE SHEAR
(Cond. C or D; pre- or post mold)
0/20 Rejects

ESD (HBM=>16000 V)
0/120 Rejects

ESD (MM=>2000 V)
0/120 Rejects

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HUMIDITY TEMPERATURE REVERSE BIAS (H3TRB)
(TA = +85 Deg C, RH = 85%, VCB = +24 V, VEB = 0 V, 1008 Hours)
0/336 Rejects

HIGH TEMPERATURE BAKE
(TA = +150 Deg C, 1008 Hours)
0/336 Rejects

HIGH TEMPERATURE REVERSE BIAS (HTRB)
(TA = +150 Deg C, VCB = +24 V, VEB = 0 V, 1008 Hours)
0/336 Rejects

HIGHLY ACCELERATED STRESS TEST (HAST)
WITH PRE-CONDITIONING
(TA = +130 Deg C, RH = 85%, PSIG = 18.8, Vr = 25 V, 96 Hours)
0/336 Rejects

INTERMITTENT OPERATING LIFE (IOL)
(TA = +25 Deg C, delta Tj => 100 Deg C, 2 minutes on/off, VCE = 20 V,
IC = 11.25 mA, PD = 225 mW, Delta TJ=100 Deg C, Rc & Re = 510
Ohms, 15,000 Cycles)
0/336 Rejects

MOISTURE SENSITIVITY LEVEL (MSL 1)
(10 TC + 24 Hour Bake at 125 Deg C + 168 Hours 85/85 + 3 IR at
220 Deg C + 1X Flux Immersion + DI Rinse)
0/336 Rejects

SOLDER HEAT
(TS = 260 Deg C, Tdwell = 10 Seconds)
0/120 Rejects

SOLDERABILTIY
(8 Hours steam aging prior to testing; 1 hour gold plated leads)
0/40 Rejects

TEMPERATURE CYCLE (TC)
(Air to Air; -65 Deg C to +150 Deg C, 1000 Cycles)
0/336 Rejects

TEMPERATURE CYCLE (TC) WITH PRE-CONDITIONING
(Air to Air; -65 Deg C to +150 Deg C, 1000 Cycles)
0/336 Rejects

THERMAL RESISTANCE
0/40 Rejects

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AFFECTED DEVICE LIST

PART

MMBT2131T1
MMBT2131T3
MMBT2132T1
MMBT2132T3
MMQA12VT1
MMQA13VT1
MMQA13VT3
MMQA15VT1
MMQA18VT1
MMQA20VT1
MMQA20VT3
MMQA21VT1
MMQA22VT1
MMQA24VT1
MMQA27VT1
MMQA30VT1
MMQA33VT1
MMQA5V6T1
MMQA6V2T1
MMQA6V2T3
MMQA6V8T1
SMQA1001T1
SMQA1002T1