TND6330/D
Rev. 5, July – 2022

Using Physical and Scalable Simulation Models to Evaluate Parameters and Application Results

July, 2022 – Rev. 5
Publication Order Number:
TND6330/D

Using Physical and Scalable Simulation Models to Evaluate Parameters and Application Results

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ABSTRACT

Physical and scalable modeling technique is an advanced SPICE modeling approach based on process and layout parameters which enables design optimization through a direct link between SPICE, physical design, and process technology. Physical and scalable models are available for nearly all discrete power components from the **onsemi** web site. The models' accuracy allows the user to extract device parameters (like in a data sheet) for a given operating point when these parameters are not in the data sheet. These models give a real picture on how the device will perform in a real application. Power device losses are not guessed with an empirical formula but obtained in a real circuit including all the parasitics (like layout, passive parasitics,...). Key information, like junction temperature, can be also monitored to determine the device mission profile used in reliability calculations.

INTRODUCTION

Physical and scalable modeling has been described by James Victory in papers [1], [2], [3] and tutorial [4]. These models are based on silicon (or silicon carbide or gallium nitride) equations and the geometry of the device. They are not obtained by curves fitting. They are behavioral models. They are linked to technology platform and device are obtained by scaling. They include packaging parasitics. Thermal dependence is also calculated step by step during simulation using the electro−thermal equivalence. This will be shown in this paper.

The simulators' (Orcad, SIMetrix and LTspice) setup is explained in the following reference [5].

This paper will focus on simple simulation schematic description to extract device parameters like on resistance and output capacitor values as a function of the operating point.

The difference between models with and without thermal dependency will be also explained.

The paper will also describe the results (like junction temperature, losses,...) obtained on a full boost stage diagram.

"ON" STATIC REGION CURVES

Drain Current versus Drain−Source Voltage with Gate−Source Voltage as Parameter (First Example: NTHL040N65S3F)

The on−region characteristic or curve shows how the drain current changes due to the drain to source voltage with the gate to source voltage used as a parameter. This curve is given in all university books describing MOSFETs (see Figure 1) and also in data sheet (see Figure 2).

The "on" characteristic or curve is made of two regions:

- The linear or ohmic region: it corresponds to the region where the MOSFET behaves as a resistor (called R_{DSon}).
- The saturation or active region: it corresponds to the region where the curve is almost flat and the MOSFET operates like a current source.

These curves depend mostly on the voltage applied to the gate.

We can find this on−region curve in "MOSFET Basics" application note from **onsemi** [6] in the Figure 1 below.

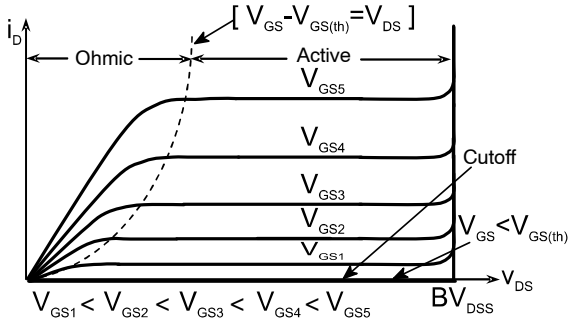

Figure 1. Typical On−Region Curve from a University Book

In specification, this curve is shown in a log scale. For example, for the NTHL040N65S3F, SuperFET3 Fast recovery 40 mΩ, the curve is the one in Figure 2.

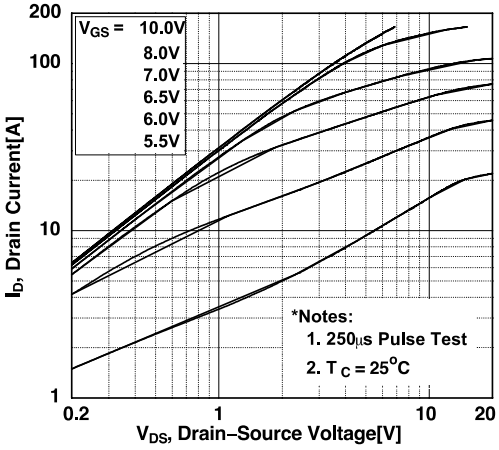

Figure 2. On−Region Curve from Data Sheet

To extract this characteristic on SIMetrix, a 3−pin transistor model was used and two voltage sources were connected to the transistor: one between the drain and source pin, the other between the gate and the source pin as shown in the Figure 3.

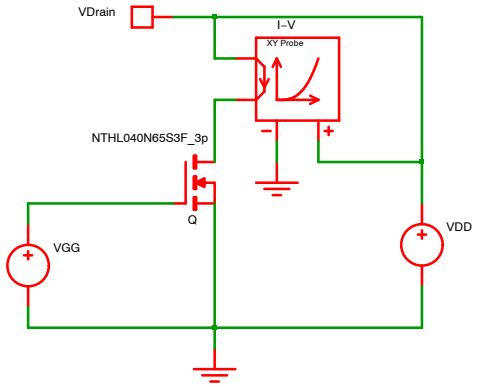

Figure 3. On−Region Simulation Schematic

For the simulation configuration, see Figure 4, we choose a dc sweep analysis mode for the drain to source voltage source (VDD).

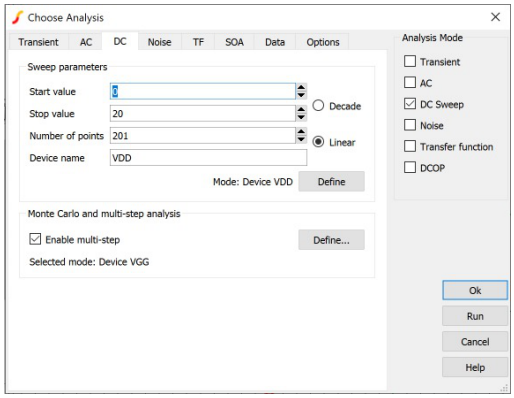

Figure 4. On−Region Simulation Setup

The multi−step analysis was enabled for the voltage source (VGG) in order to use gate−to−source as a parameter for the on−region characteristics (see Figure 5).

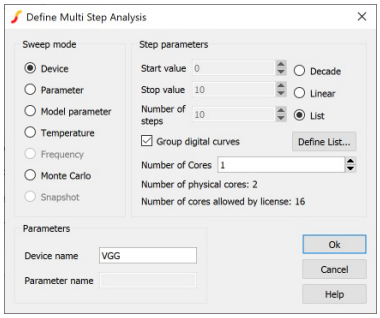

Figure 5. On−Region Multi−Step Setup

A list was created in order to define possible gate−to−source voltage values (See Figure 6).

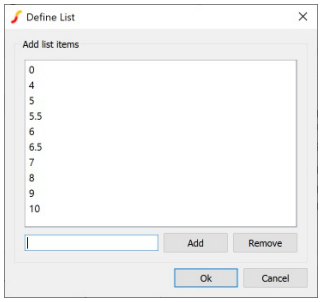

Figure 6. On−Region Simulation List Setup

Simulation was performed for a temperature of 25°C.

On the schematic Figure 3, we added an “X−Y Probe” to plot the drain current versus the drain−to−source voltage. We obtained the Figure 7.

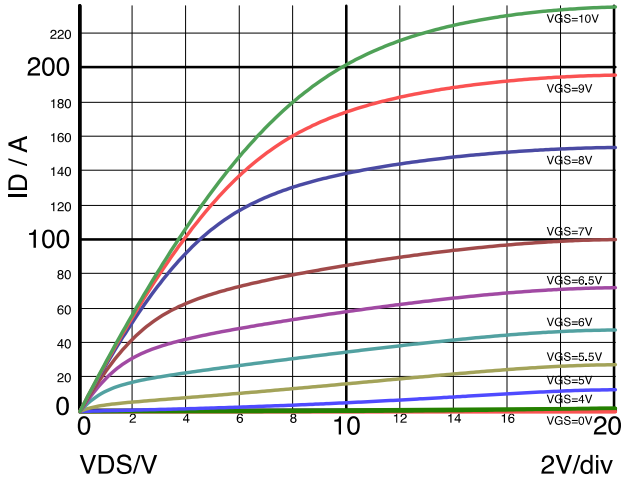

Figure 7. On−Region Curve Simulation Results

Using a list with the same values as the gate−to−source voltage used for the specification curve and also using a logarithmic scale for X and Y axes, we obtained the curve shown in Figure 8:

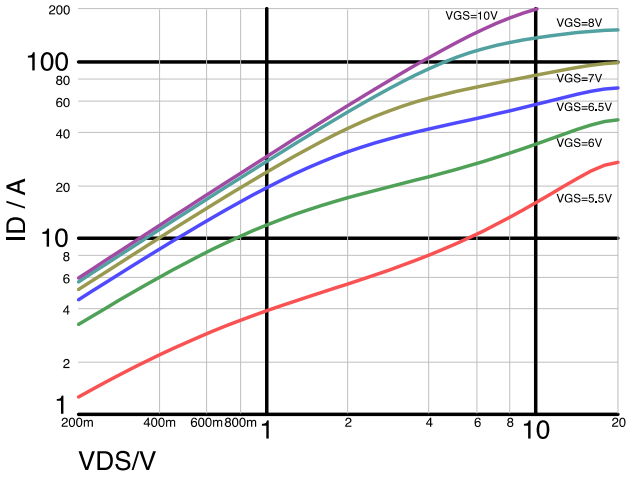

Figure 8. On−Region Curve Simulation Results

With the same test conditions, the comparison of Figures 2 and 8 shows how the simulation results (done with our MOSFET model) match perfectly with the value obtained during the lab measurement and extracted from the datasheet.

Drain Current versus Drain−Source Voltage with Gate−Source Voltage as Parameter (Second Example: NTMFS5C604N)

Now, if we use a medium voltage MOSFET model, like the NTMFS5C604N, and the same simulation schematic as Figure 3. For the drain−to−source voltage, we use the same setup. We obtained the following results (see Figure 9) using a linear scale as found in literature.

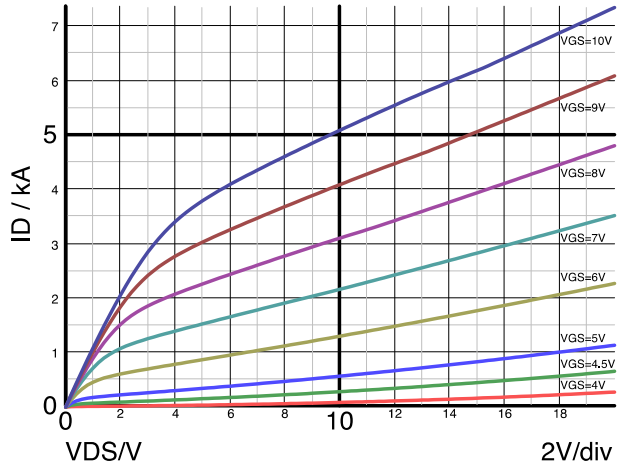

Figure 9. On−Curve Simulation Results

In this simulation, the results obtained are far beyond the MOSFET specifications. So, they are not valid. The model is only valid within specification limits.

If we use a 5−pin model to monitor the junction temperature, we have the following simulation schematic (Figure 10).

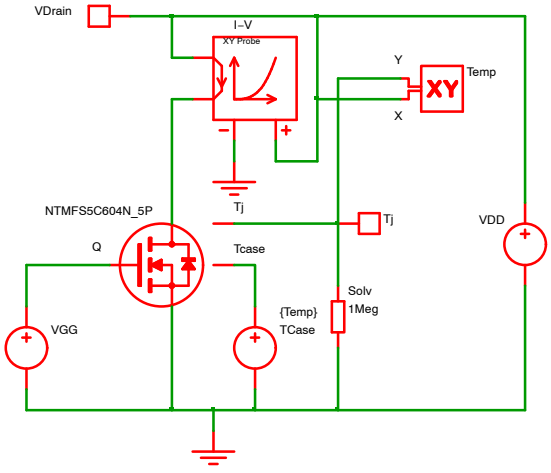

Figure 10. On−Curve Simulation Schematic with a Constant Temperature Package

The model uses the electro−thermal equivalence where Voltage represents the Temperature and the Current represents the Power dissipated. The case temperature is set to the system temperature using a voltage source. The voltage−source value is set with the SIMetrix variable "Temp" storing the system temperature. The system temperature can be set to 25°C in the option tab inside simulation setup windows (see Figure 11).

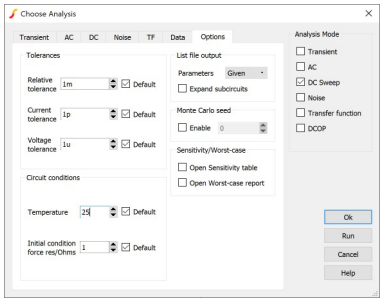

Figure 11. System Temperature Setup

We need to add a 1−MΩ resistor on the "junction temperature" pin to help the solver to converge. On top of the I−V "XY Probe", we have a second plot using a "XY Probe" to monitor the junction temperature behavior.

We obtain the curves of Figure 12.

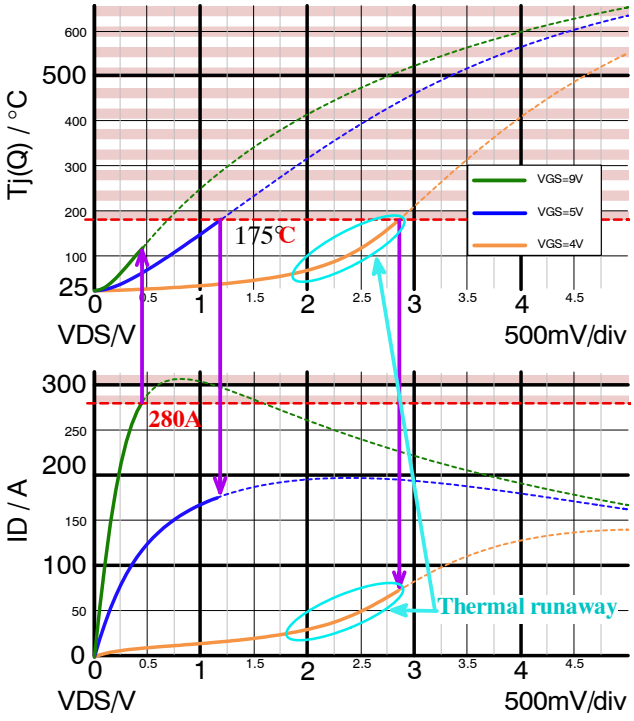

Figure 12. On−Curve Simulation Results with 25°C Constant Temperature Package

Even if we maintain the package temperature at 25°C, we have the junction temperature rising above 175°C

(maximum junction temperature specified) while the current flowing in the drain pin is above 280 A (maximum rating current at 25°C).

If we analyze the results in Figure 12, we can note:

- For a gate−to−source voltage equal to 4 V, we see a thermal runaway in the saturation region. The current increases faster and faster while the voltage rises up. The junction temperature rises above 175°C before the drain current reaches the 280 A specification limit.
- For a gate−to−source voltage equal to 5 V, the device stays in the ohmic region but the junction temperature rises to 175°C before it gets to 280−A drain current limit.
- For a gate−to−source voltage equal to 9 V, the device stays in the ohmic region but the drain current rises to 280 A limit before it gets to 175°C junction temperature.

If we stop the current flow when the current reached 300 A or when the junction temperature reached 175°C, we will stay within specification limits.

We limit the drain−to−source current source to 300 A. We use a switch driven by the junction temperature to short the current source when the temperature gets above 175°C. We implement a very large hysteresis to avoid a new turn on when the device cools down.

Figure 13 describes the following simulation schematic:

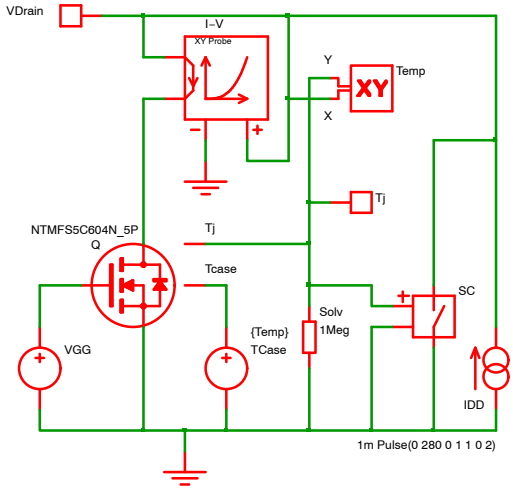

Figure 13. On−Curve Simulation Setup with Current and Junction Temperature Shutdown

Here is the setup (Figure 14) for the switch shorting the current source.

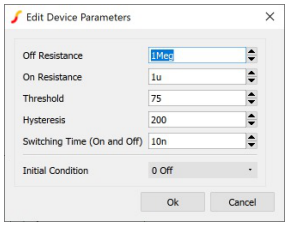

Figure 14. Switch Setup to Short the Current Source

The switch on−resistance should be much smaller than the on−resistance of the device to simulate (or measure).

The switch is made with a 1 μΩ on−resistance affected by 200°C hysteresis. The switching time is set to 10 ns.

Simulating the previous schematic, we obtained the curves shown in Figure 15:

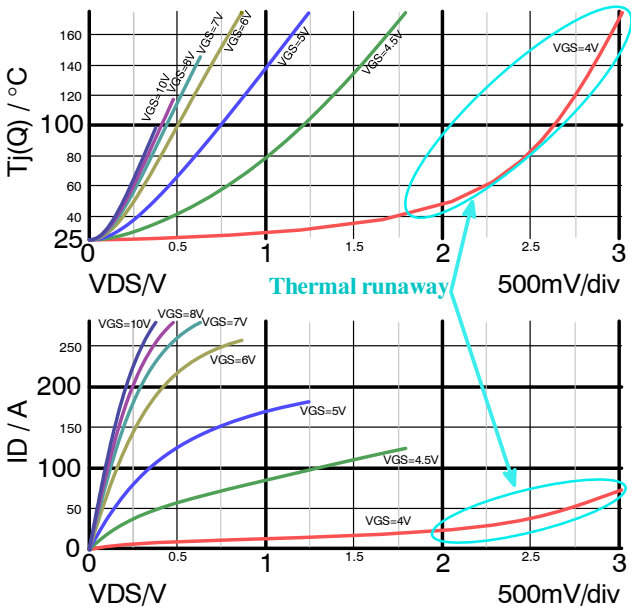

Figure 15. On−Curve Simulation Results up to 280 A and 175°C Junction Temperature with 25°C Case Temperature

When the thermal protection operates, as it is not an ON/OFF switch, the drain current goes immediately to zero with a stay horizontal line. These flat lines have been purposely removed from the graph above (in Figure 15) for clarity sake.

For a gate−to−source voltage equal to 4 V, a thermal run away can be seen. The curve in the saturation or active region rises up again and the junction temperature rises like an exponential curve. This happens when the drain−to−source voltage reaches around 2 V. The junction temperature curve slope changes very fast from 40°C to 175°C.

On−curve Comparison between Specification and 3−pin and 5−pin Models Results for NTHL040N65S3F

In the specification, to measure the on−curve, we use 250 μs pulse to limit self−heating and the case at 25°C. See Figure 2.

Using the 3−pin model in Figure 3 and the setup given in Figures 4, 5 and 6, we obtain the curve on Figure 8.

The 3−pin model gives almost the same results because in the 3−pin model the self−heating doesn't affect the die temperature. It can be similar to maintain the die in a constant temperature environment or consider an infinite heatsink that has a thermal impedance equal to zero.

Now, if we use the 5−pin model and limit the temperature rise to stay within the specification limits, we can use the

schematic in Figure 16 to obtain the on−curve in continuous operation mode.

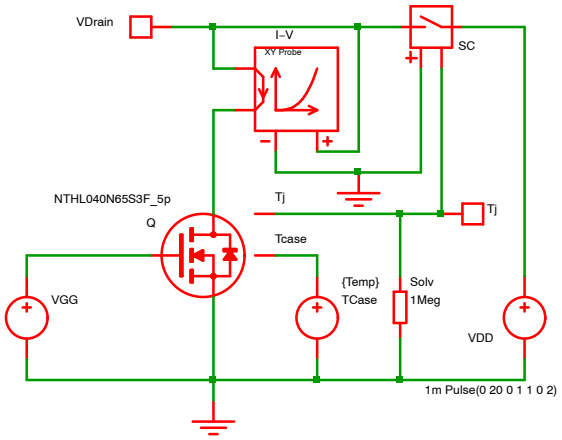

Figure 16. On−Curve Simulation Setup with Voltage and Junction Temperature Shutdown

To stop the curve when the junction temperature reaches 150°C, we use a switch driven by the junction temperature. Compare to Figure 13, we use a voltage source and inverse the operation of the voltage−switch that turn off when temperature reaches 150°C. The switch setup is given in Figure 17.

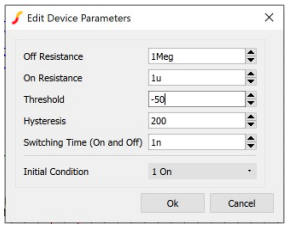

Figure 17. Switch Setup to Open the Voltage Source

Simulating the previous schematic (Figure 16), we obtained the curves shown in Figure 18.

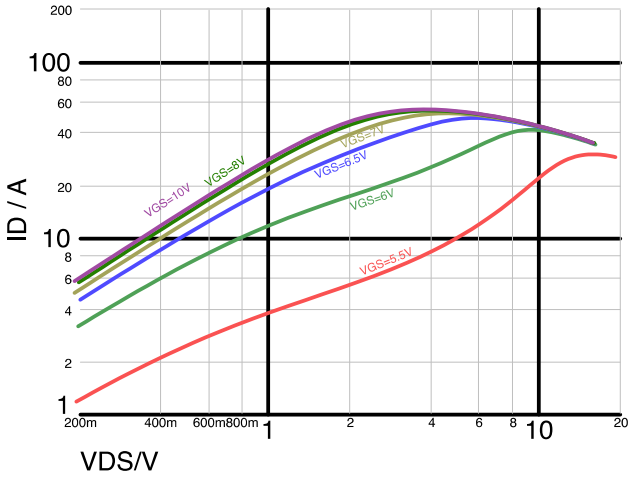

Figure 18. On−Curve Simulation Results up to 200 A and 150°C Junction Temperature with 25°C Case Temperature

When the thermal protection operates, as it is not an ON/OFF switch, the drain current goes immediately to zero with a stay horizontal line. These flat lines have been purposely removed from the graph above (in Figure 18) for clarity sake.

We can see the effect of the self−heating and we have the useful curve in continuous mode operation.

To precisely emulate the datasheet characteristics, a 250 µs−transient pulse of each drain−to−source bias condition needs to be simulated. The drain−current at the end of the pulse is sampled for each voltage source pulse. Subsequently the I_D vs. V_{DS} plot is constructed. This setup is not shown here in SIMetrix because it requires using SIMetrix scripting capability, however, it has been verified in PSpice.

On Resistance Value versus Drain Current

This characteristic shows how the on−resistance value changes with the drain current and the gate−to−source voltage. To obtain this characteristic, we connected a current source between the drain and source pin as shown in the Figure 19.

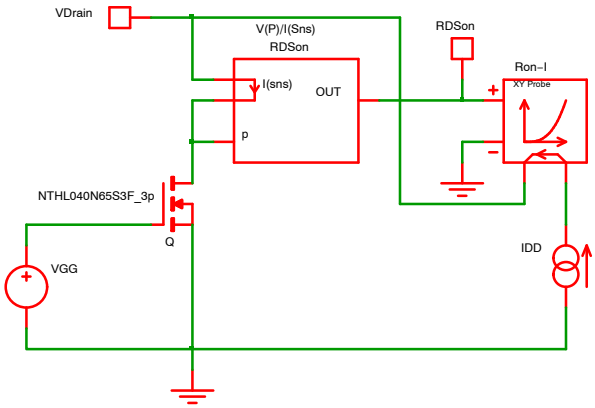

Figure 19. On Resistance versus Drain Current Simulation Schematic

Simulation was performed on the NTHL040N65S3F MOSFET 3−pin model and a 25°C temperature was used for this simulation. See Figure 11 to setup this system temperature.

In this simulation setup, we applied a dc sweep on the drain current. We enabled the multi−step analysis on the gate−to−source voltage, same as in Figure 3 to simulate on−region curves.

To calculate the on resistance, we use an arbitrary source to make the division between drain−to−source voltage by the drain current. We obtained a voltage directly proportional to the "on" resistance. See Figure 22 for an arbitrary function setup example.

To display the resistance value curve, we use X−Y probe. The X axis is connected to the drain current and the Y axis is connected to the on resistance arbitrary function.

After simulation, we get the following curve (Figure 20).

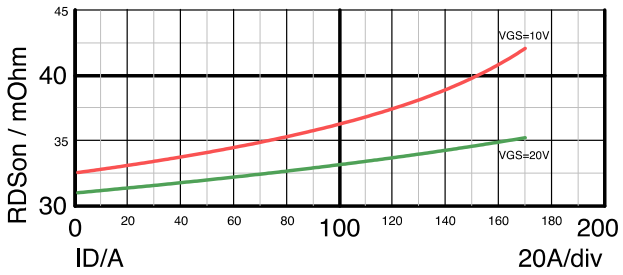

Figure 20. On−Resistance Value versus Drain−Current Simulation Results

On the plot above, we can see there is slight difference between the resistance curve obtained during the simulation performed with the NTHL040N65S3F MOSFET model and the curve shown in the datasheet.

In fact, for a 100−A drain current and a 10−V gate−to−source voltage, the difference between the simulation results and the datasheet measurement is almost 1.25 mΩ. This corresponds to a 3% relative difference. This is acceptable.

On Resistance Value versus Temperature

With this curve, we can see how the on−resistance changes with the temperature. The temperature has an impact on the charge carrier agitation, and this will affect the transistor on−resistance value.

In switching applications, during turn−on, the current starts flowing through the transistor. It has the effect of increasing the junction temperature by self−heating. As a result, the on−resistance value will increase during turn on due to temperature increase caused by current flowing.

We will use almost the same schematic (see Figure 21) as the previous simulation (in Figure 19) featuring the arbitrary function block to calculate the on−resistance value. We add a parameter to normalize the curve with the 25°C value (see Figure 22). We plotted the X−Y curve as a function of the temperature (instead of the drain current in the previous chapter).

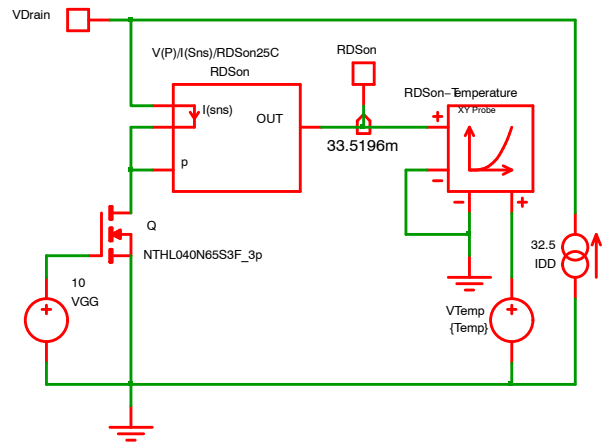

Figure 21. On−Resistance versus Temperature Simulation Schematic

For this simulation, a 10−V gate−to−source voltage was used as in the datasheet. A 32.5−A current source was set in order to match the value given in the specification.

A voltage source equal to the simulation temperature (with the SIMetrix variable "*Temp*") is used to have the X axis for the X−Y probe. The X−Y probe Y axis is connected to arbitrary function output.

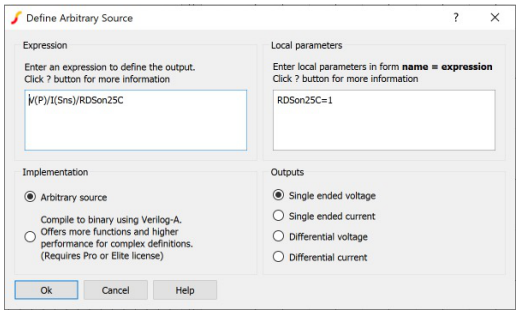

Figure 22. Arbitrary Function Setup

We will run an operating point calculation (on top of the dc sweep simulation in Figure 23) with an ambient temperature equal to 25°C. This is defined by checking the DCOP (dc operating point) simulation and the temperature in the red box in the Figure 23.

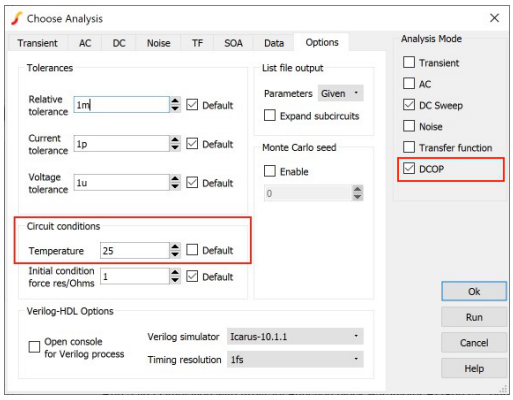

Figure 23. On−Resistance Value versus Temperature Operating Point Simulation Setup

We placed also a "Bus annotation marker" in the schematic of Figure 21 to show the arbitrary−function result (the on−resistance value) at the operating point.

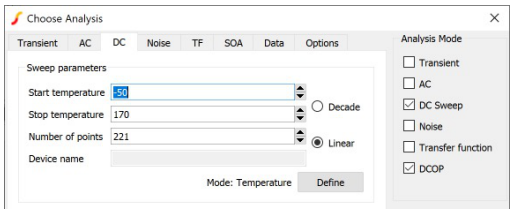

Figure 24. On−Resistance Value versus Temperature dc Sweep Simulation Setup

We setup the simulation to run a dc sweep on the temperature as shown in the Figure 24 above.

1. We set the arbitrary function block parameter RDSon25C equal to 1 as shown in Figure 22.
2. We run the simulation a first time.
3. We get the 25°C on resistance with the bus annotation marker (33.5196m as shown in Figure 21).
4. We also get the on−resistance value as a function of the temperature. (See Figure 25)
5. We set the arbitrary function parameter RDSon25C equal to this bus annotation marker result.
6. We run the simulation a second time.
7. The bus annotation marker should have a value very close or equal to 1 if the arbitrary function block parameter was properly/accurately set.
8. We get the normalized on resistance versus temperature as shown in Figure 26.

Setting the parameter (RDSon25C equal to 1), then, changing the operating point (VGG and IDD), the on resistance versus temperature can be obtained for any operating point depending on the desired application as shown if Figure 25.

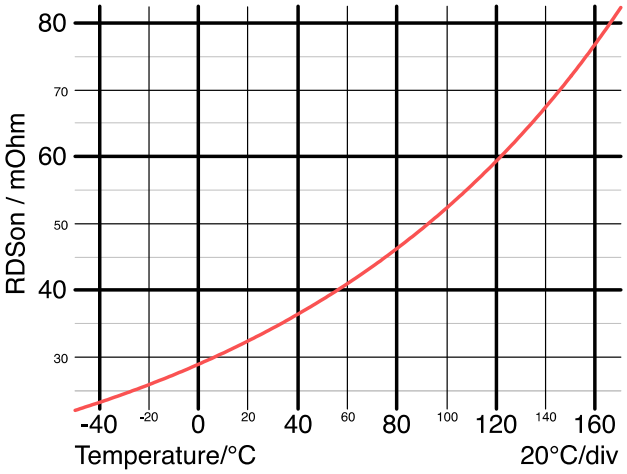

Figure 25. On−Resistance Value versus Temperature Simulation Results

In Figure 25, we can measure 33.5196m for the on−resistance at 25°C. We will use this value for the arbitrary function parameter RDSon25C to re−run the simulation and obtain the normalized on−resistance curve shown in Figure 26.

The plot Figure 26 is similar to the one in the specification.

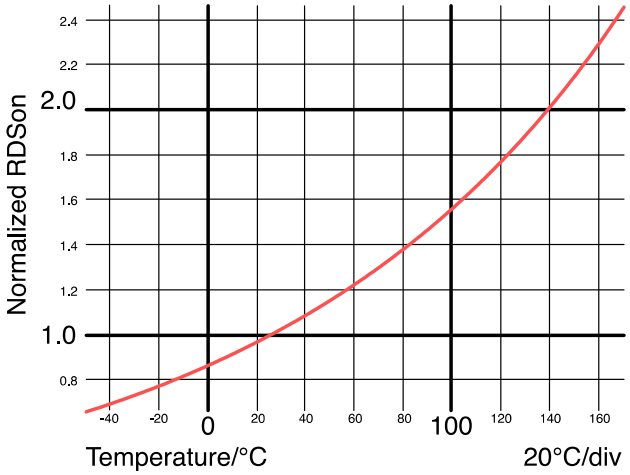

Figure 26. Normalized On−Resistance Value versus Temperature Simulation Results

On Resistance Value versus Time (Dynamic Analysis)

The 5−pin models are very useful when you want to know the junction temperature behavior depending on the mission profile.

In this exercise, we assumed to have a low frequency pulsed current from 1 A to 40 A going through a switch. We made the hypothesis: the switch case is attached to a constant temperature heatsink (without any thermal interface). This temperature is chosen to be the system temperature and modeled by a voltage source with a value equal to the SIMetrix variable "*Temp*" representing the system temperature. Using Figure 11, we set this system temperature to 25°C.

We want to analyze how the on−resistance value changes. So, we will reuse the same arbitrary function to calculate the on resistance on the fly. See Figure 22 for the arbitrary−function setup. (Here, we will not use the "RDSon25C" parameter.) We obtain the schematic shown in Figure 27.

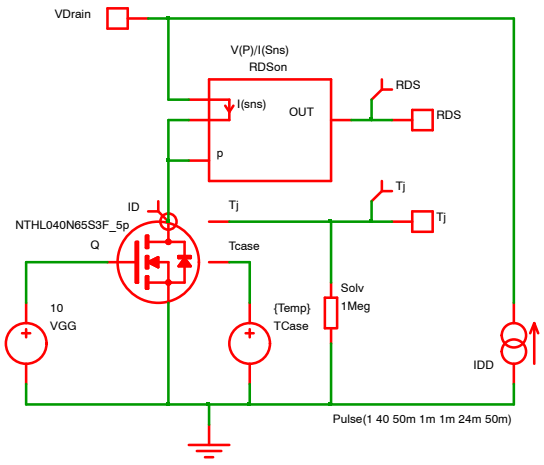

Figure 27. On−Resistance Analysis versus Time Simulation Schematic

We will plot the drain current (using a current probe) for reference. We will monitor the on resistance and the junction temperature, so we add two more probes (voltage probe) as shown in Figure 27.

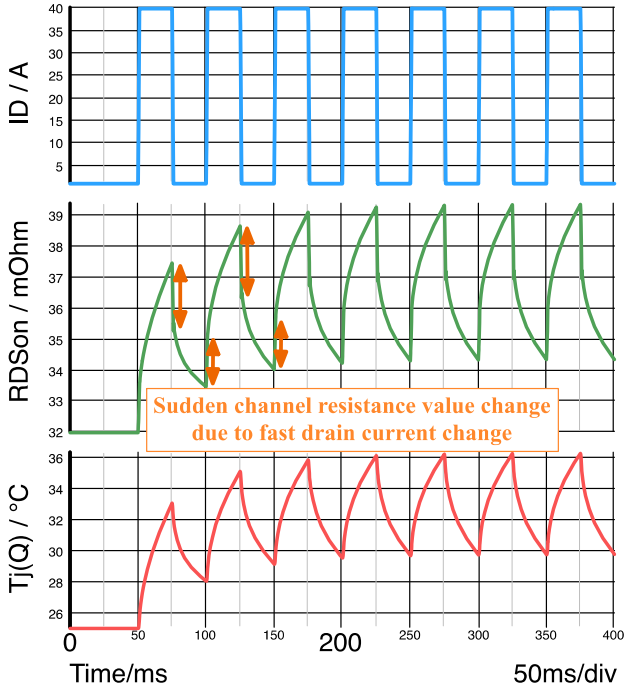

Figure 28. Dynamic Analysis Results for the On Resistance and the Junction Temperature versus Time

In Figure 28, we can notice the sudden change in the on resistance when the drain current moves rapidly from 1 A to 40 A and backward. This phenomenon was predicted by the curve obtain in Figure 20 (on resistance versus drain current). We can also see the effect of the self−heating or cooling of the device itself during the plateau phase of the current (1 A and/or 40 A).

The system is stable after a 200−ms transient. The maximum junction temperature is 36°C and the minimum is 30°C. The junction temperature oscillates between these two values. We could have also calculated the average temperature over a cycle using an “Average PerCycle Probe”, for example.

TRANSFER CHARACTERISTIC VERSUS TEMPERATURE

The transfer characteristic shows how the drain current changes with the gate−to−source voltage. The drain−to−source voltage is fixed. From this simulation setup, the MOSFET transconductance can be extracted. The simulation was done with a 20−V drain−to−source voltage (similar as the data sheet setup) and for various temperature values.

On simulation schematic Figure 29, we will use an X−Y probe to plot the transfer characteristic and the temperature will be set via the “Multi−Step” simulation list.

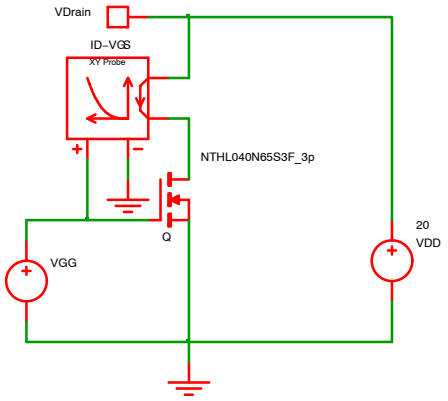

Figure 29. Transfer Characteristic Simulation Setup

We defined a dc sweep for the gate−to−source voltage and a multi−step analysis on the temperature by creating a list of temperature values to be used for this simulation.

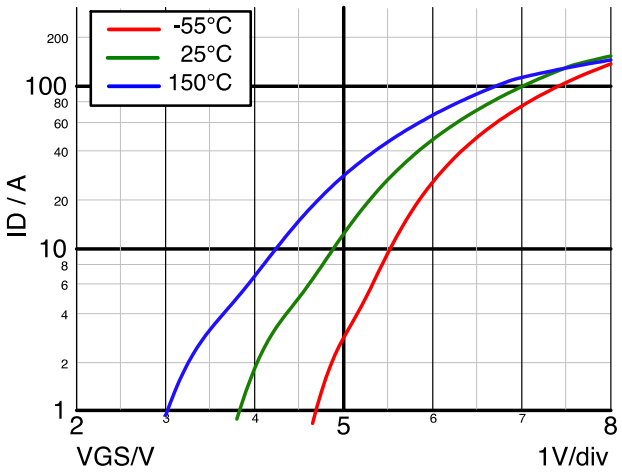

Figure 30. Transfer Characteristic Simulation Results

Figure 30 above shows a good agreement between the simulation result obtained with our transistor model and the datasheet parameters (or characterization curves).

OUTPUT CAPACITANCE

For switching application, the output capacitor called C_{oss} defined as $C_{oss} = (C_{DS} + C_{GD}$ @ $V_{GS} = 0$ V) is an important parameter as it impacts the transistor switching losses. In fact, every time the MOSFET turns on, the energy stored in output capacitance dissipatesin the transistor. The lower the C_{oss} is the better it is. C_{oss} is a non−linear capacitance and highly depends on the drain−to−source voltage.

There are 3 to 4 types of output−capacitance values found in the specification.

The capacitance types are called:

- Small signal value,
- Effective value,

- Energy related value,
- Charge related value.

In this chapter, the way to extract these values by simulation will be explained.

Small Signal Value (1st Method: Transient Simulation).

To measure the small−signal capacitor, a low−amplitude sinusoidal voltage is superimposed to a dc drain−to−source voltage source. The peak−to−peak value of the drain current is measured for several values of drain−to−source continuous voltage and is used to compute the capacitance values.

The following equation defines the capacitor admittance as a function of the ratio of the peak−to−peak current and peak−to−peak voltage:

$$2\pi \times f \times C_{oss} = \frac{(\text{Drain Current})_{Peak-to-Peak}}{(\text{Drain} - \text{to} - \text{Source Voltage})_{Peak-to-Peak}} \quad \text{(eq. 1)}$$

We will use 20−mV peak−to−peak sinusoidal voltage source with frequency equal to 1 MHz in series with the drain−to−source continuous voltage as shown in Figure 31.

We added a current probe on the drain pin of the transistor to measure the drain current.

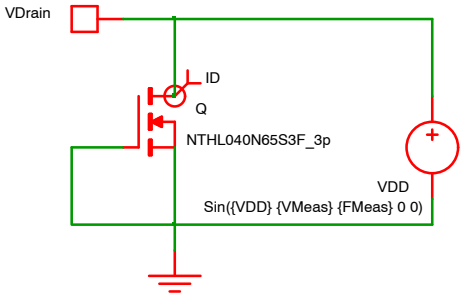

Figure 31. Small−Signal Capacitance Pre−Simulation Schematic

Parameters have been used to define the dc drain−to−source voltage (VDD), the small−amplitude sinusoidal voltage (VMeas) and its frequency (FMeas).

The statements below have been added to the SIMetrix "Command Window" (see Figure 32.) Pressing F11 shows or hides this panel.

```
.Param
FMeas=1Meg
.Param VMeas=10m
.Param VDD=400
```

Figure 32. Parameters Statements in the "Command Window"

We create a "Multi−Step" transient simulation setup using the parameter VDD with the following setup in Figure 33:

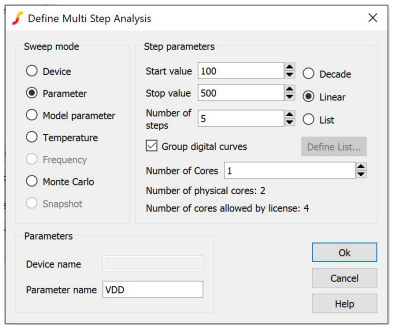

Figure 33. Small−Signal Capacitance Pre−Simulation Setup

We run the transient analysis for 10 ms but storing value only after 8 ms to display the steady−state operation and avoid the initial transient operation.

We obtain the following current waveforms in Figure 34:

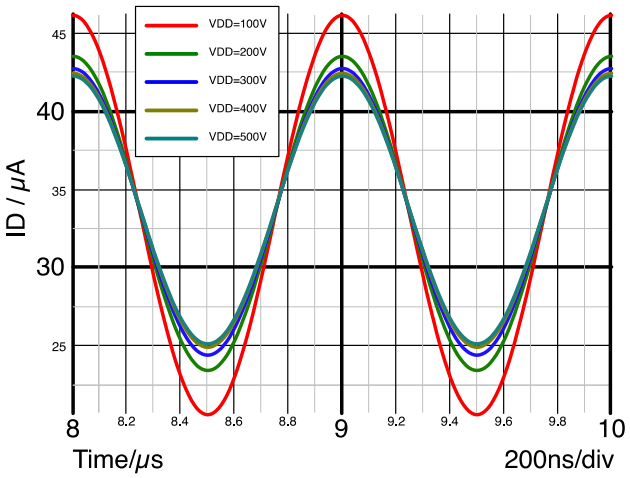

Figure 34. Drain Current Waveforms when the dc Drain−to−Source Voltage Change

in Figure 34, please note the presence of a dc current offset (around 32 µA) corresponding to the drain−to−source leakage current.

Solving equation (1) to get C_{OSS}, we obtain the following formula:

$$C_{oss} = \frac{1}{2\pi \times f} = \frac{(\text{Drain Current})_{Peak-to-Peak}}{(\text{Drain} - \text{to} - \text{Source Voltage})_{Peak-to-Peak}} \quad \text{(eq. 2)}$$

We implement this formula in an arbitrary−function probe to dynamically calculate C_{OSS} during simulation and plot its value, as shown in Figure 35. Since the measurement frequency has been defined as a parameter in the "Command Window" with the statement ".Param", we need to use the function "GetDotParamValue('Parameter Name')" to retrieve and use the parameter value. π is also treated as a parameter and obtained the same way.

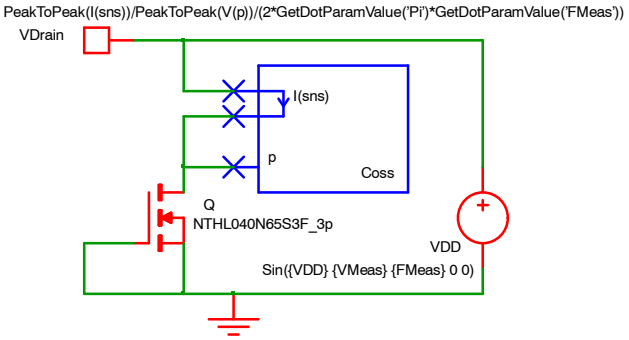

Figure 35. Small−Signal Capacitance Simulation Schematic with Arbitrary Probe

SIMetrix offers the possibility to plot a signal (here the arbitrary−function probe's results) as a function of the swept value (here the parameter VDD representing the continuous drain−to−source voltage value). This is done selecting the "Performance analysis" mode for the Multi−Step setup (see Figure 36). The swept value becomes the graph X−axis variable. The expression results are plotted on the Y−axis values.

Here is the setup of the arbitrary probe in Figure 36:

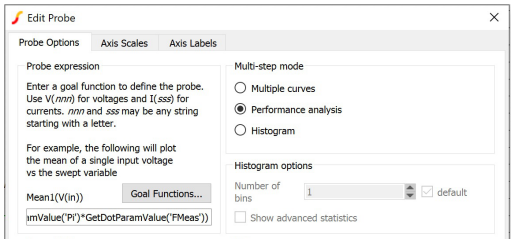

Figure 36. Arbitrary Probe Setup

After running the simulation, we get the graph displayed in Figure 37 using the same scales as the specification curve.

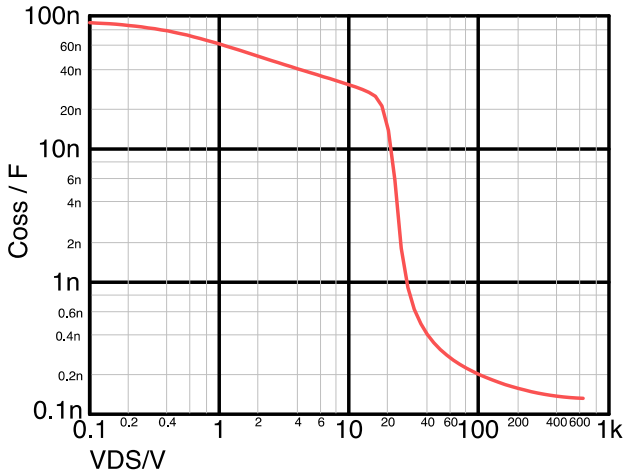

Figure 37. Small−Signal Capacitor Value versus Continuous Drain−to−Source Voltage

These measurements fit the datasheet results. As an example, for a drain−to−source equal to 400 V, we measured a C_{OSS} value of 142 pF in Figure 37 and this matches with 140 pF given in the datasheet.

Small Signal Value (2nd Method: AC Simulation).

In ac simulation, SIMetrix offers the possibility to sweep other parameters than frequency. Here, we will set the frequency to 1 MHz and sweep the drain−to−source dc voltage.

Using eq.(1), the C_{OSS} value can be calculated in the ac simulation via the following expression:

$$C_{oss} = \frac{I_{Dac}}{2\pi \times f \times V_{DSac}} \qquad \text{(eq. 3)}$$

The previous expression will be implemented in a special arbitrary−function probe to solve the C_{OSS} values depending on drain current and drain−to−source voltage as shown on schematic Figure 38.

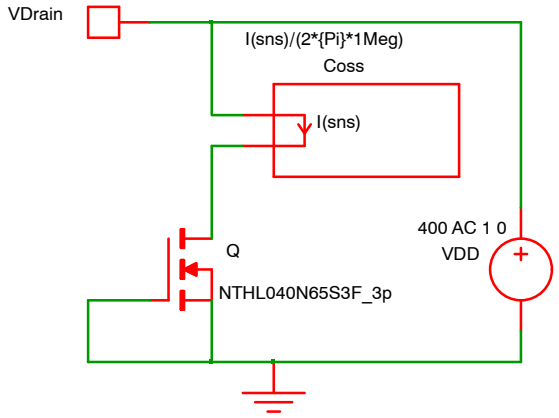

Figure 38. Small−Signal Capacitance Value Simulation Schematic

In ac simulation, SPICE linearizes the circuit after calculating the dc operating point. As the circuit is linear, we can apply any ac voltage amplitude without any saturation risk. To simplify the calculation, we can apply 1 V for the ac voltage amplitude.

The simulation setup can be found Figure 39:

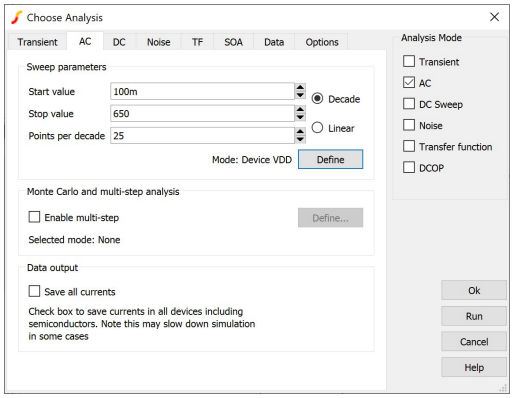

Figure 39. Small−Signal Capacitance Value Simulation Setup

The "Multi−Step" box should be unchecked. The swept values are the one for the continuous drain−to−source voltage: from 100 mV to 650 V, using 25 points per decade.

Additional setup needs to be placed under the "Define" button (see Figure 39) to set the way the sweep analysis will

be performed. In Figure 40, we define the device to sweep (VDD, the voltage source) and the ac frequency to be 1 MHz. The ac amplitude is set to 1 V.

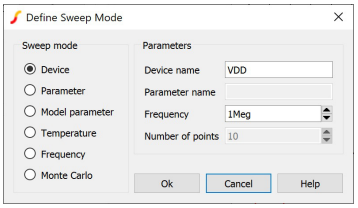

Figure 40. Small−Signal Capacitance Value Simulation Sweep mode Additional Setup

The obtained simulation curve can be seen in Figure 41.

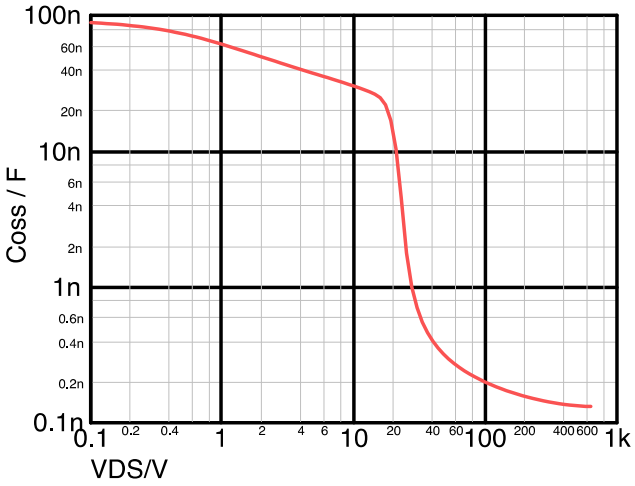

Figure 41. Small−Signal Capacitance Value Simulation Results

This curve (Figure 41) matches with the specification curve. In the “Dynamic Characteristics” table, the small−signal output capacitor is given for a drain−to−source voltage equal to 400 V. We measured a C_{OSS} value equal to 142 pF on the simulated curve above and this matches with 140 pF given in the specification.

The two methods give the same results.

Effective Value

The effective−capacitor value is defined in [7] as the equivalent linear capacitor storing the same amount of charge/energy with a voltage source equal to the breakdown voltage value while a 100−kΩ series resistor charges the output capacitor. This value can be used to calculate the switching time in resonant topologies.

The charging equation for the linear capacitor in this configuration is given by:

$$V_{DS}(Time) = V_{DD}\left(1 - e^{-Time/(RD \times C_{oss})}\right) \quad \text{(eq. 4)}$$

“Time” is the SIMetrix variable representing the current simulation time.

Solving this equation to determine the output−capacitor values, we obtain the following formula:

$$C_{oss} = \frac{Time}{RD \times \ln\left(\frac{V_{DD}}{V_{DD} - V_{DS}(Time)}\right)} \quad \text{(eq. 5)}$$

As previously done, this formula is used in an arbitrary function (or voltage source) to get the C_{OSS} value directly on the schematic (see Figure 42). We use an X−Y Probe to plot the C_{OSS} value versus drain−to−source voltage.

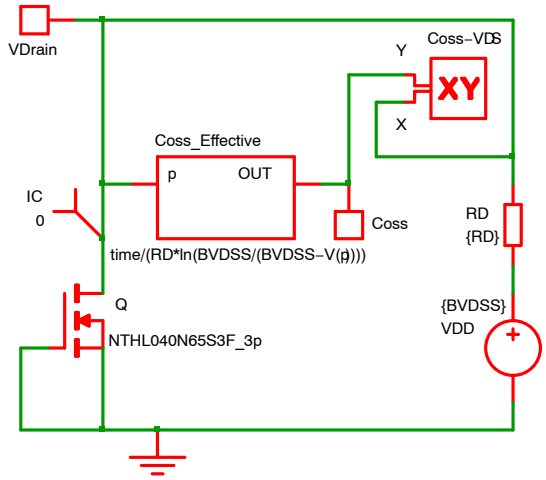

Figure 42. Effective−Capacitance Value Simulation Schematic

The values for the resistor (RD) and the voltage source (VDD) are set with parameters in the “Command Windows” (F11). The values are 100 kΩ and 650 V respectively. There are shown in the Figure 43.

```
.Param RD=100k
.Param BVDSS=650
```

Figure 43. Parameters Statements in the “Command Window”

We set an initial condition for the drain−to−source voltage to be equal to 0 V when the simulation begun using the “IC” pseudo−component, meaning the output capacitor is empty of charges (see Figure 42).

The obtained simulation curve can be seen in Figure 44.

In the “Dynamic Characteristics” table, the effective output capacitor is given for a drain−to−source voltage equal to 400 V. In Figure 44, we measured a C_{OSS} value equal to 1305 pF in the simulated curve and this matches with 1366 pF given in the specification.

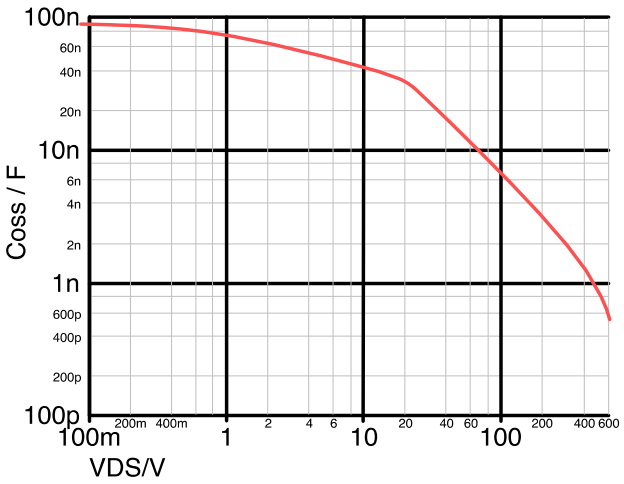

Figure 44. Effective−Capacitance Value Simulation Results

Energy−related Value

The energy stored in a capacitor is expressed by the following equation:

$$dW = v(t) \times i(t) \times d(t) \quad \text{(eq. 6)}$$

And, the final energy for a constant capacitor can be express by the following equation:

$$W = \frac{1}{2}CV^2 \quad \text{(eq. 7)}$$

If we integrate eq.(6) and replace in eq.(7), we can extract the capacitor value.

$$C_{oss} = \frac{2\int_0^{Time} V_{DS}(t) \times I_D(t) \times dt}{V_{DS}{}^2(Time)} \quad \text{(eq. 8)}$$

We use a current source to charge the output capacitor instead of a voltage source (in the effective−value setup). Here also, we use this formula in an arbitrary function to get the C_{OSS} value directly. We invoked the integral function "SDT()" to determine the numerator.

We also placed an initial condition for the drain to source voltage to be equal to 0 V when the simulation begun using the "IC" pseudo−component, meaning the output capacitor is empty of charges.

We obtain the simulation schematic shown in Figure 45.

Figure 46 displays the obtained simulation curve.

In the "Dynamic Characteristics" table, the effective output capacitor is given for a drain−to−source voltage equal to 400 V. We measured a C_{OSS} value equal to 245 pF on the simulated curve above and this matches with 247 pF given in the specification.

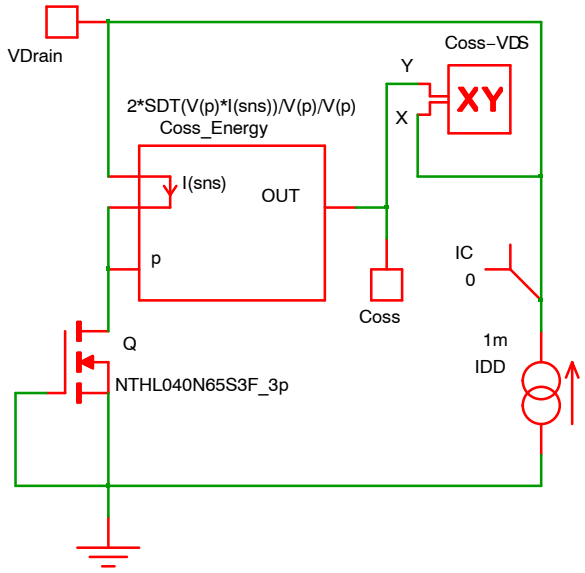

Figure 45. Energy−related Capacitance Value Simulation Schematic

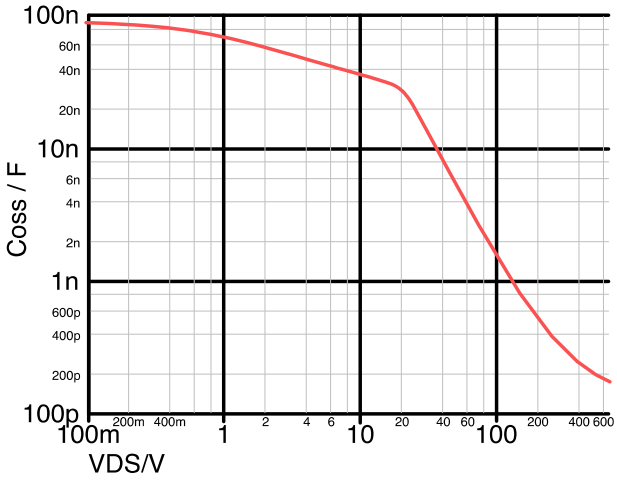

Figure 46. Energy−related Capacitance Value Simulation Results

Charge−related Value

The charge stored in a capacitor is expressed by the following equation:

$$dQ = i(t) \times d(t) \quad \text{(eq. 9)}$$

And, the final charge for a constant capacitor can be express by the following equation:

$$Q = CV \quad \text{(eq. 10)}$$

If we integrate eq.(9) and replace in eq.(10), we can extract the capacitor value.

$$C_{oss} = \frac{\int_0^{Time} I_D(t) \times dt}{V_{DS}(Time)} \quad \text{(eq. 11)}$$

We use a current source to charge the output capacitor. Same here, we use this formula in an arbitrary function to determine the C_{OSS} value directly. We use the integral function “SDT()” to calculate the stored amount of charges.

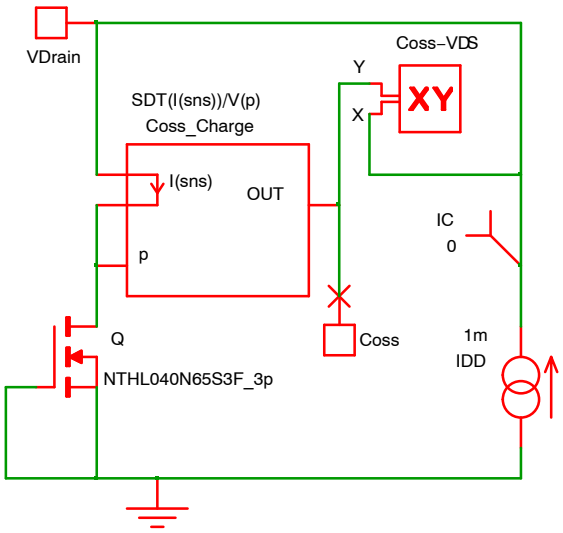

Figure 47. Charge−related Capacitance Value Simulation Schematic

We also placed an initial condition for the drain to source voltage to be equal to 0 V when the simulation begun using the “IC” pseudo−component, meaning the output capacitor is empty of charges. We obtain the simulation schematic from Figure 47.

Figure 48 shows the obtained simulation curve.

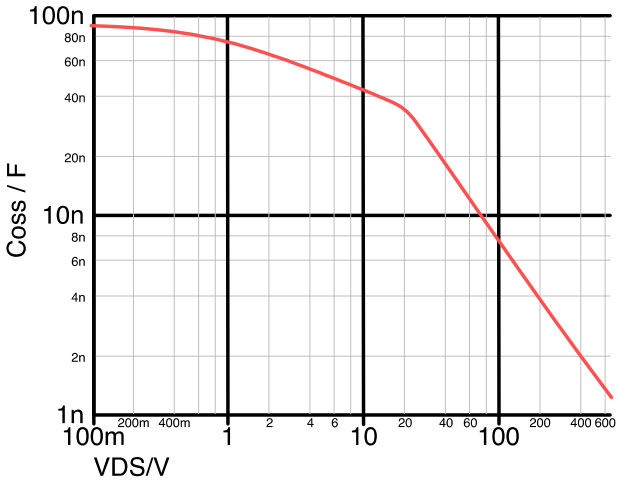

Figure 48. Charge−related Capacitance Value Simulation Results

BREAKDOWN VOLTAGE

The model gives the average values. The model is accurate within the specification limits. Results outside specification limits are not warranted by **onsemi**.

Nevertheless, the model can operate beyond the limits with relatively good accuracy and can predict values like the average breakdown drain−to−source voltage (BV_{DSS}). In the specification, only the minimum is given.

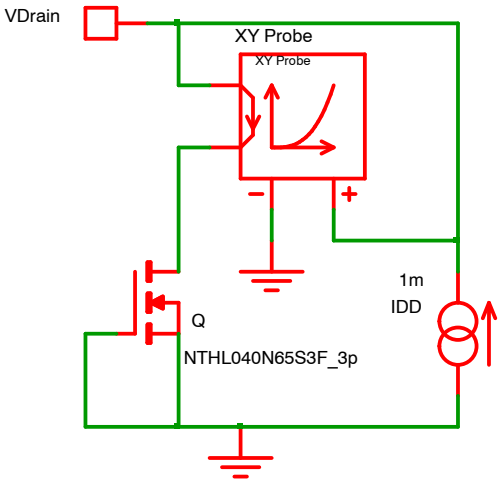

Figure 49. Breakdown Voltage Simulation Schematic

To simulate the breakdown voltage versus temperature, we will use a current source ramping up to 2 mA and plot the “off” characteristic. See Figure 49 schematic. (The specified minimum drain−to−source breakdown voltage value is given for 1 mA.)

The “off” state is obtained by shorting the gate to the source.

We will use an X−Y Probe to plot the drain−to−source voltage versus the drain current in “off” state as represented in Figure 50.

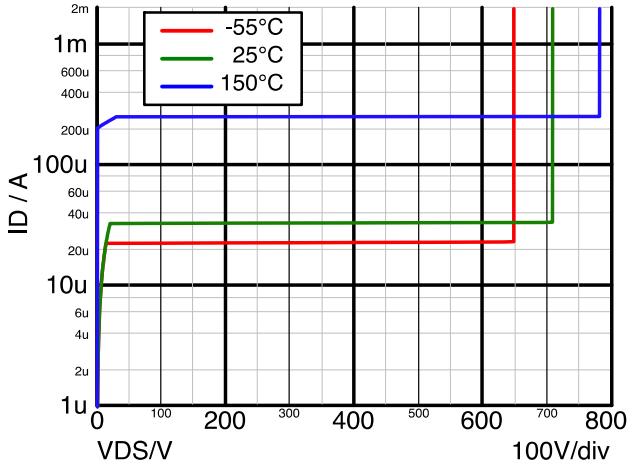

Figure 50. Breakdown Voltage Simulation Results versus Temperature

In Figure 50, we can note a leakage current variation with temperature. We can measure 23 μA, 33 μA and 254 μA for respectively −55°C, 25°C and 150°C die temperature at a drain−to−source voltage equal to 400 V. We see a big leakage current increase between 25°C and 150°C.

The drain to source breakdown voltage is equal to 648 V, 708 V and 781 V for respectively −55°C, 25°C and 150°C die temperature as shown in Figure 50.

BOOST POWER STAGE

Setup

In this chapter, we will use these scalable and physical models in a real application. We will study a boost converter stage with an Easy Drive SuperFET 3 and a 650−V SiC diode.

We will use the FCH040N65S3 for the boost switch. It is a 40−mΩ 650−V Easy Drive SuperFET 3 MOSFET.

For the boost diode, we will select the FFSB0665A. It is a SiC 6−A 650−V single diode.

The specification for the power stage is the following:

- Input voltage: 300 V,
- Output voltage: 420 V,
- Inductor current: 4 A,
- Inductor current ripple: 2 A,
- Switching frequency: 100 kHz,
- Case temperature: 90°C,
- Gate drive voltage: 10 V,
- Gate series resistor: 8 Ω

To avoid long stabilization time, we will close the loop. We will use a type 3 compensator with a voltage−mode pulse width modulator.

We will use arbitrary functions to calculate losses in the diode, in the MOSFET and the power to drive the MOSFET.

The “Per Cycle” measurement will be used to obtain the average losses for each cycle.

The schematic is shown in Figure 51.

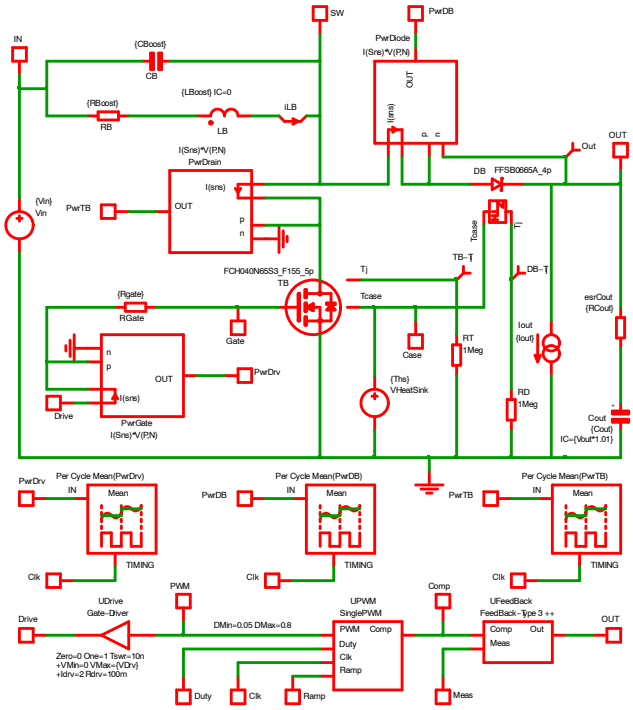

Figure 51. Boost Power Stage Schematic

In the annex section, the same schematic is shown in a bigger size in Figure 59.

Results

In Figure 52, we can see the power stage waveforms. We can observe a power stage reaching a stable point after 10 ms. The output voltage is equal to 420 V with a 300−V input voltage and an average current in the “pure” inductor (LB) equal to 4 A with ±1 A of ripple.

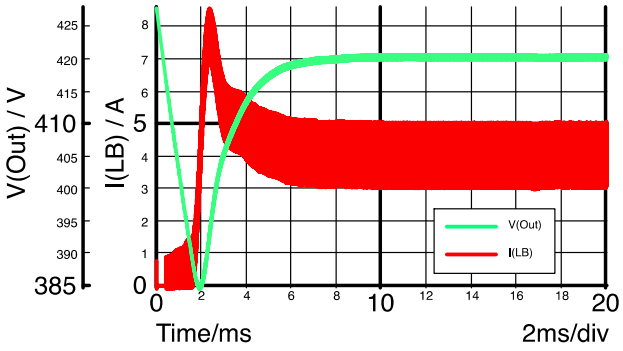

Figure 52. Boost Power Stage Waveforms

We can zoom at the simulation end (see Figure 53) and see the output voltage ripple plus the “real” (i.e. with parasitic capacitor CB in parallel) inductor current with the spike during the switch turn on and off. We can also plot the switching node voltage.

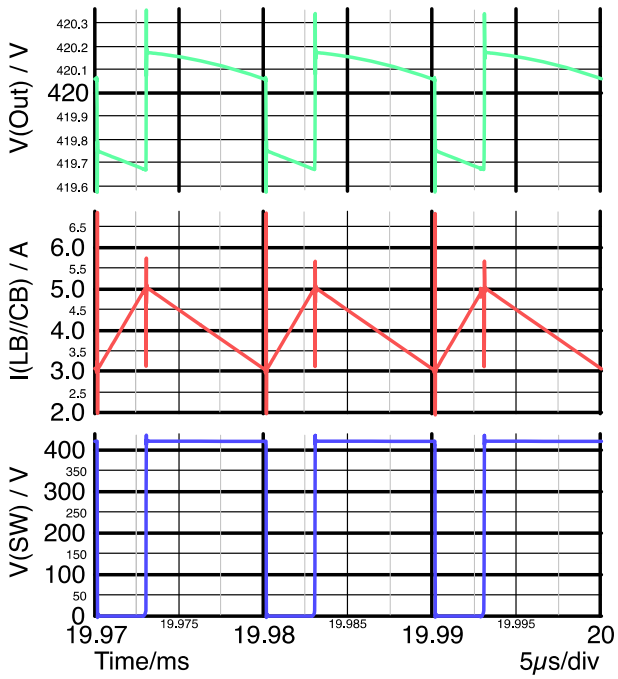

Figure 53. Zoom on Boost Power Stage Waveforms

With the 5−pin model for the MOSFET and the 4−pin model for the SiC diode, we can see (Figure 54) how much the junction temperature increases for each device.

The FCH040N65S3 (40−mΩ 650−V Easy Drive SuperFET 3 MOSFET) boost switch junction temperature increases by 1.5°C while the FFSB0665A (6−A 650−V SiC diode) boost diode junction temperature increases by 7.7°C. The diode package is a DPACK while the MOSFET is encapsulated in a TO247. The package size explains the temperature increase differences.

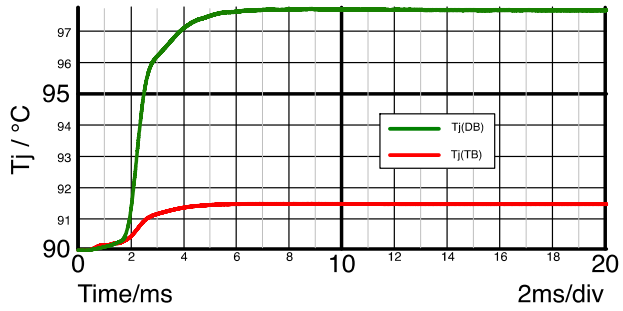

Figure 54. Junction Temperature Waveforms

We can also measure the losses in the switching devices on the waveforms from Figure 55.

When the power stage operates in stable conditions, the losses amount is around 5.0 W in the switch and 3.9 W in the diode. To drive the switch, we need around 260 mW.

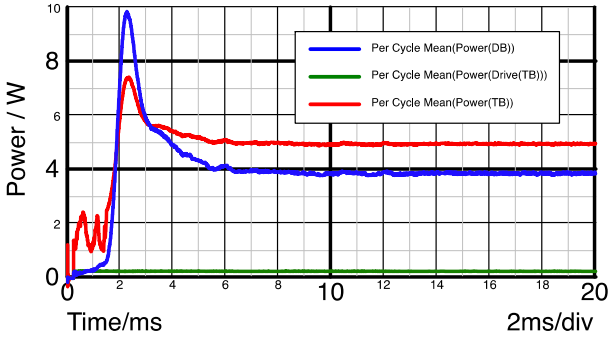

Figure 55. Averaging per Cycle Power Losses Measurement

Analysis Beyond the Waveforms

Using this power stage, we will analyze the effect of the inductor parasitic capacitor on the diode and switch losses. We will use four different values for this parasitic capacitor: 1 pF (almost nothing), 10 pF, 100 pF and finally 1 nF (a bad inductor).

In Figure 56, we can see the diode is not affected by this capacitor nor the driving power needed for the switch.

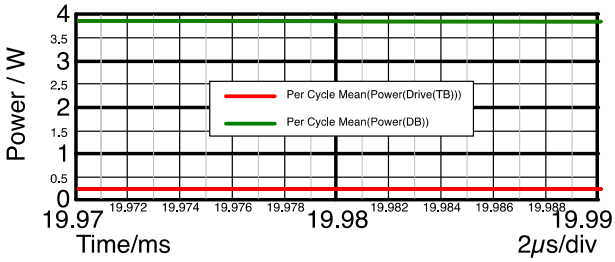

Figure 56. Diode Losses and Switch Driving Power versus Inductor Parasitic Capacitor

However, the switch losses increase with this capacitor as shown in Figure 57. We move from a 3.9 W loss budget with 1−pF parasitic−inductor capacitor to 14.0 W with a 1−nF parasitic−inductor capacitor. The switch junction temperature is affected accordingly.

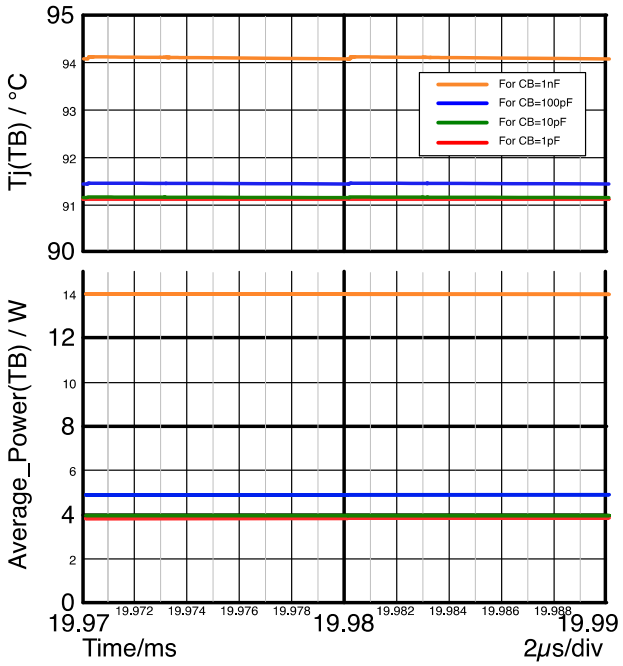

Figure 57. Switch Losses and Junction Temperature versus Inductor Parasitic Capacitor

We can measure the following values on the Figure 57:

Table 1. LOSSES AND TEMPERATURE VS INDUCTOR PARASITIC CAPACITOR VALUE (CB)

CB	Losses	Junction Temperature Increment
1 pF	3.9 W	1.1°C
10 pF	4.0 W	1.2°C
100 pF	4.9 W	1.4°C
1 nF	14.0 W	4.1°C

This analysis in Table 1 shows that not only the diode and switch performances are important to determine power stage losses, but, also the performances (or quality) of the boost inductor. The inductor losses are not so much dependent on the parasitic inductor capacitor but the switch losses are highly dependent on it. This parasitic inductor capacitor has the same effect as the switch output capacitor with a different operating mode. This parasitic capacitor plays the same role (increasing losses) and appears like being in parallel with the switch output capacitor.

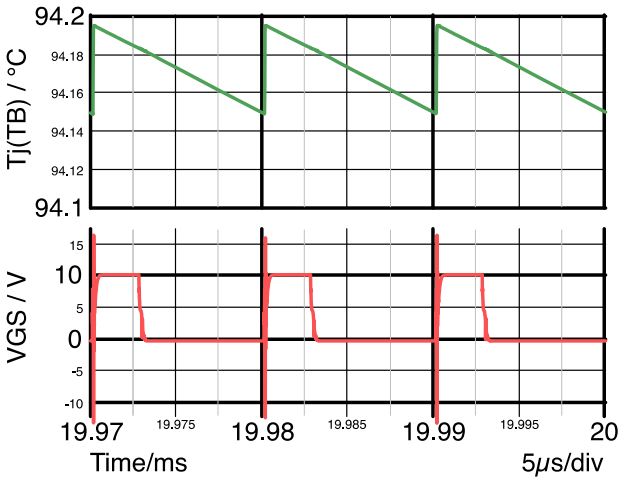

Figure 58. Junction Temperature Change when the Switch Turns On

If we zoom on the junction temperature waveform (Figure 58), we can see a sudden change of the temperature. This happens when the switch is turned on. At this particular moment, the switch output capacitor is rapidly discharged into the switch. It creates losses but the inductor parasitic capacitor is rapidly charged also bringing losses into the switch due to the high peak located on top of the “ideal” inductor current.

Optimizing the Power Stage

Now, using the same schematic, we can compare several MOSFETs and diodes to optimize the boost stage losses.

We keep the 100−pF inductor parasitic capacitor because this is a realistic value. The output power is equal to 1.2 kW.

We obtain the following Table 2 after several trials using a TO220 package for the diode and a TO247 for the MOSFET.

The last configuration with a 10−A SiC new generation diode (FFSP1065B) and 99−mΩ Easy Drive SuperFET 3 (FCH099N65S3) gives less losses... However, a 10−A SiC diode for an average output current equal to 2.8 A could be consider oversized thus expensive.

Running all these configurations can help to find the good compromise between performances and cost.

Table 2. LOSSES COMPARISON TABLE VERSUS DIODE AND TRANSISTOR PART NUMBERS

MOSFET (TB)	Diode (DB)	ΔT_J MOSFET	ΔT_J Diode	Drive Losses	MOSFET Losses	Diode Losses	Total Losses
FCH040N65S3	FFSP0465A	1.4°C	7.3°C	0.26 W	4.75 W	4.44 W	9.45 W
FCH040N65S3	FFSP0665A	1.5°C	10.0°C	0.26 W	4.98 W	3.88 W	9.12 W
FCH040N65S3	FFSP0865A	1.5°C	4.1°C	0.26 W	5.26 W	3.63 W	9.15 W
FCH040N65S3	FFSP1065A	1.6°C	3.9°C	0.26 W	5.46 W	3.41 W	9.13 W
FCH040N65S3	FFSP1265A	1.7°C	3.7°C	0.26 W	5.67 W	3.28 W	9.21 W
FCH040N65S3	FFSP0665B	1.4°C	13.5°C	0.26 W	4.80 W	3.80 W	8.86 W
FCH040N65S3	FFSP1065B	1.5°C	5.4°C	0.26 W	5.09 W	3.30 W	8.65 W
FCH067N65S3	FFSP0665B	1.6°C	13.6°C	0.15 W	3.90 W	3.80 W	7.85 W
FCH099N65S3	FFSP0665B	1.3°C	13.6°C	0.11 W	3.79 W	3.78 W	7.68 W
FCH125N65S3R0	FFSP0665B	1.7°C	13.6°C	0.09 W	3.85 W	3.79 W	7.73 W
FCH099N65S3	***FFSP1065B***	1.5°C	9.4°C	0.11 W	4.16 W	3.30 W	7.57 W

CONCLUSION

In this paper, we demonstrated the ability of the physical and scalable models to predict discrete components operation.

We can use these models to reproduce specification curves or parameters with very simple simulation setup. All these setups have been explained and results have been shown.

We can also use the models to extract parameters or generate curves when they are not available in the specification. For example, the on resistance change with temperature or with self−heating using models implementing “Junction temperature” and “Case temperature” extra pins. We can also see how self−heating affects a given operating area by monitoring the junction temperature.

They could also be used to determine parameters at a different operating point than the one given in the specification. For example, with the effective capacitor value, we can get the value for all drain to source possible voltage.

Finally, we have used these physical and scalable models in a real application simulation. We have created a boost power stage and run the simulations to get more information. We analyzed the losses in the switch as a function of inductor parasitic capacitor. We also calculate losses for several part numbers to determine the optimum boost stage configuration (MOSFET and diode).

Physical and scalable models can really help a designer to analyze components characteristics and optimize application performances.

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ANNEX: BOOST SCHEMATIC ZOOM

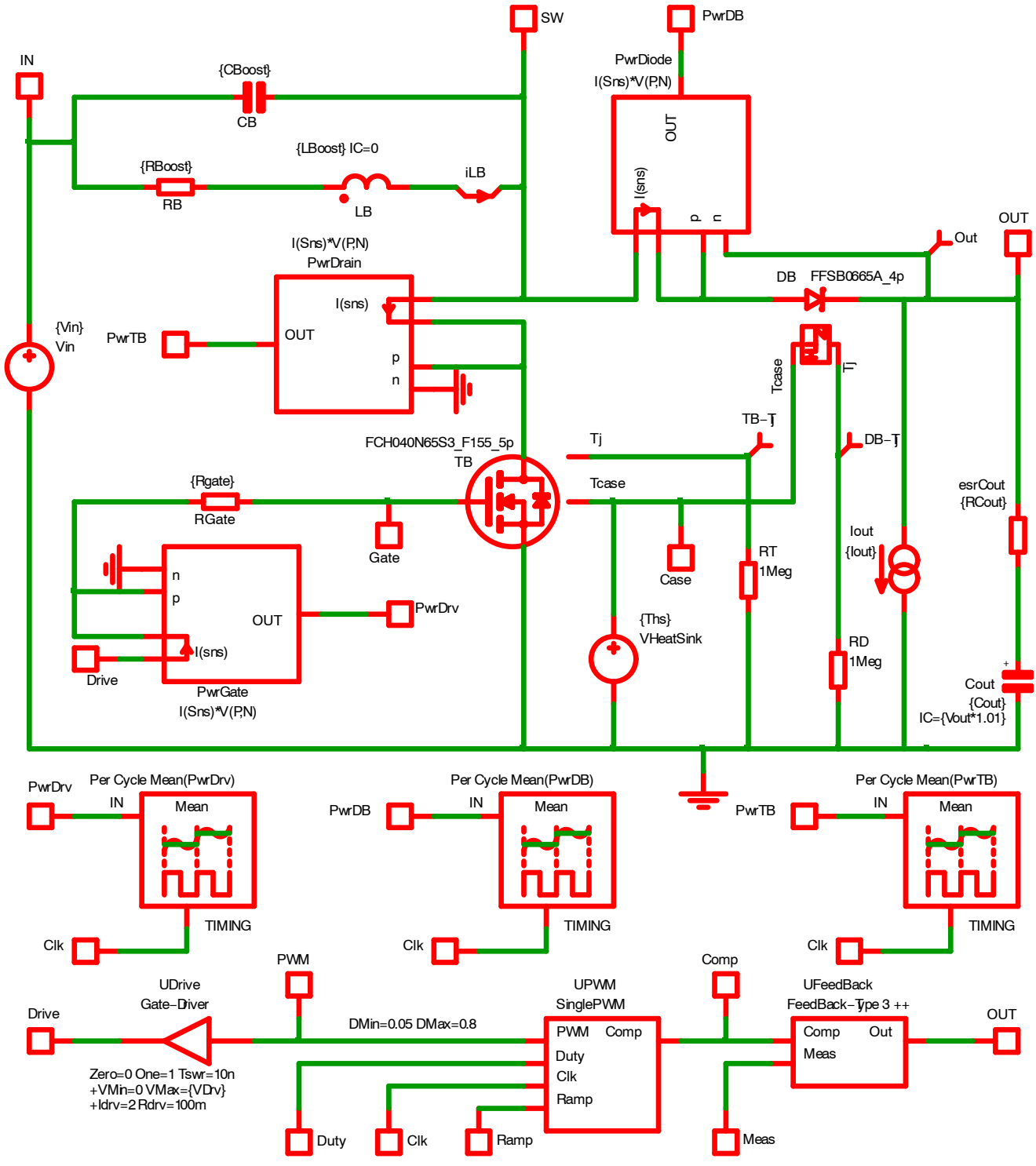

Figure 59. Boost Power stage Schematic

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