



Power Factor Correction — Optimization Options

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Abstract:

Environmental concerns lead to new efficiency requirements when designing modern power supplies. For instance, the 80 PLUS initiative and moreover its Bronze, Silver or Gold derivatives [1] force desktops and servers manufacturers to work on innovative solutions. An important focus is on the Power Factor Correction (PFC) stage which coupled to the EMI filter can consume 5% to 8% of the output power at low line, full load.

In general, relevant devices do not permanently operate at the maximum power they are designed for but only for short periods of time. Hence, for effective power savings, “green requirements” do not only target the full-load efficiency. Instead, they tend to cope with the actual operating conditions by specifying minimum levels for either the averaged efficiency or for the efficiency ratios at different loading situations like for instance 20%, 50% and 100% of the full power.

As a result, full- but also medium- and light-load efficiency ratios have become critical points to address. The paper will firstly discuss how the control scheme can help to optimize the efficiency over the load range while reducing the cost. In particular, it will be seen how the multi-mode approach can minimize losses over the whole load range. In a second step, architecture aspects will be considered with a focus on the bridgeless and interleaved approaches. Respective merits of these solutions will be compared in a 300-W, wide-mains application.

INTRODUCTION

The line utility provides a sinusoidal voltage but the shape and phase of the line current depend on the load. If the load consists of a reactive component, the current is phase-shifted. In the case of a nonlinear load, harmonic currents circulate needlessly and just contribute to an increased conduction losses.

As a result, if the line current is both phase-shifted and distorted, the real power also suffers from distortion and displacement factors:

$$P_{in,avg} = V_{line,rms} \cdot I_{line,rms} \cdot \cos(\phi) \cdot \cos(\theta) \quad (\text{eq. 1})$$

Where $\cos(\phi)$ and $\cos(\theta)$ respectively are the displacement and distortion factors.

The power factor is the product of the displacement factor (less than 1 if the line current and voltage are not in phase) by the distortion factor (less than 1 if the line current is not sinusoidal).

$$PF = \cos(\phi) \cdot \cos(\theta) \quad (\text{eq. 2})$$

The line voltage being assumed to be the well-controlled sinusoidal voltage generally provided by the electricity utility, you can immediately see that the line current will be inversely proportional to the PF for a given power demand:

$$I_{line,rms} = \frac{P_{in,avg}}{V_{line,rms} \cdot PF} \quad (\text{eq. 3})$$

Low power factor ratios are thus indicative of useless reactive currents flowing in the distribution network. As highlighted by Equation 3, this causes the line rms current and hence, the conduction losses to be increased. This also limits the power which can be absorbed from an outlet. For instance, if $PF = 0.5$, the line rms current is doubled compared to its value when PF is 1, thus limiting by 2 the power one can draw from a 16-A electric socket!

The EN 61000–3–2 specification, usually named Power Factor Correction (PFC) standard, has been issued with the goal of minimizing the Total Harmonic Distortion (THD) of the current which is drawn from the mains. In practice, the law specifies a maximum harmonic magnitude from the second up to the 40th order. Please note that in addition to the EN 61000–3–2 norm, PF specification is part of standards like Energy Star, what highly contributes to generalize the power factor correction use. Other standards exist for applications with input currents > 16 A (e.g., EN 61000–3–12) and for specific applications like aircraft.

Active solutions are the most effective means to meet the legislation. As illustrated by Figure 2, a PFC pre-regulator is inserted between the input bridge and the bulk capacitor. This intermediate stage is designed to deliver a constant voltage while drawing a sinusoidal current from the line. In practice, the step-up (or boost) configuration is adopted, because this type of converter is robust and easy to implement. One can just notice that this topology requires the output to be higher than the input voltage. That is why the output regulation level is generally set to around 400 V in universal mains conditions.

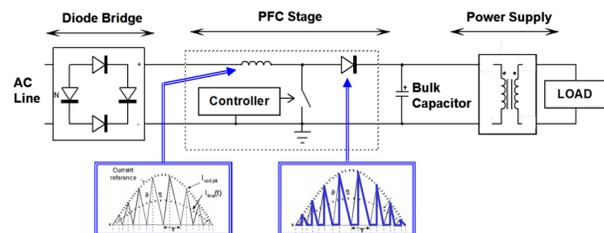


Figure 1. Power Factor Corrected Power Converter

This additional stage simplifies the design of the main downstream converter by providing it with a narrow input voltage. Also, the high-voltage dc-link (bulk) capacitor helps meeting hold-up time requirements while the non-pulsating input current of a boost converter eases EMI filtering. However, as aforementioned, efficiency is a major requirement for modern power supplies. A PFC

pre-converter is the seat of some losses which must be mitigated to meet today specifications. Figure 2 reports the efficiency performance of a 300-W, wide-mains PFC stage driven by the NCP1654 from **onsemi** [2]. The efficiency of a PFC boost converter is generally worse at low line. [3] instructs that an efficiency chart generally shapes as a bell curve peaking at an intermediate load level. From this top, the efficiency decays when the load rises because of the conduction losses while in the light-load side, it diminishes due to the constant and switching losses [4].

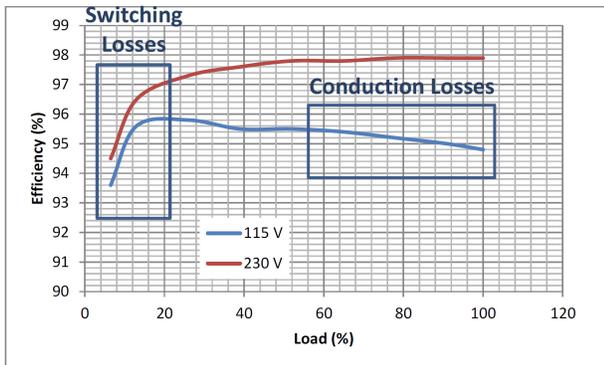


Figure 2. Efficiency over the Load Range of the NCP1654 Evaluation Board

We can identify two types of losses:

- First, the conduction losses increase as the load rises. Some of them are approximately proportional to the input power. Typically, these are those caused by diode forward voltage like in the input bridge as discussed later. Since they are a nearly constant portion of the input power, their impact on the efficiency is constant over the load range. Other are proportional to the square of the input current and hence at a given line level, to the square of the power. They consist of the dissipation of all the resistances present in the current path: the EMI filter parasitic resistances and the boost inductor ac resistance, the MOSFET on-time resistance, the current-sensing resistance or the bulk capacitor equivalent series resistance. Being proportional to the input power square, the negative impact of these losses on efficiency dramatically increases as the load rises. They typically cause the low-line, heavy-load efficiency drop shown in Figure 2. If we omit those incurred to the EMI filter, these losses are highly dependent on the inductor current ripple.
- Second, the switching losses consist of:
 - ♦ The energy lost when the current transitions from the power switch to the boost diode and vice versa. These losses are proportional to the current which is commuted and to the switching frequency. They also depend on transitions delays which result from components no-ideality (parasitic capacitances and current charge necessary to force the recovery of

a diode – Q_{rr}). These losses are proportional to the current and have a substantially-constant impact of the efficiency over the load if the frequency is fixed. The impact dramatically worsens in CrM since the switching frequency rises in light-load conditions.

- ♦ The energy necessary to manage the switching-mode power transfer, with mainly the commutation of the switching cell. These losses termed as constant losses in [4] are independent on the current which is commuted. For instance, the power necessary to drive the power switch can be expressed for a MOSFET as $P_{drive} = V_{CC} \cdot Q_g \cdot f_{sw}$, where V_{CC} is the voltage applied to the MOSFET gate, Q_g is the total gate charge necessary to charge the gate to V_{CC} and f_{sw} is the switching frequency. Also, the losses caused at turn on by the discharge of the MOSFET output capacitance are independent of the processed current unless a specific control law is in play. As such, they can be considered independent from the load and as a result, their impact on efficiency is generally minored at full load while considerably increased in light load. The degradation is even worse if the switching frequency increases at light load like with critical conduction mode circuits since the losses are no more constant but rising in the low-power range.
- ♦ The magnetic core losses which to some extent, could be included in the precedent category in continuous (CCM) and critical (CrM) conduction modes since the Steinmetz's equation ($P_C = k \cdot f_{sw}^\alpha \cdot (\Delta B)^\beta$) shows a dependence on the only magnetic field swing and switching frequency which both are constant in CCM and the variations of which tend to cancel in CrM.

To these losses, we can add the permanent power consumed by the PFC controller (V_{CC} consumption) and the dissipation caused by the different biasing currents like those of the high-voltage sensing networks. These losses can be a problem if high-efficiency ratios are required at very low power.

The full-load losses of a PFC boost converter should be mainly considered at the lowest line level where the efficiency is worse. The thermal management and power components selection will largely depend on them. Thus, based on the above rapid overview of efficiency nibblers, it appears that switching losses must be controlled at light load while the conduction losses are to be contained at full load, low line.

We will see in the next sections how PFC control schemes and architectures can help optimize the operation to reach this goal.

ONE-CHANNEL PFC TYPICAL OPERATION MODES

Figure 3 summarizes the basic control schemes in play in a PFC stage:

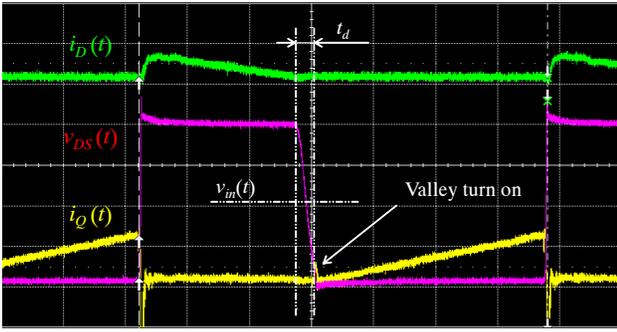


Figure 5. Valley Turn-on of the MOSFET (Measured on the NCP1612 Evaluation Board)

On the other hand, CrM has two major inconveniences:

- The inductor current ripple is large, thus leading to bulky input/output current filters. The ripple also implies, high rms currents within the boost converter and large copper/core losses within the inductor. This limits the cost-effectiveness and practical use of the solution for high-power applications.
- The switching frequency is variable and can reach high level particularly in light-load conditions, thus, altering the efficiency in this mode. The following equation provides a simplified expression (in which the delay to reach the valley is neglected) of the switching frequency as a function of the line voltage and of the input power:

$$f_{SW}(t) = \frac{V_{in,rms}^2}{2 \cdot L \cdot P_{in,avg}} \cdot \left(1 - \frac{V_{in}(t)}{V_{out}}\right) \quad (\text{eq. 6})$$

As it will be seen in the next section, the rise of the switching frequency dramatically pulls efficiency down in light-load conditions. Unfortunately, the degradation can only mitigated by the use of large inductors.

B. DCM Operation: a Good Idea?

[7] explains that clamping the switching frequency of a CrM PFC stage causes a dramatic line current distortion if no additional circuitry is added. **onsemi** has released several controllers like the NCP1612 or the NCP1632 which purposely embed a proprietary circuitry. Practically, these controllers sense the dead-time generated in the precedent switching cycles and based on this input, increases the on-time so that the averaged value of the current over one switching period remains what it would be in CrM.

This is what is shown by Figure 6: to maintain the same line current, we need a CrM peak current of $(I_{L,pk})_{CrM}$ while a higher one $(I_{L,pk})_{DCM}$ is necessary in DCM and:

$$i_{line}(t) = \frac{(I_{L,pk})_{CrM}}{2} = \frac{(I_{L,pk})_{DCM}}{2} \cdot \frac{t_{on,DCM} + t_{demag,DCM}}{T_{SW,DCM}} \quad (\text{eq. 7})$$

Where:

- $t_{on,DCM}$ is the on-time of the considered DCM cycle
- $t_{demag,DCM}$ is the demagnetization phase corresponding to $t_{on,DCM}$
- $t_{SW,DCM}$ is the DCM switching period

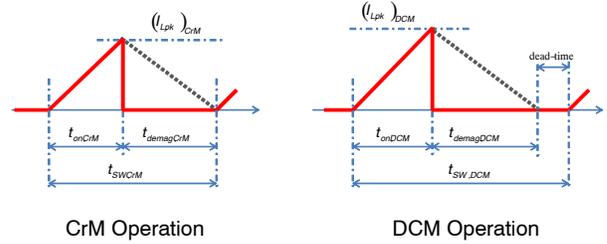


Figure 6. Power Switch Current in CrM (Left) and DCM (Right)

Note that the system is auto-adaptive in the sense that within a half-line cycle, the system can transition between CrM (typically at the top of the sinusoid) and DCM (typically near the line zero crossing) with no discontinuity in operation and no PF degradation. Simply, the on-time will be higher in DCM cycles and recovers its CrM duration when there are no dead-times. This ON proprietary scheme is named frequency-clamped critical conduction Mode (FCCrM). It can be associated to different frequency foldback modes like the gradual decrease of the switching frequency as a function of the load (NCP1631), the current-controlled frequency foldback (NCP1611/2) or the valley-switching frequency foldback (NCP1602/22).

The current shapes of Figure 6 suggest that the DCM mode causes higher conduction losses. [8] shows that clamping or even more reducing switching frequency (frequency foldback) can be counter-productive. Practically, the optimal frequency reduction is the ratio between the switching losses and the conduction losses when the converter operates in CrM. This means that if α is the $(f_{SW,CrM} \text{ over } f_{SW,DCM})$ ratio, where $f_{SW,DCM}$ is the DCM switching frequency and that $f_{SW,CrM}$ is the switching frequency if CrM operation was maintained, the optimal value for α is:

$$\alpha_{opt} = \frac{(P_{SW})_{CrM}}{(P_{cond})_{CrM}} \quad (\text{eq. 8})$$

Where $(P_{SW})_{CrM}$ and $(P_{COND})_{CrM}$ are respectively the switching and conduction losses of the PFC stage when operated in CrM. Switching losses being difficult to predict, it is difficult to theoretically and accurately find α_{opt} . Anyway, this means that since conduction losses are produced by the input current, the input current is a nice information to control the frequency foldback.

Following these efficiency considerations, **onsemi** released parts (NCP1611/2/5/6) to drive PFC boost stages in so-called Current Controlled Frequency Fold-back (CCFF). In this mode, the PFC stage operates in traditional critical conduction mode when the line current exceeds a programmable value. Conversely, when the current is below this preset level, the switching frequency decays down towards about 20 kHz as the line current reduces to zero.

Figure 7 shows how CCFF can reduce the switching frequency. These plots were obtained using the NCP1612 evaluation board [9]. The circuit lengthens the dead-time when the line current becomes smaller as it gets closer to the line zero crossing. Finally, a CCFF boost stage is intended to operate in CrM under heavy line current conditions and as the line current reduces, the controller enters discontinuous conduction mode operation. By the way, even in DCM, the MOSFET turn-on is stretched until its drain-source voltage is at its valley for an optimal power saving.

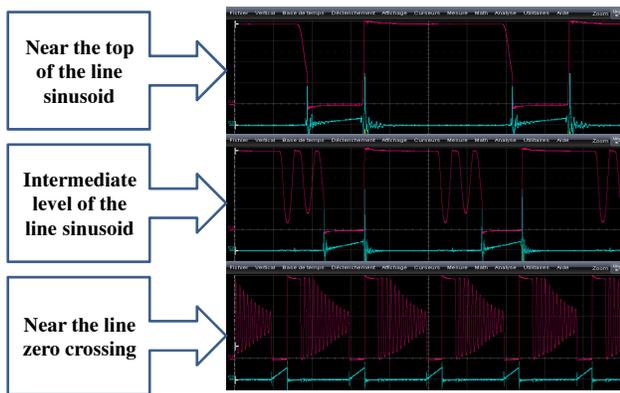


Figure 7. Operation @ 230 V, 160 W Near the Line Zero Crossing of the NCP1612 Evaluation Board. The MOSFET Drain-source Voltage is in Red, the Blue Trace Showing the MOSFET Current

Figure 8 reports data detailed in [9] obtained using the NCP1612 evaluation board. The CCFF efficiency is compared to that of a pure CrM circuit in the same board (by inhibiting the NCP1612 CCFF function). In addition, the NCP1612 can skip cycle near the line zero crossing where the current is very small (green trace). The efficiency ratios were measured at low and high line over a large power range (from 5% to 100% of full load). The right-hand side of the CCFF efficiency curves resembles that of a traditional CrM PFC stage. In the left-hand side, the efficiency normally drops because of the switching losses until an inflection point where it rises up again as a result of the CCFF operation. As previously detailed, CCFF makes the switching frequency decay linearly as a function of the instantaneous line current when it goes below a preset level. The CCFF threshold was set to about 20% of the line maximum current at low line, to nearly 45% at high line as confirmed by the aforementioned inflection points observed

in Figure 8. Thus, CCFF significantly improves efficiency below 20% of the load at low line while some benefit starts to become visible starting below 50% of the load at 230 V.

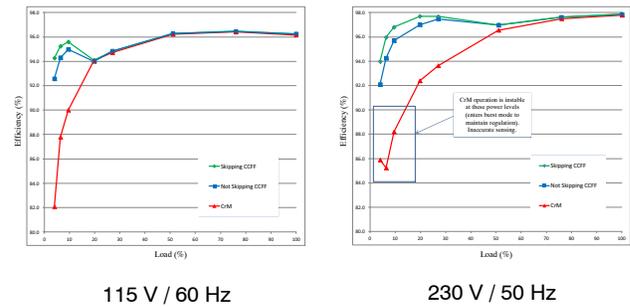


Figure 8. Efficiency over the Load Range at Low- and High-line Conditions

Frequency foldback is hence a very effective means to improve the light-load efficiency.

Note that the control of the switching frequency brings two other major benefits:

- Because of the propagation delays in the power switch control chain and the high switching frequency, CrM PFC stages generally cannot maintain a continuous operation below 20% of the load when operating at the highest line levels. Instead, they enter a burst-mode of operation. It can cause audible noise and the board may fail to pass THD specifications. Figure 8 illustrates that reducing the switching frequency solves this limitation. Thus, it should be noted that frequency foldback and in particular a CCFF circuit feature a stable operation down to extremely low power levels.
- In the absence of frequency clamp or frequency foldback, the only way to improve the light- and even medium-load efficiency is to increase the inductor value to lower the CrM switching frequency (since as instructed by Equation 6, the switching frequency is inversely proportional to L). In practice, experience shows that pure CrM PFC stages require an inductor in the range of $(45 \text{ mH} \cdot \text{W} / (P_{in,avg})_{max})$ (i.e., 300 μH for a 150-W, wide-mains application) while less than $(30 \text{ mH} \cdot \text{W} / (P_{in,avg})_{max})$ (i.e. 200 μH or less for the same 150-W, wide-mains application) is sufficient if the frequency is clamped. As an example, the NCP1631 wide mains, 300-W evaluation board runs with PQ26/20, 150- μH inductors [10].

C. Reducing Conduction Losses

We have seen that at low line, full load, conduction losses represent the main problem. The best solution consists of limiting the resistance and/or voltage drop of the components seen by the current. Now, to mitigate the heavy-load, low-line efficiency drop shown in Figure 2, it will mainly be necessary to reduce the resistive losses which rise as a function of the square of the input power. Thus, as

an example, it makes sense to try to reduce the series resistor of the EMI choke or use a lower $r_{DS(on)}$ MOSFET.

Above a given power level, such a solution becomes impractical and costly, causing continuous conduction mode to be preferred. As the rule of thumb, this power level is often said to be 300 watts but it may have increased due to newest components. However, the merit of CCM is to reduce the inductor current ripple which lowers the rms current circulating within the boost converter, as shown by Figure 9. The lower ripple offers several other advantages:

- Eased EMI filtering
- Less stress and lower heating of the capacitor

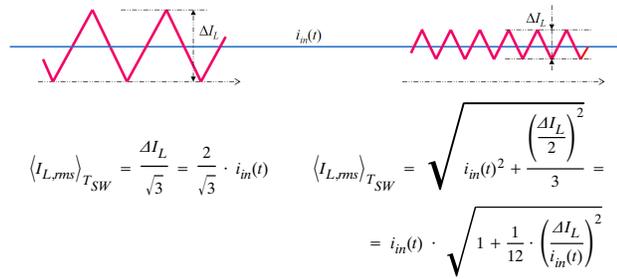


Figure 9. Reducing the Current Ripple to Lower its rms Value

Now, turn on losses are minimized in CrM since as aforementioned, the power switch closes at the valley and zero voltage switching can even be obtained if ($v_{in}(t) < V_{out}/2$). This is no more the case with CCM which adds significant turn on losses, particularly if slow-recovery boost diodes are used.

Low- t_{rr} diodes are hence to be preferred to minimize the turn-on losses which according to [11], can be computed as follows:

- Recovery boost diode losses:

$$P_D = \left(\frac{V_F \cdot I_L \cdot t_1}{2} + \frac{V_F \cdot I_{RRM} \cdot t_A}{2} + \frac{V_{OUT} \cdot I_{RRM} \cdot t_B}{6} \right) \cdot f_{SW} \quad (\text{eq. 9})$$

- Power switch turn on losses:

$$P_{Q,on} = V_{OUT} \cdot \left(\frac{I_L \cdot (t_1 + 2 \cdot t_A + t_B)}{2} + \frac{I_{RRM} \cdot (3 \cdot t_A + 2 \cdot t_B)}{6} \right) \cdot f_{SW} \quad (\text{eq. 10})$$

Where I_{RRM} , t_A and t_B are the following parameters also highlighted in Figure 10:

- I_{RRM} is the diode reverse recovery current
- t_A is the time between the diode zero crossing of the current and the peak reverse current.
- t_B is the time between the peak reverse current and diode actual opening.
- The sum of t_A and t_B is the reverse recovery time, t_{RR} ($t_{RR} = t_A + t_B$).

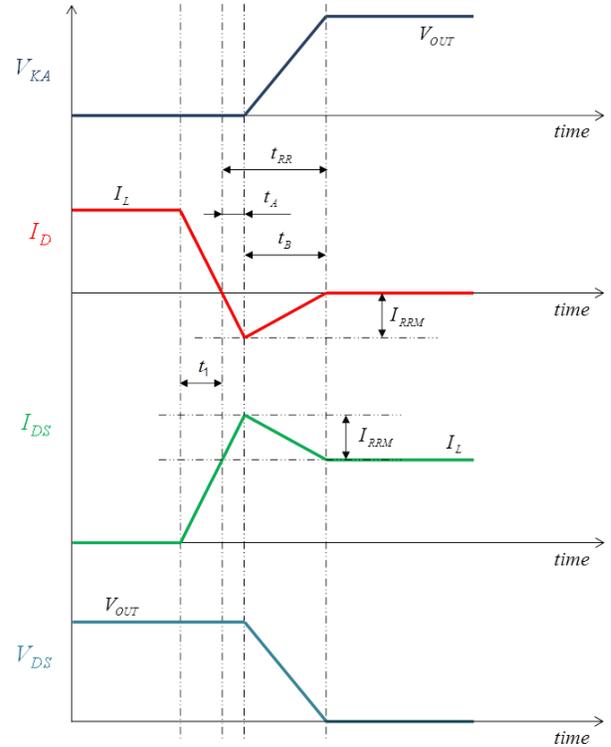


Figure 10. CCM Power Switch Turn-on Sequence

D. Multi-Mode Conduction Scheme

Multi-mode solution tries to combine the merits of each conduction mode and bring a high efficiency over the full load range:

- DCM in light load
- CCM in heavy load, low line where the input current is high and the inductor current ripple, ΔI_L , would be too large if the PFC was operated in CrM
- CrM otherwise

onsemi releases the NCP1618 which features such an operation mode:

- The circuit operates in CrM by default
- If the current cycle is shorter than a preset period (DCM period clamp of for instance 8 μ s for a 125-kHz DCM frequency), the circuit operates in DCM where the switching cycle is a bit longer than the preset period since the turn on is delayed until the valley is detected (left case of Figure 11)
- Transition between CrM and DCM can be managed cycle-by-cycle so that the circuit can transition from DCM to CrM and vice versa within a half-line cycle. Practically, DCM is more likely to occur near the line zero crossing and CrM at the top of the sinusoid.

- At very light load, the DCM period clamp is increased (a longer minimum switching period is forced causing frequency foldback), generally causing DCM operation over the whole half-line cycle)
- In heavy-load conditions, the circuit enters CCM when the current cycle is longer than the CCM period (about 15 μs for a 65-kHz CCM switching frequency). The circuit can leave CCM on a cycle-by-cycle basis. It permanently operates in CCM until no current cycle longer than the CCM period is detected for a blanking time of several line cycles. In other words, the circuit remains in CCM over the entire half-line cycle until the load is decreased enough to recover the DCM/CrM modes.

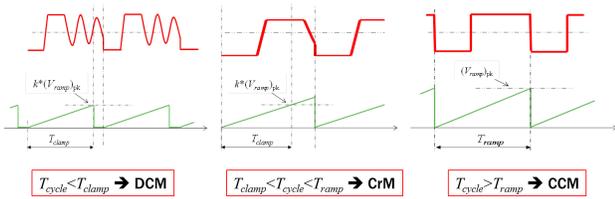


Figure 11. The Mode is Selected Based on the Switching Current Duration (T_{clamp} is the DCM Period Clamp, T_{ramp} is the Switching CCM Period)

From above description, we can deduce that the inductor selection will set the power above which the circuit will enter CCM. Equation 11 gives the CrM switching frequency as a function of the instantaneous line voltage. If we focus on the line sinusoid top, it comes:

$$f_{sw} \Big|_{v_{in}(t) = \sqrt{2} \cdot V_{in,rms}} = \frac{V_{in,rms}^2 \cdot (V_{out} - \sqrt{2} \cdot V_{in,rms})}{2 \cdot L \cdot P_{in,avg} \cdot V_{out}} \quad (\text{eq. 11})$$

We can then compute the power ($P_{in,transition}$) above which the above computed switching frequency at the top of the line sinusoid, is as low as the CCM switching one (f_{CCM}). Because of some hysteresis, 80% of f_{CCM} is actually to be targeted due to the system hysteresis.

$$L = \frac{V_{in,rms}^2 \cdot (V_{out} - \sqrt{2} \cdot V_{in,rms})}{2 \cdot 80\% \cdot f_{CCM} \cdot P_{in,transition} \cdot V_{out}} \quad (\text{eq. 12})$$

As an example, if we target $P_{in,transition} = 300 \text{ W}$ with $f_{CCM} = 65 \text{ kHz}$, a 180 μH inductor is to be chosen.

$$L = \frac{V_{in,rms}^2 \cdot (V_{out} - \sqrt{2} \cdot V_{in,rms})}{2 \cdot 80\% \cdot f_{CCM} \cdot P_{in,transition} \cdot V_{out}} \quad (\text{eq. 13})$$

INTERLEAVING CHANNELS

A 2-channel interleaved PFC converter consists of two paralleled PFC stages operated out-of-phase. Each individual stage is generally termed phase, channel, leg or branch. Figure 12 provides a simplified representation of an interleaved PFC driven by the NCP1632 from **onsemi** [12].

As a first interleaving merit, we can first note that 2 small PFC stages are to be designed instead of a larger one, somehow offering a modular approach. The interleaving solution requires more components but they are smaller and often more standard. These characteristics make the solution ideal for flat panels where the height of the components is critical like LCD TVs.

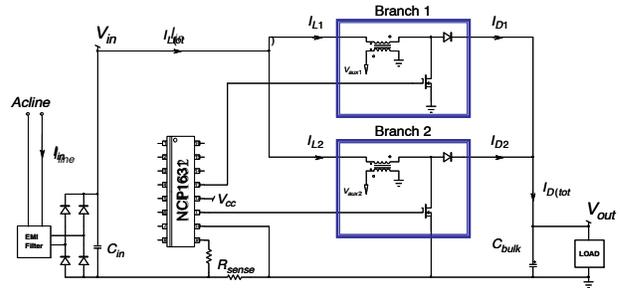


Figure 12. 2-channel Interleaved PFC Stage

Also, if the two channels are properly operated out-of-phase, a large part of the switching-frequency ripple currents generated by each individual branch cancel when they add within the EMI filter and the bulk capacitors. As a result, EMI filtering is significantly eased and the bulk capacitor rms current is drastically reduced. Interleaving therefore extends the CrM power range by sharing the task between the two phases. This allows a reduced input current ripple and a minimized bulk capacitor rms current [13]. As an example, Figure 13 sketches the input current absorbed by each channel (red trace for channel 1 and green trace for channel 2) by a two-channel CrM interleaved PFC. Starting from zero, they ramp up until a peak value is reached and then linearly return to zero. Their ripple is hence large, leading to a strong rms value which limits the power range of the CrM approach. Now since these two currents are out-of-phase, the total current absorbed from the input rail has a very small ripple and actually resembles the current absorbed by a hysteretic CCM PFC. Figure 15 shows that if the line peak voltage is below 50% of the output voltage, the input current looks like the input current of a hysteretic CCM PFC. A similar benefit can be observed in the output side.

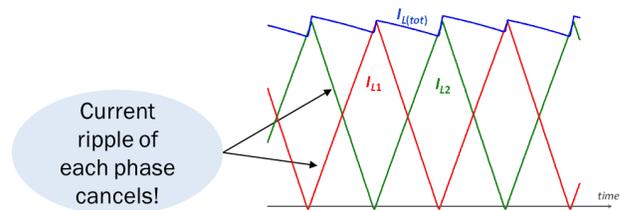


Figure 13. A Large Part of the Input Ripple Cancels

Figure 14 illustrates interleaving benefits on the output refueling current in a 300 W, wide-mains application. The output rms currents are reduced, thus minimizing the bulk capacitor heating and improving the application reliability.

	Single-phase CCM PFC	Single-phase CrM / FCCrM* PFC	Interleaved CrM / FCCrM* PFC
Diode(s) rms current ($I_{D,rms}$)	$I_1 = \sqrt{\frac{8\sqrt{2} \cdot \left(\frac{P_{out}}{\eta}\right)^2}{3\pi \cdot V_{in,rms} \cdot V_{out}}}$	$\frac{2}{\sqrt{3}} \cdot I_1$	$\sqrt{\frac{2}{3}} \cdot I_1$
C_{Bulk} rms current ($I_{C,rms}$)	$\sqrt{(I_1)^2 - (I_{out})^2}$	$\sqrt{\frac{4 \cdot (I_1)^2}{3} - (I_{out})^2}$	$\sqrt{\frac{2 \cdot (I_1)^2}{3} - (I_{out})^2}$
300-W, $V_{out} = 390$ V $V_{in,rms} = 90$ V	$I_{D,rms} = 1.9$ A $I_{C,rms} = 1.7$ A	$I_{D,rms} = 2.2$ A $I_{C,rms} = 2.1$ A	$I_{D,rms(to)} = 1.5$ A $I_{C,rms} = 1.3$ A

Figure 14. Comparison of the Bulk Capacitor rms Current in a 300 W Application

Furthermore, if the input current is well balanced, each channel processes half the total power. The size and cost of each individual branch is hence accordingly minimized and losses are spitted between the two channels. Hence, hot spots are less likely to be encountered. As an example, interleaving PFC stages require two boost diodes but each of them will only have to dissipate half the losses of the single boost diode of a 1-channel PFC. In addition, this load sharing may help save cost. Applications exist where two inexpensive axial diodes can do the job while a 1-channel PFC may need a more costly TO220 rectifier.

Conduction losses and current ripple can be further reduced by adding more branches. For instance, CCM controller FAN9673 [14] is designed to drive a 3-channel interleaved PFC with a 120-degree phase shift between branches.

This is why this approach which at first glance, may appear more complex and costly than the traditional 1-channel solution, can actually be extremely cost-effective and efficient for powers above 300 watts. As an example, it can be a very good choice, for applications like LCD and Plasma TV applications where the need for smaller components, although more numerous, helps meet the required low-profile form-factors.

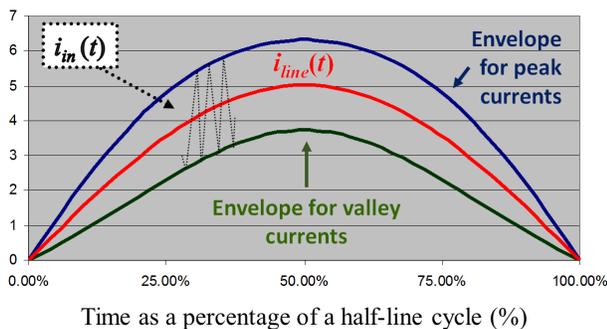


Figure 15. Low-line ($V_{in,pk} < V_{out}/2$), Peak, Valley and Input Current of a CrM Interleaved PFC

As a matter of fact, interleaving extends the CrM power range by sharing the PFC task between two phases and by allowing for a reduced input current ripple and a reduced bulk capacitor rms current. By the way, if one admits that a CrM PFC stage is very efficient up to 300 W, wide-mains, an interleaved PFC stage is very efficient up to 600 W, wide mains. Continuous improvements of the components tend to increase this power threshold. If interleaving merits were mainly illustrated by CrM-based solutions, discussed benefits remain similarly valid if CCM channels are interleaved.

THE BRIDGELESS OPTION

Figure 16 portrays the diodes bridge that is usually inserted between the EMI filter and the PFC stage. This bridge rectifies the line voltage to feed the PFC stage with a rectified sinusoid input voltage.

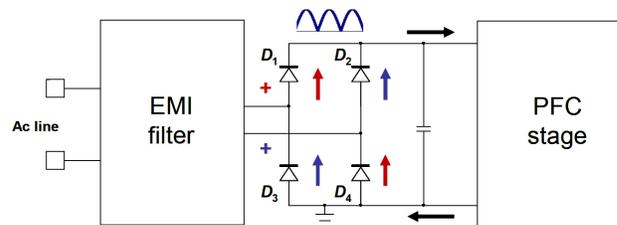


Figure 16. The Input Current Flows through Two Diodes

As a result of this structure, the input current must flow through two diodes before being processed by the PFC boost (D_1 and D_4 during a first half-line cycle – see red arrows of Figure 16, D_2 and D_3 for the other half-line cycle – blue arrows of Figure 16). As a matter of fact, two diodes of the bridge are permanently inserted in the current path. Unfortunately, these components exhibit a forward voltage that leads to conduction losses.

The mean value of the current seen by the bridge is the line average current.

Considering the input average current, [15] gives the following expression of the diodes bridge losses:

$$P_{\text{bridge}} = 2 \cdot V_f \cdot \langle I_{\text{bridge}} \rangle_{T_{\text{line}}} \cong 2 \cdot V_f \cdot \frac{2\sqrt{2} \cdot P_{\text{out}}}{\eta \cdot \pi \cdot V_{\text{in},rms}} \quad (\text{eq. 14})$$

Where:

- P_{out} is the output power
- η is the efficiency
- $V_{in,rms}$ is the rms line voltage

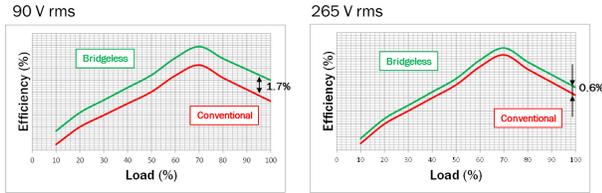


Figure 17. Typical Bridgeless Efficiency Gain over the Load Range @ 90-V (Left) and 265-V (Right) Line Voltages

Finally, if we assume a 850-mV forward voltage per diode and assuming a 90-V lowest line rms level $(V_{in,rms})_{LL} = 90\text{ V}$, it comes:

$$P_{\text{bridge}} \cong 2 \cdot 0.85 \cdot \frac{2\sqrt{2} \cdot P_{\text{out}}}{\eta \cdot \pi \cdot 90} \cdot \frac{(V_{in,rms})_{LL}}{V_{in,rms}} \quad (\text{eq. 15})$$

Or:

$$P_{\text{bridge}} \cong 1.7\% \cdot \frac{P_{\text{out}}}{\eta} \cdot \frac{(V_{in,rms})_{LL}}{V_{in,rms}} \quad (\text{eq. 16})$$

Where $(V_{in,rms})_{LL}$ is the lowest level of the line rms voltage.

In other words, Equation 16 instructs that the input bridge dissipation is inversely proportional to the line magnitude and that hence, it reduces at high line. For instance, the input bridge consumes about 1.7% of the input power @ 90-V rms and about 0.6% @ 265-V rms. Now, as shown by Figure 17, this percentage substantially remains the same over the load range assuming that the diode V_F voltage is not too affected by the conducted current. The diodes bridge conduction losses thus cause a significant efficiency drop over the whole load range and also a major hot spot affecting the application reliability. Eliminating it or at least one diode from the current path is thus of high interest. Here are the motivations behind the bridgeless approach.

2-BOOST APPROACH

As detailed in [16], several possible solutions are available from the “basic” dual-boost option or the promising totem-pole approach. We focus here on the 2-boost solution for its ease of implementation. Figure 18 portrays this bridgeless solution first proposed in [17]. Two PFC stages operate in parallel, one fed by one line terminal, the other by the other line terminal. This option eliminates the full-wave rectifier but the line negative terminal remains linked to the application ground by either diode D_1 or D_2 depending on the half-line cycle. Hence, the solution could be viewed as 2-boost PFC where the two branches operate in parallel:

- For the half-wave when the terminal “ PH_1 ” of the line is high, diode D_1 is off and D_2 connects the PFC ground to the negative line terminal (“ PH_2 ”). Thus, D_2 grounds the input of the “ PH_2 PFC stage” branch which hence, is inactive and the “ PH_1 PFC stage” processes the full power.

- For the second half-line cycle (when “ PH_2 ” is high), the “ PH_2 PFC stage” branch is operating and the “ PH_1 PFC stage” that has no input voltage, is inactive.

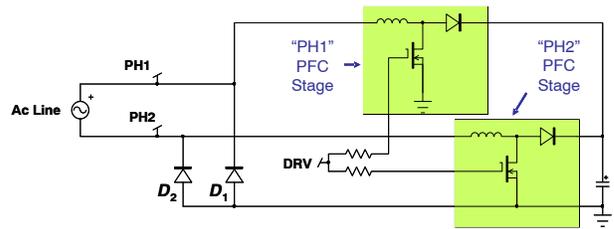


Figure 18. 2 Boost Architecture

Figure 19 gives an equivalent schematic for the two half-waves.

This bridgeless structure saves one diode in the current path and hence improves the efficiency.

One other interesting characteristic of this structure is that the active PFC stage behaves as a conventional PFC boost would do:

- When the “ PH_1 ” terminal is positive (see Figure 19a), diode D_1 opens and D_2 offers the return path. The input voltage for the “ PH_1 ” PFC stage is a rectified sinusoid referenced to ground.
- For the other half-wave (see Figure 19b), when “ PH_1 ” is the positive terminal, D_1 offers the return path. Diode D_2 is off and sees a rectified sinusoid that inputs the “ PH_2 ” PFC stage. Again, we have a conventional PFC where the input voltage and the boost stage are traditionally referenced to ground.

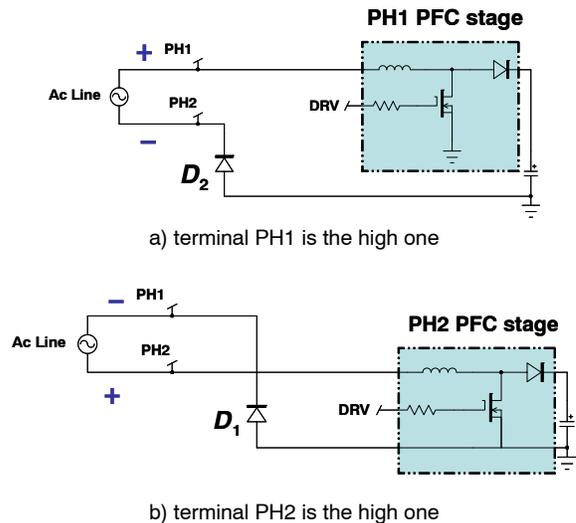


Figure 19. Equivalent Schematic for the Two Half-waves

It is also worth noting that the 2-boost structure does not require any specific controller. The MOSFETs of the two

branches are referenced to ground and they can be permanently driven even during the idle phase.

It is worth noting that the body diode of the inactive MOSFET provides the current with another return path. The inductance exhibiting a low impedance at the line frequency, we have two diodes in parallel and the current share between them. That is why current sensing generally requires a special attention like the use of current sense transformers [15].

INTERLEAVED VS. BRIDGELESS PFC

Two wide-mains, 300-W PFC stages shown in Figure 20 are compared.

The two boards are controlled by a FCCrM driver (NCP1605 for bridgeless, NCP1631 for interleaved).

Inductors are hence to be designed to operate in CrM in the most stressful conditions while DCM limits the switching frequency at light load and near the line zero crossing. Note that since the frequency is clamped, there is no need to over-size the inductor to avoid excessive frequency levels at medium load.

The two boards embark the same input bridge, the same MOSFETs (one 250-mΩ or one 99-mΩ $r_{DS(on)}$ MOSFET per branch), the same boost diodes (axial ultrafast MUR550) and an identical 2.9-°C/W heat-sink. The two boards also share similar components for the EMI filter even if the reduced ripple of the input current significantly eases the differential mode filtering in the interleaved PFC. The NCP1605 and the NCP1631 are both powered by an external 15-V power source.

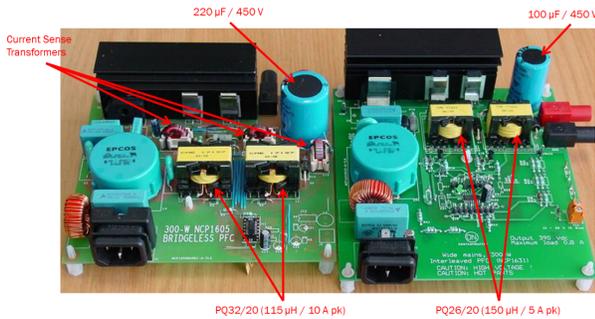


Figure 20. Pictures of the Two Boards: Interleaved PFC (Left) and Bridgeless PFC (Right)

The 2-boost bridgeless solution generates the same rms current in the bulk capacitor as a single-channel PFC while one of the interleaved merits is to reduce it (1.3 A instead of 2.1 A). In order to have the same stress in both applications, the semi-bridgeless stage embeds a 220-µF/450-V capacitor while a 100-µF/450-V is mounted on the interleaved board.

Another significant difference is in the inductor selection. Each inductor of the 2-boost bridgeless drives the total power for one half-line cycle over two when each inductor of the interleaved PFC processes permanently half of the power. The current stress is hence higher in the bridgeless case.

The frequency clamp is set to 130 kHz for each branch of both solutions. To do so, PQ26/20, 150-µH inductors equip the interleaved PFC while the 2-boost bridgeless application incorporates bigger PQ32/20, 115-µH chokes.

For the sake of consistency, the standby management featured by the two controllers (soft-skip mode for the NCP1605 and frequency fold-back for the NCP1631) are disabled for a fair comparison of the intrinsic efficiency performance of each concept over the power range.

An exhaustive losses analysis between the two systems is difficult to perform. However, [18] shows that the two options designed to operate in the same frequency range exhibit similar switching losses.

[18] also highlights that each system brings one major benefit regarding the conduction losses:

- As above discussed, the 2-boost bridgeless PFC saves the losses of one diode in the current path.
- The input current is equally divided between the two branches of the interleaved PFC while in the bridgeless case, only one branch is active at a time and it sees the total input current. The rms current in each of the interleaved PFC MOSFETs is twice the rms current in the active MOSFET of the 2-boost bridgeless PFC. As a consequence, the conduction losses in each interleaved PFC MOSFET are four times those of the semi-bridgeless active MOSFET. Now, as there are two MOSFETs working in parallel in the interleaved application, the conduction losses are twice in the interleaved case compared to the 2-boost bridgeless one. Here is a clear advantage for the interleaved PFC: if the same MOSFETs are used, conduction losses are 2 times lower in the interleaved solution:

$$(P_{\text{cond}})_{\text{Interleaved}} = 2 \cdot \left[\frac{4 \cdot r_{DS(on)}}{3} \cdot \frac{\left(\frac{P_{\text{out}}}{2 \cdot \eta}\right)^2}{V_{\text{in,rms}}^2} \cdot \left(1 - \frac{8\sqrt{2} \cdot V_{\text{in,rms}}}{3\pi \cdot V_{\text{out}}}\right) \right] \quad (\text{eq. 17})$$

Which leads to:

$$(P_{\text{cond}})_{\text{Interleaved}} = \frac{(P_{\text{cond}})_{\text{Bridgeless}}}{2} \quad (\text{eq. 18})$$

We could easily check that the boost diodes dissipate a similar power in both approaches.

Finally, if we assume the same losses for both applications in the inductors, the bulk capacitor and the EMI filter, we can note that each approach brings an efficiency advantage.

Simply, the 2-boost bridgeless approach saves an identical portion of the output power and leads to approximately the same efficiency improvement at full or light load. Closed to 0.85% at low line (90 V rms), the savings drop to about 0.3% at high line (270 V rms).

The power savings of the interleaved PFC are proportional to the square of (P_{out} over $V_{\text{in,rms}}$). Thus, they are maximum at the most stressful conditions (full load, low line) and rapidly decay as the load decreases or the line magnitude becomes higher.

These most stressful conditions must be considered when dimensioning the components and the board cooling system. We can compute a MOSFET on-time resistance ($r_{\text{DS(on)}}$) for which both the bridgeless and interleaved options provide the same savings. In our 300-W application, 410 mΩ is the resistance which is not far from the on-time resistance of our 250-mΩ MOSFET at 110°C (250 mΩ is the $r_{\text{DS(on)}}$ @ 25°C and this resistance is roughly multiplied by 1.8 at high temperature). This is confirmed by Figure 21 which shows no bridgeless benefit at full load with the 250-mΩ MOSFET.

In other words, high $r_{\text{DS(on)}}$ MOSFETs cancel the bridgeless advantage with respect to the interleaved solution while with low $r_{\text{DS(on)}}$ MOSFETs which reduces the weight of the MOSFET conduction losses, it is possible to obtain the full efficiency benefit obtained by saving half the power consumed by the input diodes bridge of a traditional PFC stage.

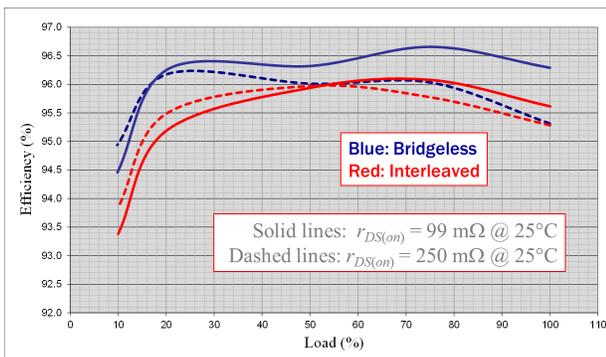


Figure 21. Efficiency Comparison @ 90 V rms

The portion of the load power saved by the bridgeless PFC is inversely proportional to the line magnitude. At 230 V rms, the gain is hence limited but not necessarily negligible (about 0.25%). As for the interleaved PFC, savings are proportional to the square of the ratio (power

over line voltage magnitude). Hence, its savings are very low at full load to null at light load.

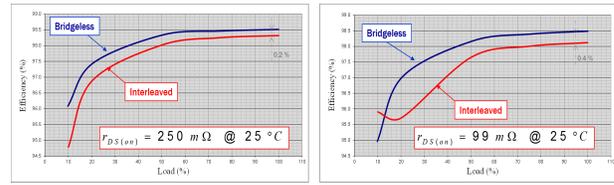


Figure 22. Efficiency Comparison @ 230 V rms

This is what Figure 22 confirms:

In the left, experiments were performed with the most resistive MOSFET (250-mΩ $r_{\text{DS(on)}}$), while, in the right, we used the lowest $r_{\text{DS(on)}}$ (99-mΩ). We see that the bridgeless option is more efficient in both cases and the gap is more significant at light load. The interleaved PFC performance are worse with the lowest $r_{\text{DS(on)}}$ MOSFET particularly at light load. This can be explained by the capacitive turn-on losses which were neglected till now. When the MOSFET turns on, it dissipates the energy stored by the lumped capacitor attached to its drain. The lowest $r_{\text{DS(on)}}$ MOSFET exhibits a higher output capacitance (130 pF vs 63 pF). Note that the interleaved PFC has two branches switching in parallel versus the semi-bridgeless in which only one channel operates at a time. The influence is then more significant in the interleaved PFC.

As a conclusion, the 2-boost bridgeless structure appears to be the most efficient at low line. This is particularly true if low $r_{\text{DS(on)}}$ MOSFETs are used. In this case, it brings the full efficiency advantage obtained by saving half the power consumed by the input diodes bridge of a traditional PFC stage. If not, the gain is moderate compared to an interleaved PFC.

Note that that as the line increases, bridgeless benefits reduce. Practically, bridgeless should be preferably envisaged in applications where the line magnitude can be low.

As already pointed-out, the bridgeless gain is line-dependent but the efficiency percentage point increase remains substantially the same over the load range. Hence, light-load performance is also improved.

Clearly, the bridgeless approach is more complex and expensive and hence seems to be reserved to applications with efficiency targets impossible to be met by traditional solutions. A bit less efficient, interleaved PFC is a more compact and cost-effective solution.

CONCLUSIONS

CrM is a popular and efficient solution for low power, particularly offering valley- and even zero-voltage-switching when the instantaneous line voltage is below 50% of the output voltage. However, its major drawback lies in the wide switching frequency variation which affects efficiency particularly at light load (high switching losses).

Frequency clamp and frequency reduction techniques are hence necessary if high efficiency is targeted at low power.

In addition, frequency clamp helps optimize the inductor size and cost since the inductance does not need to be oversized to limit the switching frequency at medium- and light-load and maintain high-efficiency ratios.

Continuous conduction mode becomes necessary at power levels causing too high an input current ripple which would be uneconomically addressed in CrM, unless an interleaved multi-channel approach is used.

In both CrM and CCM, interleaving offers a modular approach with more but smaller components and easier thermal management. This option increases the CrM power range or improves a CCM solution by mainly dramatically reducing the current ripple.

Bridgeless solutions cost but they further improve the efficiency particularly at low line. It is noticeable that the efficiency gain remains approximately the same over the whole power range. If you cannot meet your efficiency specification, this looks like the ultimate solution to consider.

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