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Quad MOSFET Approach Delivers Dramatic PoE Efficiency Improvements over Diode Bridge Alternatives

ON Semiconductor®

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While wireless connectivity offers many significant benefits, it is not yet ready to completely replace hard-wired network connections. Wired connections can still provide a number of advantages – including reliability, security and the ability to transmit power through the network itself. 'Power over Ethernet' (PoE), for example, reduces the amount of wiring needed to establish a network with remotely powered devices by removing the need for a separate power cable for devices.

Implementing PoE brings many advantages, whether it is a new installation or a retrofit/ upgrade:

- *Time and Cost Savings* – as no power cables are needed costs and installation time are reduced. The installation is also simplified as mains wiring regulations do not apply and a qualified electrician is not required.
- *Flexibility* – proximity to a power source is no longer a consideration. Equipment can be placed wherever LAN cables can be run.
- *Reliability* – The centralized power source replaces low-cost wall adapters and allows the system to be backed up by a single uninterruptible power supply.

PoE Networks

There are several methods for configuring a PoE network. The preferred approach depends on a variety of factors including network size and whether PoE is being added as an upgrade or as a completely new installation.

A PoE switch is a standard network switch that has PoE capability built-in. As network devices are connected to the switch, it will detect whether they are PoE-compatible and enable power automatically. Adding PoE capability to existing networks or provide a versatile solution where fewer POE ports are required can be achieved by using a midspan (or PoE injector). Each network connection that requires PoE is patched through the midspan, and as with POE switches, power injection is controlled and automatic.

The 802.3af PoE standard was developed for network devices requiring power levels up to 13 W. Some more sophisticated devices require more power so 802.3at (or POE Plus) was introduced by the IEEE to support powers up to 25.5 W. 802.3at exists alongside the 802.3af standard and does not replace it. Indeed, 802.3af will remain in use by the majority of PoE devices for the foreseeable future. That's why PoE Plus is backwards compatible with 802.3af, with higher power devices restricting the power they use when operating with the older standard. It also introduces smart power budgeting whereby devices can communicate and negotiate for the power they need.

However, as networks get larger and more complex with more devices attached, so the requirement for power increases. *New generations of IoT devices, for example are likely to require 25.5 W or more*. In the context of rising energy costs, demands for ever smaller solutions, the need to comply with multiple standards and address restricted budgets, this presents a number of challenges to the designer. Challenges that can only be met using ever more advanced power conversion semiconductors that operate with high levels of efficiency and low levels of heat generation in a compact space.

A Power Device (PD) in a PoE application requires a bridge circuit to regulate the polarity of the input power when the Power Source Equipment (PSE) supplying power to the PD is equipped with an Uninterruptible Power Supply (UPS). A simple diode bridge design has been the most popular approach to this, providing a reliable and low cost solution. However, as PDs require more power, the conduction loss of the diode bridge caused by the forward voltage drop becomes one of the main issues to be solved efficiently. ON Semiconductor's GreenBridge™ solution has been developed to address this issue by reducing power losses in the bridge circuit and delivering an efficient and cost-effective PoE system.

Introducing GreenBridge

To improve the conduction loss and efficiency of the conventional diode bridge, ON Semiconductor developed its GreenBridge family. The first generation of these devices integrated dual P-channel and dual N-channel MOSFETs into a compact and thermally enhanced surface mount package as shown in Figure 1. The specifications for this device are shown in Table 1.

Table 1. PERFORMANCE PARAMETERS FOR THE FDMQ8203 GreenBridge QUAD MOSFET

Column Head	MOSFET	BV_{DSS} (V)	$R_{DS(ON)}$ (mΩ)	Q_g (nC)	Θ_{JA} (°C/W)
			Max.	Typ.	
FDMQ8203	Q1, Q4	100	110	2.9	50
	Q2, Q3	−80	190	13	

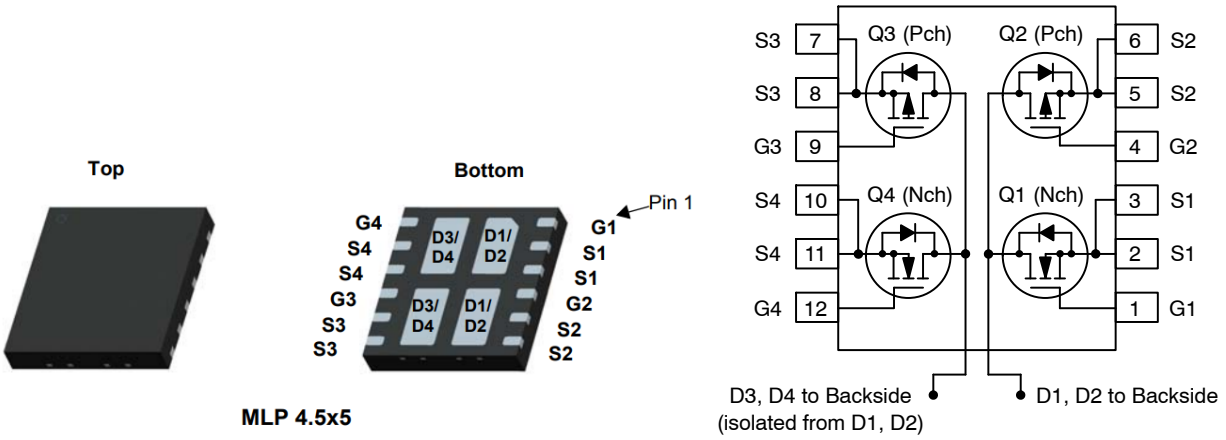


Figure 1. Internal Configuration and Pin Assignment

The high-performance MOSFETs in the GreenBridge solution replace diodes in a classic bridge embedded in the PD. This regulates power polarity from the PSE and, as this is a non-switching application, all of the power loss is conduction loss – directly proportional to the $R_{DS(ON)}$ value of the MOSFETs.

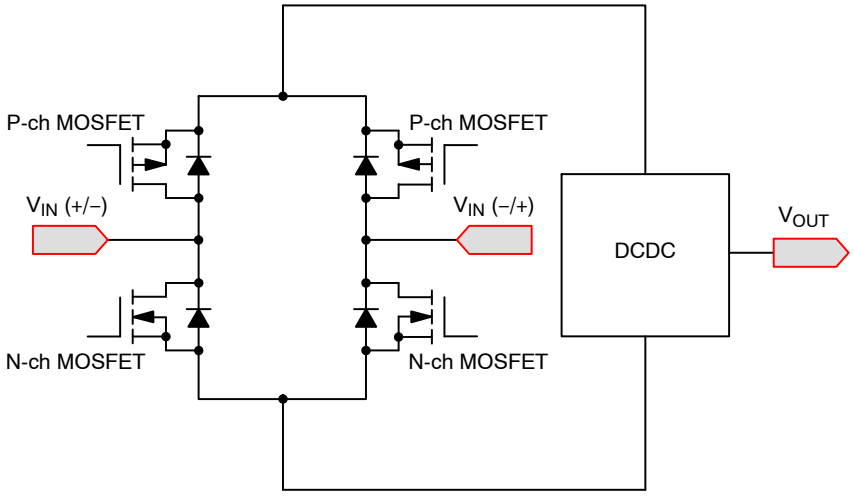


Figure 2. GreenBridge Solution Showing Bridge Formed from MOSFETs

As power (V_{IN}) is applied, current flows through one branch of the bridge. This is the same as with a diode bridge, except that the conduction losses are lower as the MOSFET losses are lower than those related to V_F in a diode.

The power loss for a conventional diode bridge is given by:

$$2 \times V_F \times I \qquad \text{(eq. 1)}$$

whereas the power loss in the MOSFET-based solution is given by:

$$I^2 \times R_{DS(ON)\ P-Channel} + I^2 \times R_{DS(ON)\ N-Channel} \qquad \text{(eq. 2)}$$

Completing a design based on the FDMQ8203 GreenBridge solution simply requires the addition of external circuitry to drive and protect the MOSFETs as shown in Figure 3. Red lines indicate the power flow path and green lines express the bias current of the gate circuit. Zener diodes are used to limit the gate-to-source voltage of the GreenBridge device, so as not to exceed BV_{GSS}.

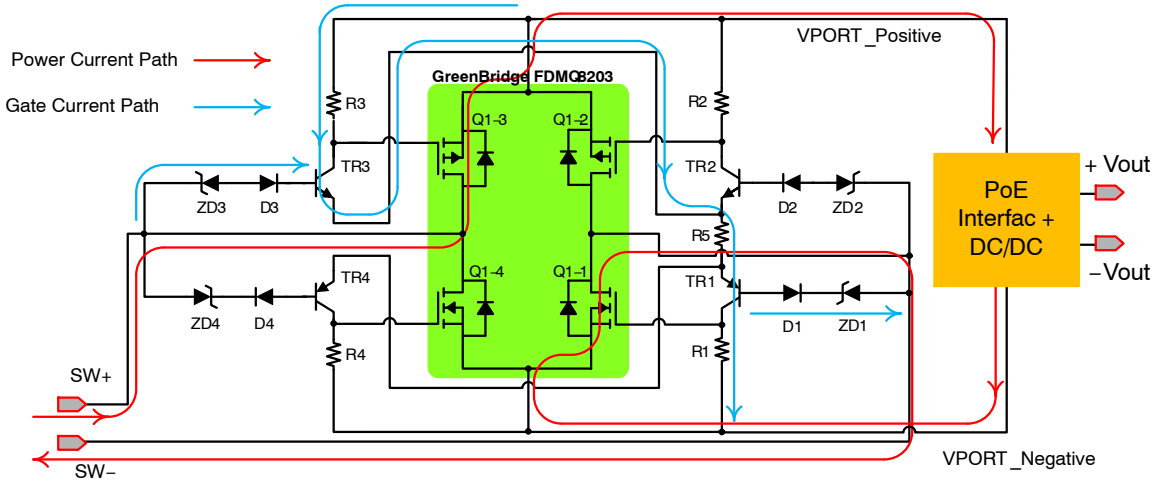


Figure 3. Solution Based on GreenBridge FDMQ8203 and External Drive/Protection Circuitry

When a PD is plugged into a PSE, the PSE recognizes the presence of the PD by checking the current through a 25 kΩ (±1.3 kΩ) resistor on the PD. This is the resistance detection process described in the PoE standard.

The PSE provides two consecutive voltages – V1 = 2.7 V and V2 = 10.1 V – to the PD for resistance detection and records the measured current values, I1 and I2. The $\Delta V / \Delta I$ calculated by the PSE establishes the presence of a PD. The PSE then moves on to identify the power class of the PD. This is sometimes known as the 'classification' phase and is shown in Figure 4.

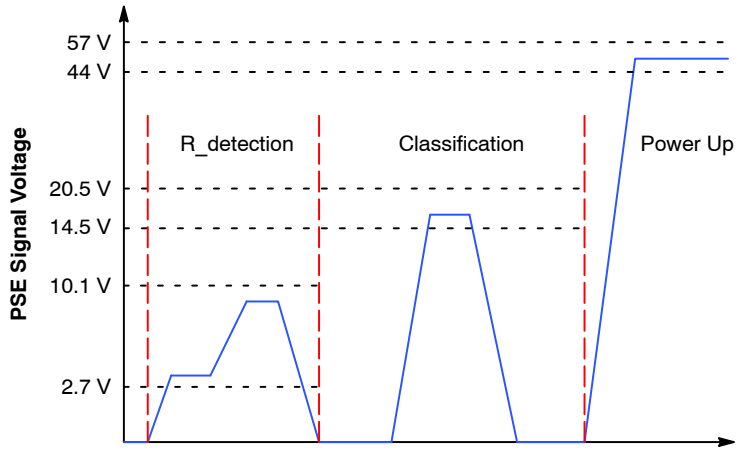


Figure 4. Waveforms during the Startup Phase

During this phase, the GreenBridge device must not compromise the resistance detection procedure by bypassing the current through the body diode. The recommended gate drive circuit helps the GreenBridge device stay turned off, with current bypassing via the body diode at 2.7 V and 10.1 V from the PSE.

Without the safe gate drive circuit, the GreenBridge device can turn on at the 10.1 V input given by the PSE during the resistance detection because the MOSFETs of the GreenBridge device have a 4 V maximum threshold voltage. This could cause the resistance detection process to fail.

In order to demonstrate the performance benefits over a conventional Schottky diode bridge, a 25 W PD block was designed to meet the specifications shown in Figure 5:

PoE Class	Class 4
IEEE Standard	IEEE802.3at
DCDC Topology	Flyback
Input Voltage	36 V ~ 57 V
Output Voltage	5 V
Maximum Output Current	5 A
Output Power	25 W
Switching Frequency	250 kHz

Figure 5. Specification for PD Used for Comparison Testing

At 25 W maximum output power and 36 V minimum input voltage, the estimated input current is 0.7 A through the bridge – this is the same for both the GreenBridge and diode solution.

Based on the equations above, the power loss for the diode solution (V_F = 0.7 V) is 0.98 W. The corresponding loss for the GreenBridge ($R_{DS(ON)\ P\text{-}Channel}$ = 190 mΩ, $R_{DS(ON)\ N\text{-}Channel}$ = 110 mΩ) solution is 0.147 W. This is a 0.83 W improvement in power loss and corresponds to a 2.41% improvement in efficiency of the bridge at maximum power and minimum input voltage.

Figure 6 shows a comparison of the power loss and efficiency of both solutions, illustrating that the GreenBridge solution offers performance improvements from minimum to maximum power.

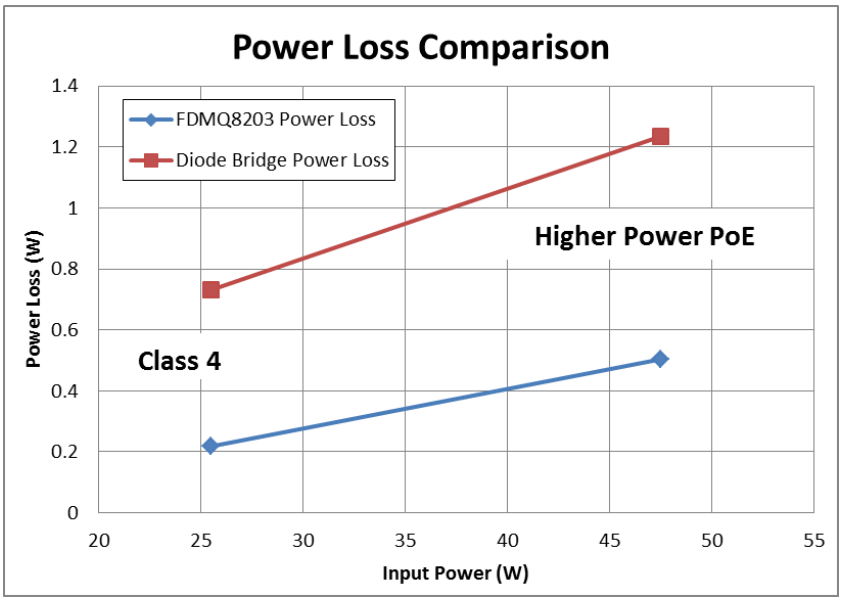


Figure 6. Power Loss and Efficiency Comparison of the GreenBridge and Diode Solutions

Even though the GreenBridge solution (including the gate circuits) is around half the size of the diode bridge, the lower thermal impedance of the MLP 4.5 × 5 mm package leads to a lower surface temperature. When tested with V_{IN} = 36 V and an ambient temperature of 25°C, the surface temperature of the GreenBridge package was 45°C – some 8.4°C lower than the diode bridge package.

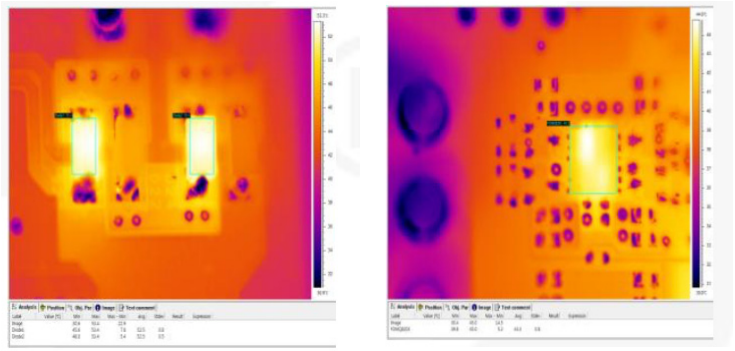


Figure 7. Thermal Analysis of the GreenBridge Package (Left) and Diode Package (Right)

To summarize the testing, the GreenBridge solution delivers reduced power loss, improved efficiency and reduced operating temperature in a solution that occupies around half the PCB area of the equivalent diode bridge.

GreenBridge Second Generation

Originally launched in 80 V versions, second-generation GreenBridge II high-efficiency bridge rectifiers are now available with ratings of 100 V. A block diagram of the GreenBridge 2 FDMQ8205A is shown in Figure 8. Here it can be seen that the device comprises two N-channel and two P-channel 100 V-rated MOSFETs as well as all necessary gate drivers. The result is a device that is supplied in the same small MLP 4.5 × 5 package as the first generation yet requires no external circuitry to drive or protect it.

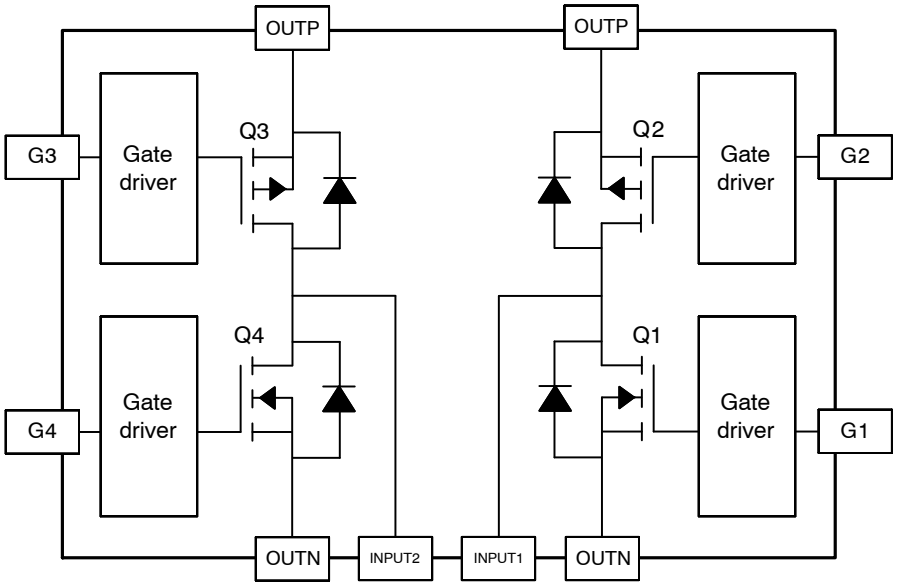


Figure 8. Block Diagram of GreenBridge 2 FDMQ8205A

With improved conduction loss and superior efficiency compared to a conventional Schottky bridge, all GreenBridge solutions provide up to 10 times better power dissipation.

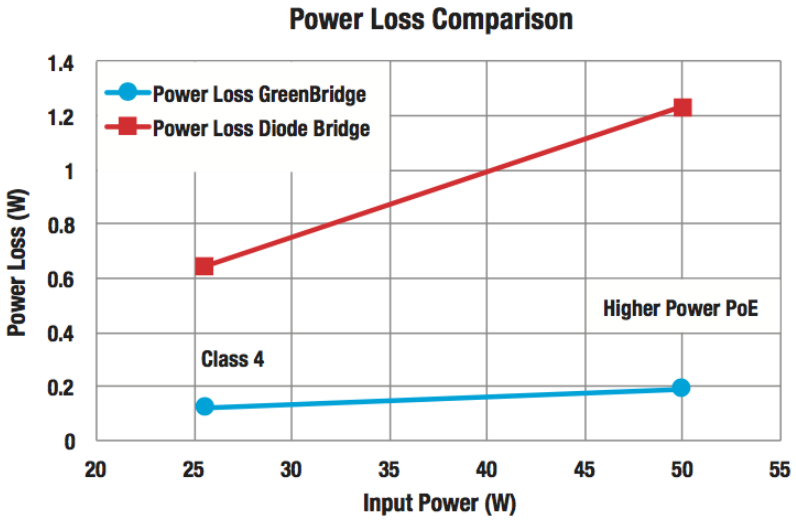


Figure 9. GreenBridge II Shows Improved Power Loss across All Power Levels

GreenBridge II supports a further improvement in PCB area, requiring just 45 mm^2, compared with 192 mm^2 for a diode solution (Figure 10).

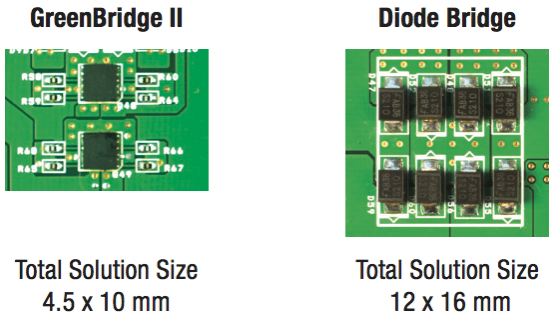


Figure 10. GreenBridge II Requires Less than 25% of the Space for a Conventional Diode Solution

At the same time, GreenBridge II achieves improved thermal performance over the first generation with thermal imaging testing shows that at 25.5 W, the top case temperature is now reduced to 29.9°C (a reduction of more than 15°C). This allows designers more margin in their designs and facilitates higher power densities.

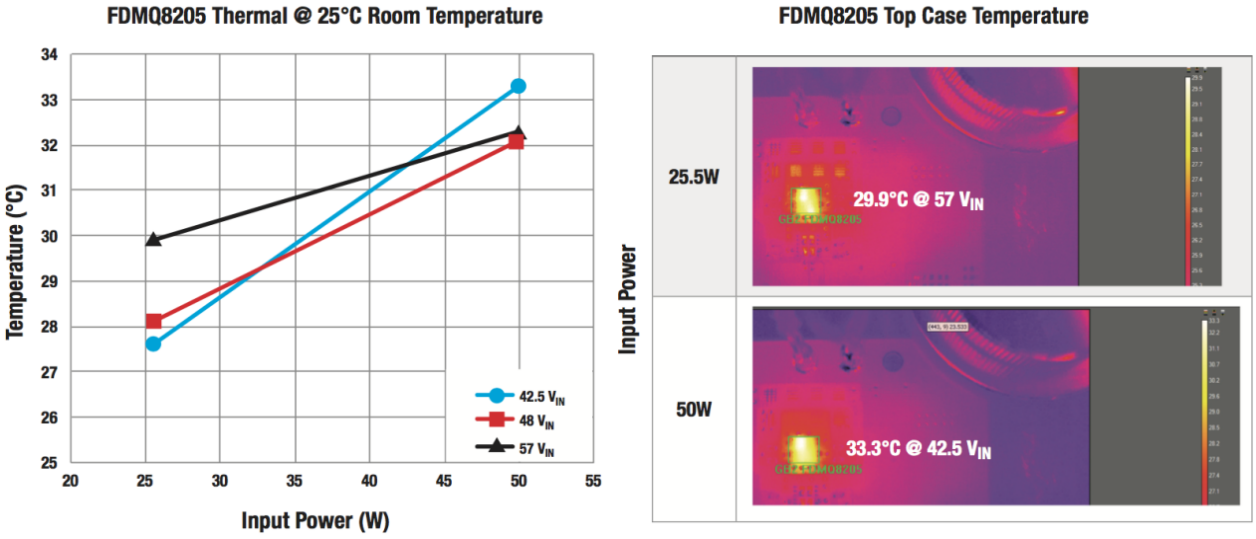


Figure 11. GreenBridge II Shows Improved Thermal Performance in Testing

How GreenBridge Addresses New IEEE802.3bt Standard

In IEEE802.3af/at of the PoE standard, there are four existing Classes, providing up to 25.5 W to PDs in 2-Pair powering of the network cable. The new coming PoE standard as IEEE802.3bt introduces 4-Pair powering to utilize both pairsets to deliver a power simultaneously, which expanded with four new Classes, taking the power level higher, up to 51 W for Type 3 PDs and up to 71.3 W for Type 4 PDs. 4-Pair powering can be constructed by single-signature or dual-signature 4-pair powering PoE. Single-signature 4-Pair has the same PD architecture as of 2-PAIR PD except 4-PAIR powering of PSE like Figure 12. A single-signature PD presents a valid detection signature on one of both pairsets to inform the connected device is PoE available. After passing detection, PD is classified by PSE. The intend of PD classification is to inform how much power a PD consumes during operation and also is used to establish mutual identification between PSE and PD. As the new standard defines the classification way to identify higher power classes called as type 3 and type 4, PSE uses multiple-event classification for Type 3 and Type 4 PDs, while PSE under IEEE802.3af/at standard implements single-event or two-event classification for Type 1 and Type 2 respectively.

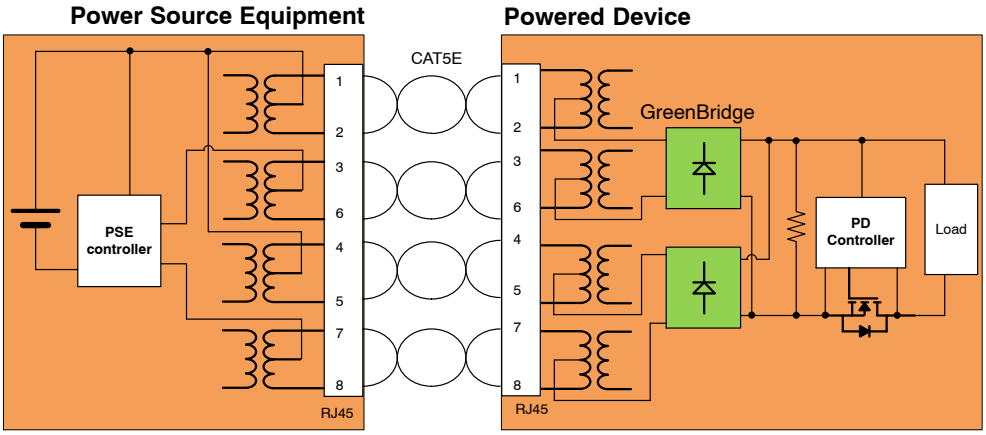


Figure 12. Single-signature 4-Pair Power PoE

The maximum average PD power on both pairsets (P_{Class_PD}) for Single-signature PD in accordance with the classification is tabulated in Table 2.

Table 2. MAXIMUM AVERAGE POWER FOR SINGLE-SIGNATURE PD

PD Type	Class	P_{Class_PD} (W)	Note
1	1	3.84	2-PAIR (IEEE802.3af)
	2	6.49	
	3	13.0	
2	4	25.5	2-PAIR (IEEE802.3at)
3	5	40.0	4-PAIR (IEEE802.3bt)
	6	51.0	
4	7	62.0	
	8	71.3	

In dual-signature powering system, each of both pairsets has the detection signature and classification separately between a PSE and a PD. It is designated as Type 3 and Type 4 depended on the assigned PD power. Dual-signature PDs advertise different class signature on each pairset. During the mutual identification onto each pairset, PSE identifies Class 5 by implementing multiple class events. Figure 13 illustrates Dual-signature 4-Pair PoE diagram.

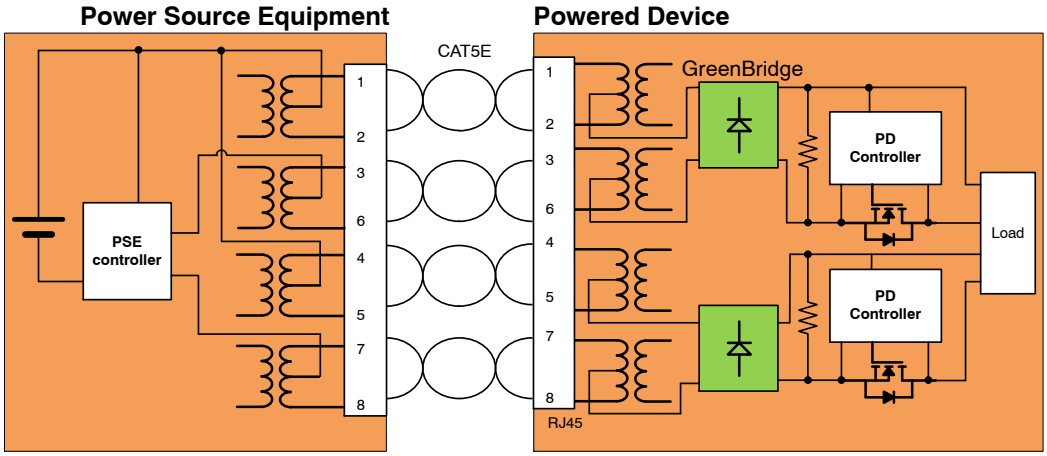


Figure 13. Dual-signature 4-Pair Power PoE

The maximum average PD power on each pairset (P_{Class_PD-2P}) for dual-signature PD in accordance with the classification is defined by Table 3.

Table 3. MAXIMUM AVERAGE POWER FOR DUAL-SIGNATURE PD

PD Type	Class	P_{Class_PD-2P} (W)
3	1	3.84
	2	6.49
	3	13.0
	4	25.5
4	5	35.6

4-Pair powering PoE needs the pair-to-pair current unbalance regulation. The new standard defines maximum PD common mode input resistance ($R_{Pair\_PD\_max}$) in order that the current in one of both pairsets don't exceed the continuous 2-Pair unbalance current ($I_{Con-2P-unb}$) like Table 4.

Table 4. PAIR-TO-PAIR CURRENT UNBALANCE REQUIREMENT

PD Type	Class	$I_{Con-2P-unb}$ (A)	$R_{Pair\_PD\_max}$ (Ω)
3	5	0.55	2.182 x $R_{PAIR\_PD\_min}$ + 0.125 Ω
	6	0.692	1.988 x $R_{Pair\_PD\_min}$ + 0.105 Ω
4	7	0.794	1.784 x $R_{Pair\_PD\_min}$ + 0.08 Ω
	8	0.948	1.727 x $R_{Pair\_PD\_min}$ + 0.074 Ω

Smaller constants α and β in the equation $R_{Pair\_PD\_max} = \alpha \times R_{Pair\_PD\_min} + \beta$ ensures to meet $I_{Con-2P-unb}$ requirement. The extremely low $R_{DS(ON)}$ of GreenBridge II FDMQ8205A by incorporating the shielded gate power trench MOSFET technology is far less than the maximum PD common mode input resistance. On the other hand, the conventional diode bridge has the relative cumbersome voltage drop around 0.5 V, which results in 540 mΩ of the effective input resistance when 90 W power at 48 V PSE voltage is delivered from PSE.

Table 5. $R_{DS(ON)}$ OF P&N-CH MOSFETS IN FDMQ8205A

Parameter	Conditions	Typ.	Max.	Unit
N-ch MOSFET (Q1, Q4)	V_G = 48 V, I_{INPUT} = 1.5 A, T_A = 25°C	29	44	mΩ
P-ch MOSFET (Q2, Q3)	V_G = 48 V, I_{INPUT} = 1.5 A, T_A = 25°C	83	125	mΩ

The positive temperature coefficient of $R_{DS(ON)}$ of the internal MOSFETs in GreenBridge becomes the advantage to improve the pair-to-pair current imbalance by enforcing proper current sharing through junction temperature differentials. For instance, if there is a current unbalance in 4-Pair powering, it makes one of both GreenBridges hotter and increase $R_{DS(ON)}$ more due to the positive temperature coefficient. It results that the other cooler GreenBridge with less current will conduct more current and the current unbalance is reduced. On the other hand, the conventional diode bridge has the negative temperature coefficient forward voltage (V_F). If one of diode bridges becomes hotter due to pair-to-pair current unbalance, the forward voltage of the hotter diode bridge decreases further less than the other cooler diode bridge. It forces the hotter diode bridge to conduct even more current. Eventually, there is the possibility to be a thermal runaway so the diode bridge needs more attention to manage the tolerance of the forward voltage in 4-Pair powering.

GreenBridge achieves much more power saving and improved thermal performance than conventional diode bridge at higher power condition.

The power loss in GreenBridge is calculated by:
= [MOSFET Conduction loss] + [Gate driving loss]
= $[I_{IN}^2 \times R_{DS(ON)\_Pch} + I_{IN}^2 \times R_{DS(ON)\_Nch}] + [V_{IN} \times I_G]$,

where I_{IN} is the input current and I_G is the consumed current by the gate driver which is around 2 mA at 48 V of the typical input voltage. The simulated power loss of FDMQ8205A at 4-Pair powering is compared with the conventional diode bridge like Figure 14. It shows FDMQ8205A delivers over 80% improvement in power saving compared to the diode bridge at all PD power class.

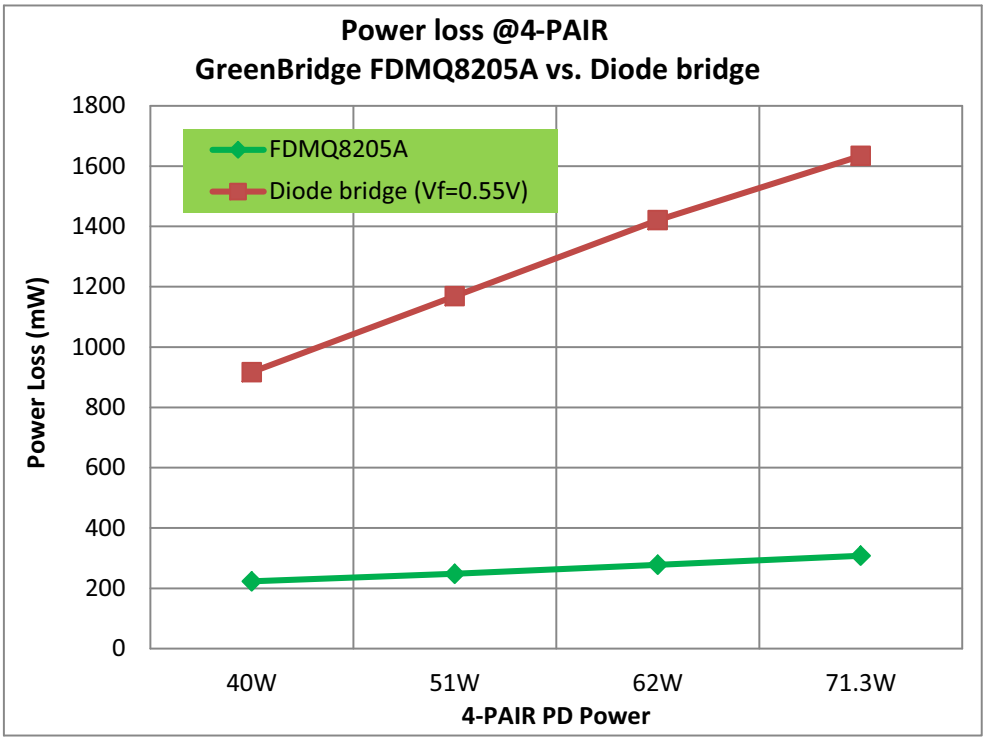


Figure 14. Power Loss Comparison @ 4-PAIR

The thermal performance of the FDMQ8205A is shown as Figure 15. When both FDMQ8205A rectify 90 W of the input power in the 4-pair powering, the top case temperature is maintained to less than 60°C at 25°C ambient temperature, while 100 V Schottky diode bridges heat up 110°C. FDMQ8205A is an excellent solution for customers having challenges in developing high power PoE PD applications that suffer from the thermal challenges on the limited PCB area.

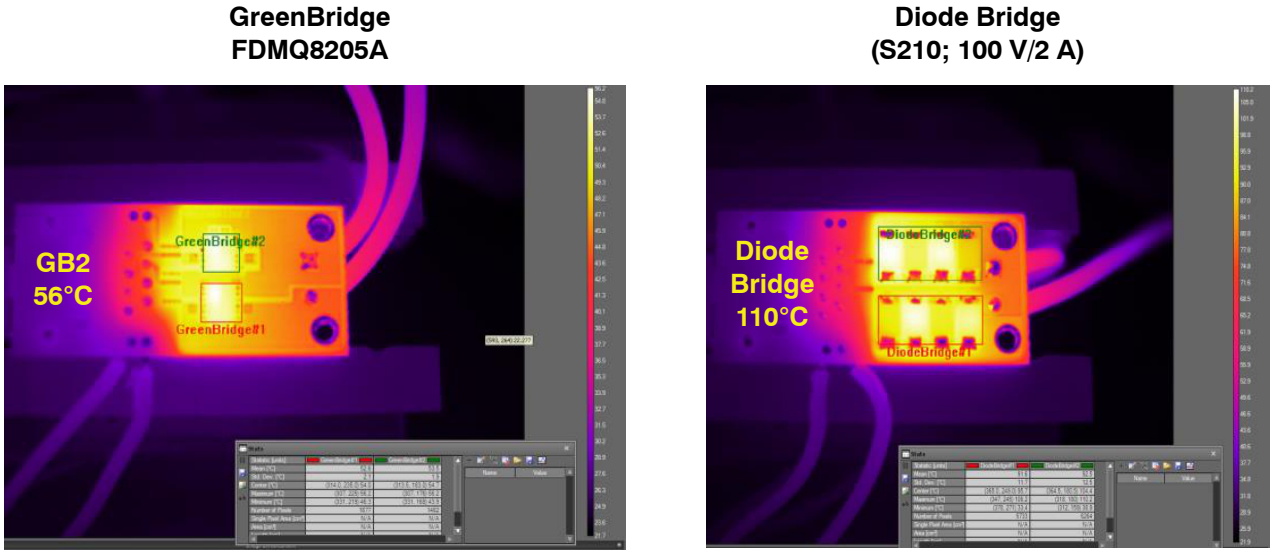


Figure 15. FDMQ8205 Thermal Performance @ 90 W (25°C Room Ambient Temperature)

Summary

PoE allows networks to be safely implemented at low cost as it removes the requirement to distribute mains-level voltages to devices on the network. It also brings additional functionality, such as the ability to protect the entire network with a single uninterruptible power supply. However, as power levels within the devices on the network increase in line with their increased functionality, energy efficiency and size rise up the design agenda.

Table 6. ON SEMICONDUCTOR FDMQ8203 AND FDMQ8205 APPLICATIONS

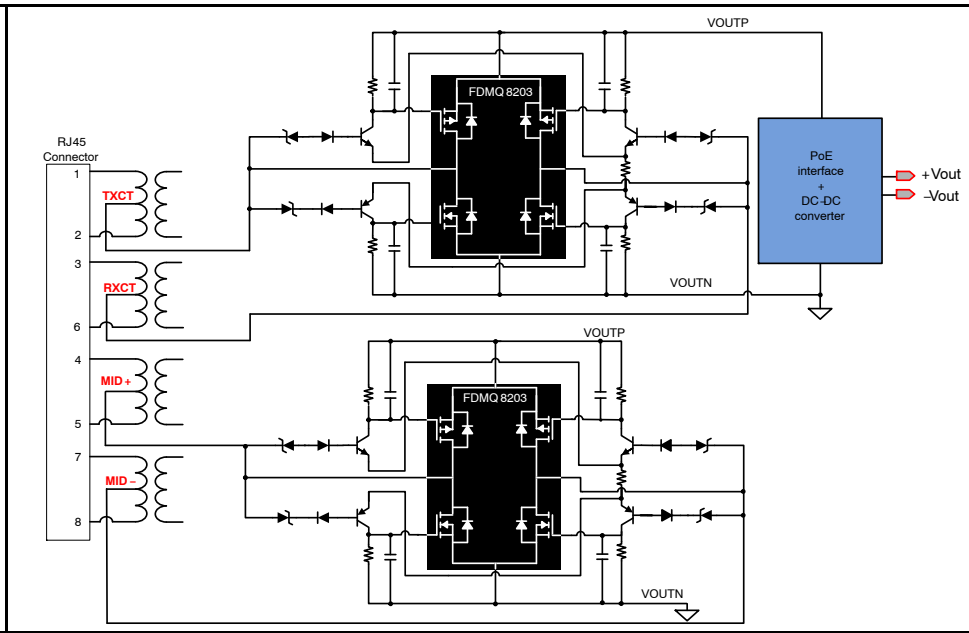
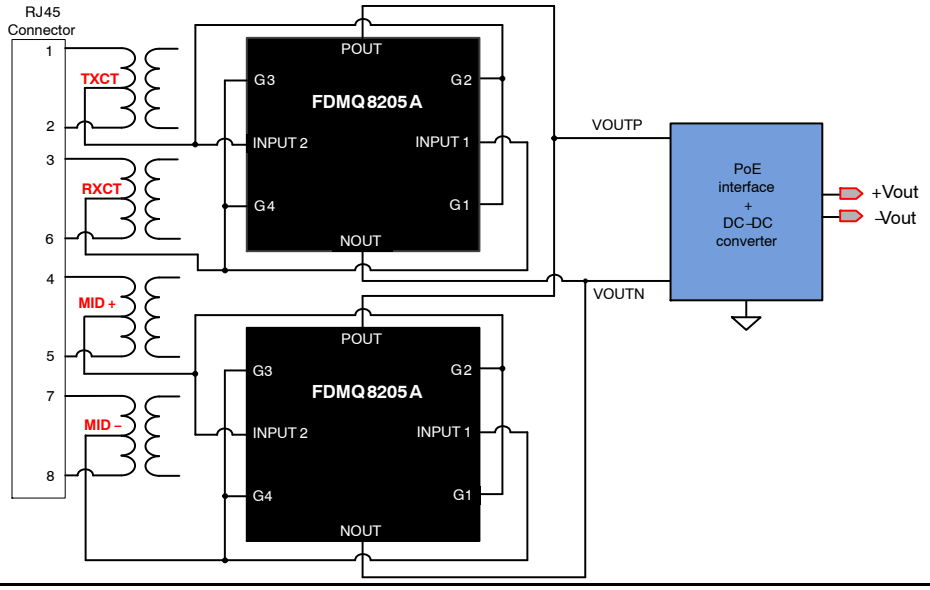
GreenBridge FDMQ8203	
GreenBridge II FDMQ8205/A	

Table 6 shows how the ON Semiconductor first and second generation GreenBridge technologies described above can be deployed in such applications. These high-power density MOSFET-based semiconductors help engineers to address functionality, power and size issues by significantly increasing system efficiencies and driving down operating temperatures when compared to conventional diode-based alternatives.

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