



ON Semiconductor®

Selecting Camera Switches for Next-generation Imaging Applications



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Providing high-quality camera and display functionality for single and multiple cameras is important in applications ranging from surveillance systems and gaming devices, to mobile phones and tablets. As users demand higher levels of performance and reliability from increasingly integrated designs, delivering camera-enabled systems presents a growing number of challenges for today's designers.

Some of the most daunting technical challenges are determining the most effective methods for routing high volumes of data, protecting and isolating high-frequency signals to ensure data integrity, and maximizing power efficiency. One way to address these challenges is to use analog 'camera' switches. By choosing the proper switch designers can simplify the handling of multiple camera interfaces, ensure high-integrity data communications, reduce the impact of EMI, protect against ESD, minimize power consumption, and even improve the options for board layout.

Interface Handling

Portable, camera-enabled applications typically integrate an application processor and video/imaging coprocessors with technologies such as baseband processors for handling wireless communications and one or more displays. The primary approach to connecting peripherals such as displays and cameras with application processors or coprocessors is the increasingly prevalent serial-oriented interface based on standards developed by the MIPI® (Mobile Industry Processor Interface) Alliance. MIPI has been widely adopted as the camera standard across mobile, automotive, and multimedia applications for both Display Serial Interfaces (DSI) and Camera Serial Interfaces (CSI-2). The MIPI protocol is thoroughly proven through testing, low power, and low cost.

With the advancements of smartphone camera technology, vehicles with assisted driving, and IoT networking, many systems are faced with the challenge of seamlessly integrating multiple cameras.

Integrating multiple cameras and displays can potentially cause problems when it comes to signal integrity. With a parallel interface, the simplest approach is to connect the two peripherals to the same set of signals. In the case of a camera, the data flows to the processor, and in the

case of a display the data flows from the processor. Such one-way flow can allow the bussed-signal connection to function even without a bus-contention management scheme.

However, two peripherals connected on the same set of conductors can cause problems for both the camera and display. There is inherently a difference in distance between the processor and each of the peripherals resulting in significant potential for signal reflections. One way to improve the parallel interconnect design case is via the use of an analog switch. A typical design will likely switch and isolate the signals that travel the furthest distance.

Newer designs based on MIPI interfaces have a similar problem. While MIPI interconnects do afford a better opportunity to support multiple cameras and displays, they were originally conceived as point-to-point links. As most processors and coprocessors include only a single MIPI port for each peripheral type, multiplexing is essential. For this, the proper choice of switch is critical.

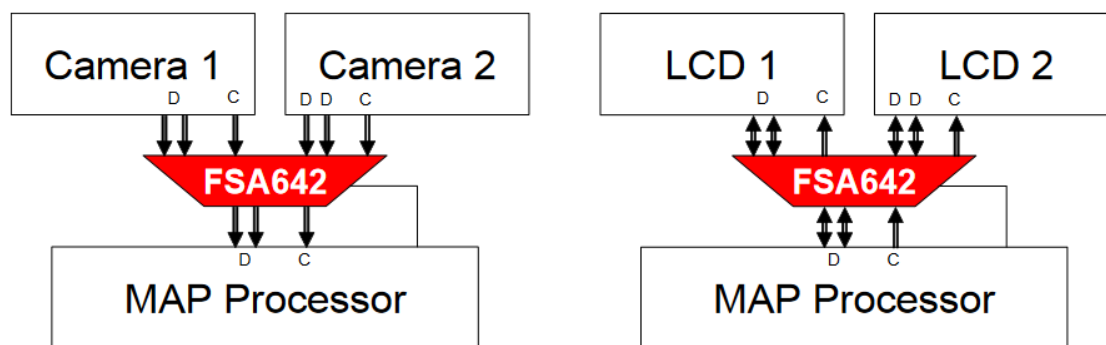


Figure 1. Dual Camera and Display Applications with SPDT Multiplexing Switch

In Figure 1, for example, the two MIPI camera modules or two MIPI display modules offer four data interface lanes and two clock signal lanes. In this case, a three-lane, 2:1, single-pole double-throw (SPDT) device such as the ON Semiconductor FSA642 three-port, high-speed differential switch can fully multiplex access to a peripheral ensuring that only one link is active at any time. The switch accommodates the D-PHY standard, has a typical (-3 dB) bandwidth of 1.0 GHz and minimizes power consumption with quiescent current consumption of less than 1 μ A.

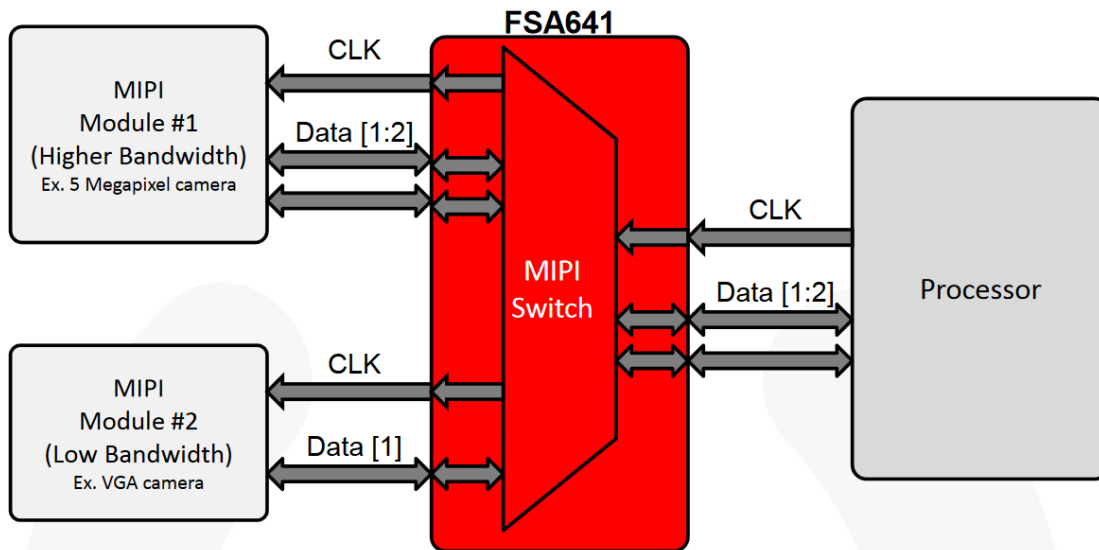


Figure 2. Dual 4-data Lane Camera/Display

More complex designs may need to accommodate multiple data lanes and/or multiple high-resolution and low-resolution cameras as shown in Figure 2. Here we see connectivity for dual high/low resolution cameras with the FSA641 single-pole double throw (SPDT) 2:1 MIPI switch – which has the same power and bandwidth specifications as the FSA642 – providing the requisite multiplexing.

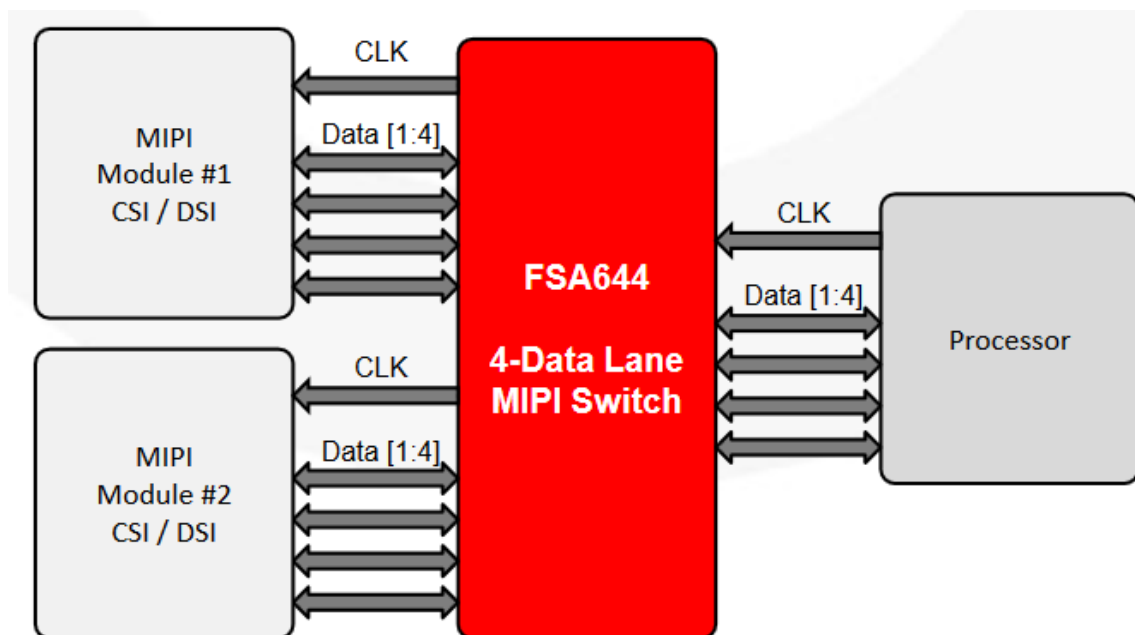


Figure 3. Dual 4-data Lane Camera/Display

Figure 3 illustrates a four-data lane camera/display architecture with multiplexing provided by the ON Semiconductor FSA644. This switch supports up to 1.6 GHz signals and up to 6 Gbps data rates using MIPI DPHY. Optimized routing helps to minimize channel to channel cross talk while consuming less than 6 mm² of PCB area.

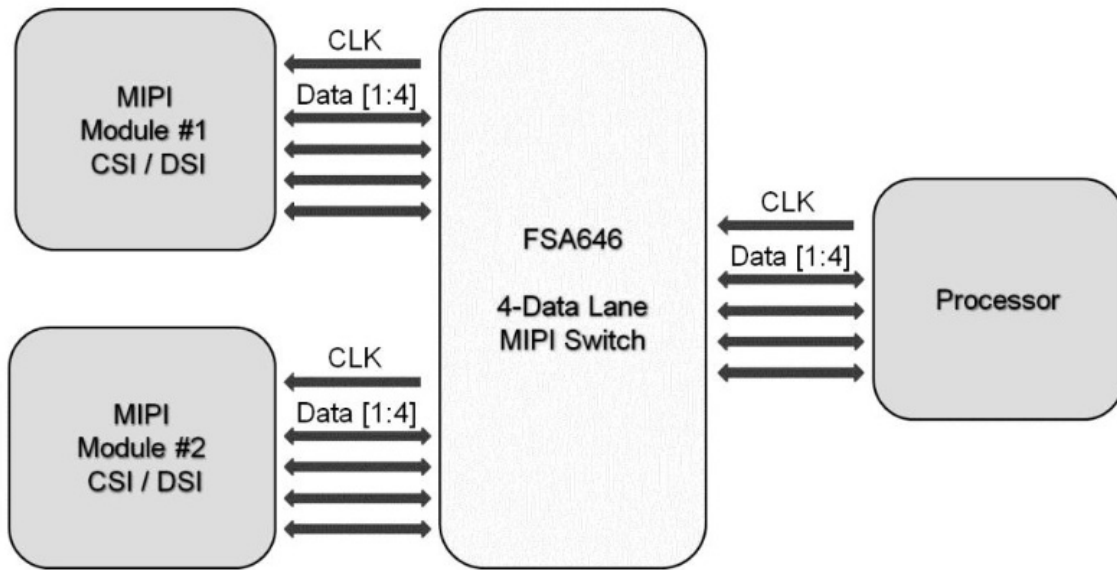


Figure 4. Dual 4–data Lane 2.5 Gbps Camera/Display

With the release of MIPI D–PHY V1.2 came an increase in the data rate spec from 1.5 Gbps to 2.5 Gbps. ON Semiconductor quickly responded to this change by developing the FSA646. Like the FSA644, the FSA646 is a four–data lane, high–speed differential switch. The switch accommodates both the C–PHY and D–PHY standards with a D–PHY data rate of 2.5 Gbps per lane and a (–3 dB) bandwidth of 4 GHz. Current consumption of less than 1 μ A in disabled mode minimizing power consumption.

Table 1 and Figure 5 summarize the MIPI switch architecture options offered by the highlighted devices.

Table 1. FSA64X SWITCH OPTIONS

Product	Configuration	Lanes	BW (Typ)	Data Rate (Max)	Package
FSA641	2:1 D–Phy 1.1	(1) 2 Lane (1) 1 Lane	1 GHz	3 Gbps	UMLP 20
FSA642	2:1 D–Phy 1.1	2 Lane	1 GHz	3 Gbps	UMLP 24
FSA644	2:1 D–Phy 1.1	4 Lane	1.6 GHz	6 Gbps	WLCSP 36
FSA646	2:1 D–Phy 1.2 2:1 C–Phy 1.0	4 Lane 3 Lane	4 GHz	10 Gbps 17.1 Gbps	WLCSP 36
FSA660	2:1 C–Phy 1.0	1 Lane	> 5 GHz	5.7 Gbps	TMPL 18

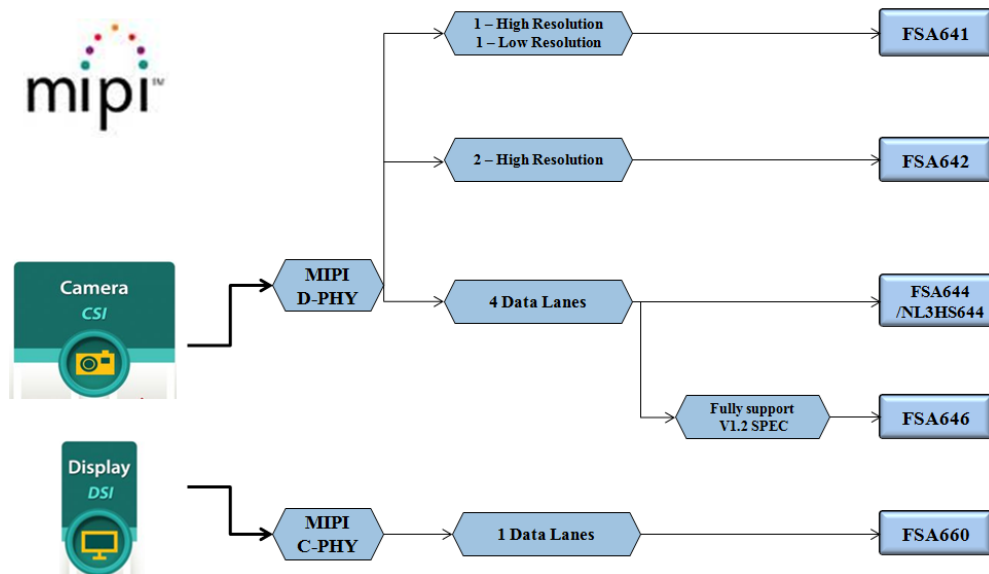


Figure 5. MIPI Switch Options

Data Integrity – The Need for Isolation

Higher frequencies of modern portable devices such as cell phones means there is a need to manage parasitics for optimal signal integrity. As cameras within these phones move to higher resolutions and higher data rates, parasitic components can easily deteriorate signals and generate unwanted EMI. That’s where high-speed isolation switches come in.

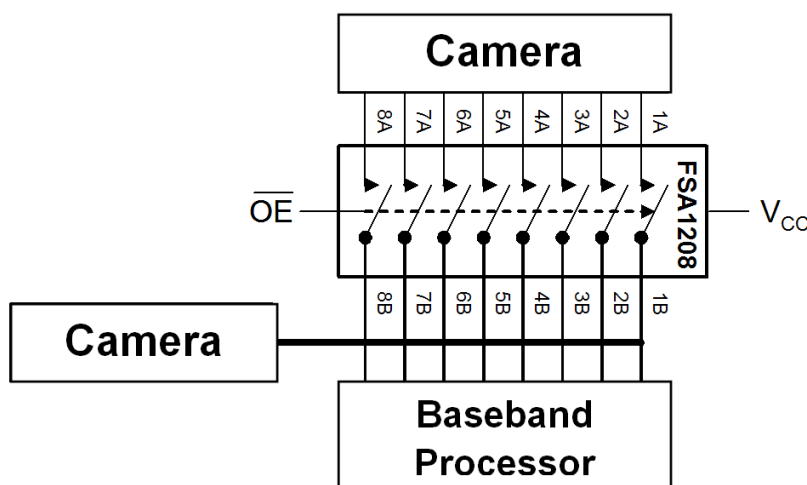



Figure 6. Isolating the High-speed Bus in Dual Camera Applications Using Analog Switches

Take, for example, the FSA1208 low-power, 8-port, high-speed switch illustrated in Figure 6. This part is configured as a single-pole, single-throw switch (SPST) and is designed to isolate the high-speed bus from parasitic components in dual camera applications. With a bandwidth in excess of 400 MHz and high ESD rating of 7.5 kV, the FSA1208 offers an optimal way to isolate capacitance and maintain signal integrity for high-speed data paths.

When isolating the unused parallel interface, the FSA1208 reduces the radiated EMI of the path, improving RF desense. The traditional parallel solution can deteriorate the signal due to the unwanted “stub”, resulting in image degradation of the camera module. Another approach is to use multiple analog switches, which complicates design and adds to the overall bill of material (BOM) costs. In contrast, the FSA1208 offers robust isolation and ease of design at a lower cost.

The FSA1208 features an extremely low on capacitance (C_{ON}) of 6 pF. The wide bandwidth (> 400 MHz) contributes to signals with minimum edge and phase distortion. Superior channel-to-channel crosstalk minimizes interference. Furthermore, special circuitry on pins A and B allows the switch to withstand an over-voltage condition. The device is also designed to minimize current consumption even when the control voltage applied to the \overline{OE} pin is lower than the supply voltage (V_{CC}). This feature is especially valuable for mobile applications, such as cell phones, allowing direct interface with the general-purpose I/Os of the baseband processor.

Other applications include port isolation and switching in portable cell phones, PDAs, digital cameras, printers, and notebook computers.

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