NCV887300

Small-Signal PSPICE Model

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The PSPICE model is a small-signal implementation of the NCV887300 non-synchronous SEPIC/Boost IC [1] intended for feedback loop stability analysis in a Boost, SEPIC or Flyback topology.

The example PSPICE file demonstrates the model implementation used for the NCV8873LEDBSTGEVB [2] boost evaluation demo board (Fig. 1) and will be described in this article. An example simulation for a discrete inductor SEPIC LED converter is also included (not discussed in this article).
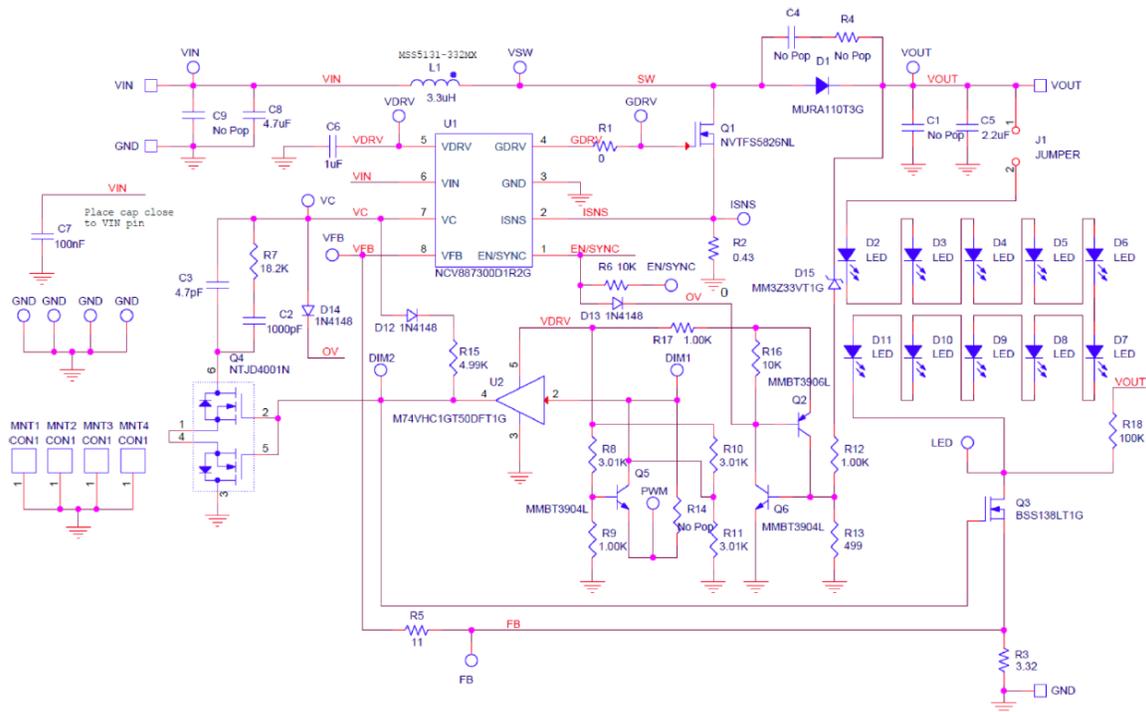

Figure 1 NCV887300LEDBSTGEVB Evaluation Board Schematic

Modeled Elements

The PWMCM_L_NCV887300.LIB switch model is a product specific version on the public domain current-mode PWMCM_L lossy model published by Christophe Basso [3].

A stability analysis of the LED boost converter design may be performed by passing the following parameters to the PWMCM_L_NCV887300 library file:

- SW: operating losses from the series combination of MOSFET rDS(ON) and current sense resistor (Ω)

- DIO –

  o Boost topology: Connect the rectifier diode model to include diode loss contribution. Anode to GND and cathode to DIO.
  o SEPIC topology: Connect the rectifier diode model to include diode loss contribution. Anode to DIO and cathode to GND (example provided in PSPICE file).

- L –
    - Boost topology: Equivalent boost inductor (operating value of L1), (H).
    - SEPIC topology: Equivalent boost inductor (parallel operating value for L1//L2 for the discrete inductor SEPIC topology, operating value of L1 for the coupled-inductor SEPIC), (H).
- Rsense – Current sense resistor (Ω)
    - Boost topology: Parameter value must be negative, (see [3]).
    - SEPIC topology: Parameter value must be positive.
- Rdson – MOSFET ON-resistance (Ω)

Modeling Example

A PSPICE small-signal analysis implementation of the NCV887300SEPGEVB demo board is shown in Fig. 2. Simulation results are shown in Fig. 3. Node definitions are provided in Table 1. The NCV8873 feedback amplifier is an operational transconductance amplifier (OTA). A 542 Ω resistor between the OTA output and the IC-VC compensation pin is implemented in silicon for ESD protection. To permit an accurate OTA gain analysis when selecting compensation feedback components, the internal OTA output node ("CTRL") is made available and is strictly intended for analysis.
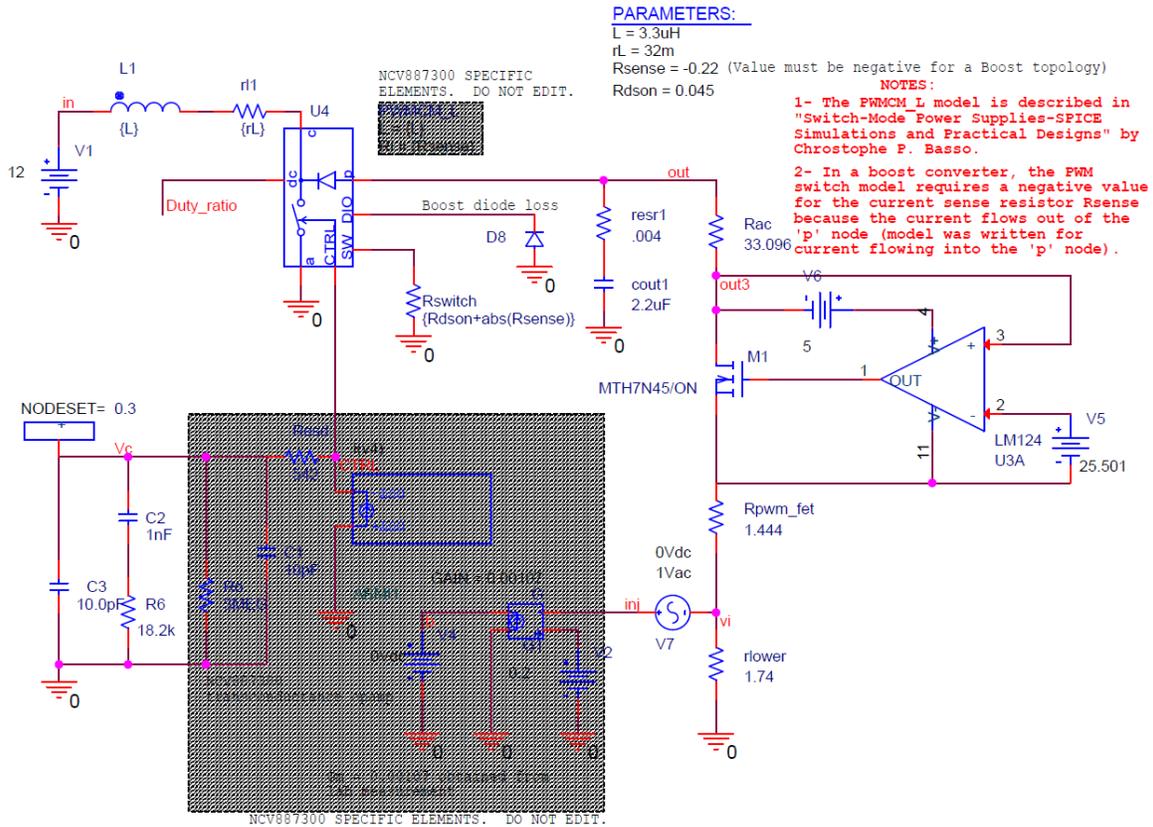
Figure 2 NCV887300LEDBSTGEVB Evaluation Board Small-Signal Simulation

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NCV887300 PSpice Model
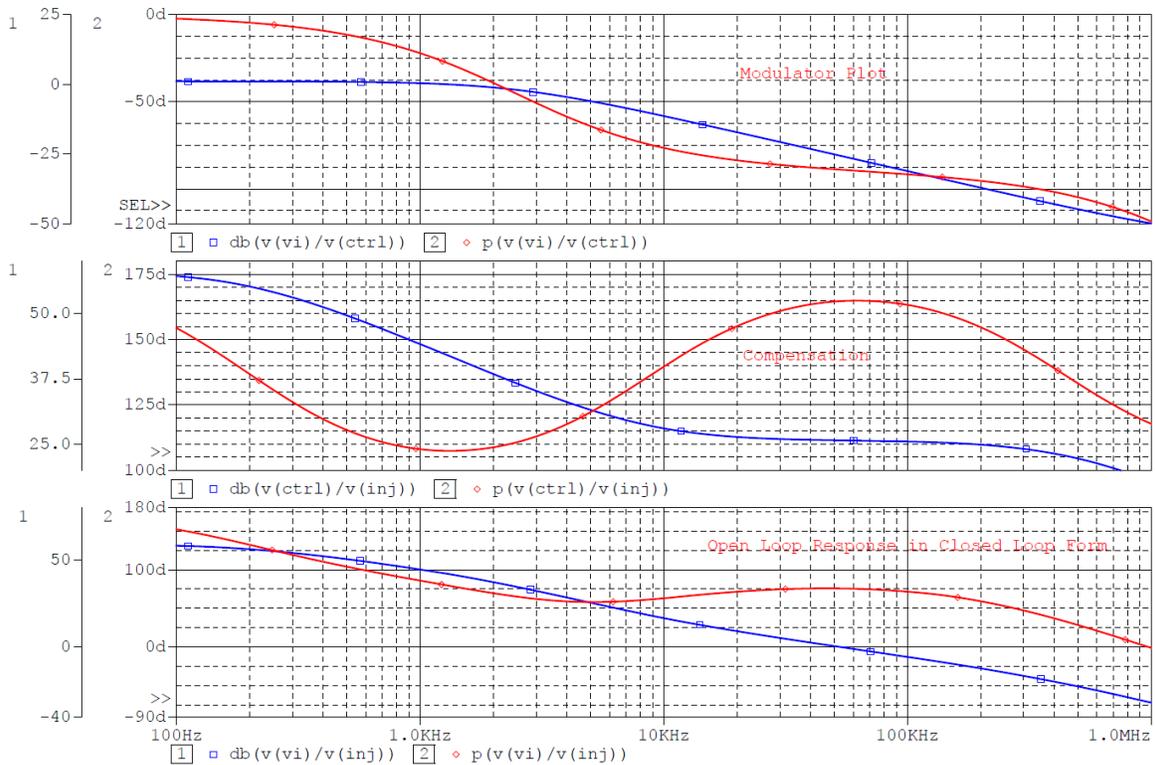
Figure 32 NCV887300LEDBSTGEVB Evaluation Board Small-Signal Simulation Feedback Loop Response

An ESD protection resistor is present between the OTA output and the VC package pin on the die (this is not documented in the datasheet). A virtual output (CTRL) is provided to access the controller's internal feedback node to permit a more accurate analysis for instances where the compensation resistor approaches the value of Resd (set to 542 Ω within the model).

Table 1 NCV887300 Model – Node Definitions

Parameter	Monitoring Purposes Only?	Unit	Range	Comment
A	No	V		Active Node [3]
C	No	V		Common Node [3]
P	No	V		Passive Node [3]
CTRL	Yes	V	N/A	INTERNAL NODE FOR SIMULATION ANALYSIS
Duty_Ratio	Yes	V	0-D_{max} (see datasheet)	INTERNAL NODE FOR SIMULATION ANALYSIS
VC	No	V	N/A	IC Compensation Pin
INJ	No	V	V_{ref} = 0.2 V	Voltage feedback node
DIO	No	-	Rectifier Loss	Connection point of rectifier diode, only used for a more accurate duty ratio calculation in the simulation.
SW	No	-	rDS(on) and current sense losses	Connection point to include the influence of rDS(on) and current sense resistor losses, only used for a more accurate duty ratio calculation in the simulation.

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Table 2 NCV887300 Model – Parameters Table Definition

Parameter	Unit	Comment
Rsense	Ω	Current Sense Resistor
L1 (L1/L2)	H	Boost Inductor (SEPIC Inductors)

Feedback Loop Analysis Methodology

Simulations should be run at worst case parameter conditions (e.g.: Minimum input voltage, worst case output capacitor parasitic ESR values, etc). Additional simulations under less stringent conditions (e.g. nominal ESR, different input voltage conditions) are recommended as well for verification. The disturbance injection point is introduced by inserting and AC source between nodes ***inj*** and ***vi***.

1- Control-Output (Modulator Plot) Response

This is the response of the power supply as seen by the IC's internal CTRL node (V(VI)/V(CTRL)). This information is required to select OTA compensation components (R6, C2, C3).

2- OTA Compensation

From the modulator plot data, the OTA compensation network is determined (V(CTRL)/V(INJ)) by selecting the desired zero gain and frequency values (R6/C2) and pole frequency (C3). CTRL is the OTA output (before Resd) and is a node internal to the IC and is strictly intended for analysis.

3- Loop Response (Open-Loop Response in Closed-Loop Form)

The power supply feedback loop response is obtained by plotting V(VI)/V(INJ). The resulting design cross-over frequency, phase-margin and gain-margin are now obtained.

References

[1] NCV8873: Non-Synchronous Boost Controller datasheet:
http://onsemi.com/PowerSolutions/product.do?id=NCV8873

[2] NCV8873: Automotive Grade High-Frequency SEPIC Controller Evaluation Board User's Manual:
http://onsemi.com/PowerSolutions/supportDoc.do?type=boards&rpn=NCV8873

[3] C. Basso, "Switch-Mode Power Supplies – SPICE Simulations and Practical Designs", Second Edition, McGraw Hill, 2014.