NCV7349-ADD/D

CAN Transceiver NCV7349 Specification Addendum

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TECHNICAL REPORT

Introduction and Document Scope

This document deals with impact of extended supply range of 4.5 V to 5.5 V (VCC pin) to parametric operation of NCV7349 and also impact to specific Velio system test.

Datasheet Parameters in Extended Range

NCV7349 in datasheet clearly specify power supply conditions for parametric operation in the range from VCC = 4.75 V to 5.25 V. Table 1 in NCV7349 datasheet [1] notes that the functional range of the chip is extended to 4.5 V to 5.5 V.

Absolute Maximum Ratings

The chip absolute maximum ratings as defined in NCV7349 datasheet [1] in Table 4 are not affected by extended supply range conditions from VCC of 4.5 V to 5.5 V.

Thermal Characteristics

The chip thermal characteristics as defined in NCV7349 datasheet [1] in Table 5 are not affected by extended supply range conditions from VCC of 4.5 V to 5.5 V.

ELECTRICAL CHARACTERISTICS V_{CC} = 4.75 V to 5.25 V; V_{IO} = 2.8 V to 5.5 V (NCV7349−3 only); T_J = −40 to +150°C; R_{LT} = 60 Ω unless specified otherwise. On chip versions without V_{IO} pin, reference voltage for all digital inputs and outputs is V_{CC} instead of V_{IO}.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Impact of extended supply range of 4.5 V to 5.5 V on V_{CC} pin
SUPPLY (Pin V_{CC})							
I_{CC}	Supply current	Dominant; V_{TxD} = 0 V Recessive; V_{TxD} = V_{IO}	−	48 6	79 10.5	mA mA	Max value 5% impacted
I_{CCS}	Supply current in standby mode	$T_J \le 100°C$, (Note 1)	−	10	15.75	μA	Max value 5% impacted
V_{UVDVCC}	Undervoltage detection voltage on V_{CC} pin		2	3	4	V	NO IMPACT
SUPPLY (pin V_{IO}) on NCV7349−3 Version Only							
V_{IO}	Supply voltage on pin V_{IO}		2.8	−	5.5	V	NO IMPACT
I_{IOS}	Supply current on pin V_{IO} in standby mode	Standby mode	−	1	−	μA	NO IMPACT
I_{IONM}	Supply current on pin V_{IO} in normal mode	Dominant; V_{TxD} = 0 V Recessive; V_{TxD} = V_{IO}	−	−	1 0.2	mA mA	NO IMPACT
V_{UVDVIO}	Undervoltage detection voltage on V_{IO} pin		1.3	−	2.7	V	NO IMPACT
TRANSMITTER DATA INPUT (Pin TxD)							
V_{IH}	High−level input voltage	Output recessive	2.0	−	V_{IO}	V	NO IMPACT

1. Values based on design and characterization, not tested in production
2. The performance is dominantly defined by the same IP like used in NCV7351 and NCV7342 where supply range is guaranteed and characterized from 4.5 V to 5.5 V

ELECTRICAL CHARACTERISTICS V_{CC} = 4.75 V to 5.25 V; V_{IO} = 2.8 V to 5.5 V (NCV7349−3 only); T_J = −40 to +150°C; R_{LT} = 60 Ω unless specified otherwise. On chip versions without V_{IO} pin, reference voltage for all digital inputs and outputs is V_{CC} instead of V_{IO}.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Impact of extended supply range of 4.5 V to 5.5 V on V_{CC} pin
TRANSMITTER DATA INPUT (Pin TxD)							
V_{IL}	Low−level input voltage	Output dominant	−0.3	−	+0.8	V	NO IMPACT
I_{IH}	High−level input current	$V_{TxD} = V_{IO}$	−5	0	+5	μA	NO IMPACT
I_{IL}	Low−level input current	V_{TxD} = 0 V	−75	−200	−350	μA	NO IMPACT
C_i	Input capacitance	(Note 1)	−	5	10	pF	NO IMPACT
TRANSMITTER MODE SELECT (Pin STB)							
V_{IH}	High−level input voltage	Standby mode	2.0	−	V_{IO}	V	NO IMPACT
V_{IL}	Low−level input voltage	Normal mode	−0.3	−	+0.8	V	NO IMPACT
I_{IH}	High−level input current	$V_{STB} = V_{IO}$	−5	0	+5	μA	NO IMPACT
I_{IL}	Low−level input current, NCV7349−0	V_{STB} = 0 V	−10	−4	−1	μA	NO IMPACT
I_{IL3}	Low−level input current, NCV7349−3	V_{STB} = 0 V	−40	20	−4	μA	NO IMPACT
C_i	Input capacitance	(Note 1)	−	5	10	pF	NO IMPACT
RECEIVER DATA OUTPUT (Pin RxD)							
I_{OH}	High−level output current	Normal mode $V_{RxD} = V_{IO}$ − 0.4 V	−0.1	−0.4	−1	mA	NO IMPACT
I_{OL}	Low−level output current	V_{RxD} = 0.4 V	1.6	6	12	mA	NO IMPACT
V_{OH}	High−level output voltageWeaker RxD pin in Standby mode is on NCV7349−0 version only	Standby mode I_{RxD} = −100 μA	V_{IO} − 1.1	V_{IO} − 0.7	V_{IO} − 0.4	V	NO IMPACT
BUS LINES (Pins CANH and CANL)							
$V_{o(reces)}$ (norm)	Recessive bus voltage on pins CANH and CANL	$V_{TxD} = V_{IO}$; no load; normal mode	2.0	2.5	3.0	V	NO IMPACT (Note 2)
$V_{o(reces)}$ (stby)	Recessive bus voltage on pins CANH and CANL	$V_{TxD} = V_{IO}$; no load; standby mode	−100	0	100	mV	NO IMPACT (Note 2)
$I_{o(reces)}$ (CANH)	Recessive output current at pin CANH	−35 V < V_{CANH} < +35 V; 0V < V_{CC} < 5.25 V	−2.5	−	+2.5	mA	NO IMPACT (Note 2)
$I_{o(reces)}$ (CANL)	Recessive output current at pin CANL	−35 V < V_{CANL} < +35 V; 0 V < V_{CC} < 5.25 V	−2.5	−	+2.5	mA	NO IMPACT (Note 2)
$I_{LI(CANH)}$	Input leakage current to pin CANH	0 Ω < R(V_{CC} to GND) < 1 MΩ $V_{CANL} = V_{CANH}$ = 5 V	−10	0	10	μA	NO IMPACT

1. Values based on design and characterization, not tested in production
2. The performance is dominantly defined by the same IP like used in NCV7351 and NCV7342 where supply range is guaranteed and characterized from 4.5 V to 5.5 V

ELECTRICAL CHARACTERISTICS V_{CC} = 4.75 V to 5.25 V; V_{IO} = 2.8 V to 5.5 V (NCV7349−3 only); T_J = −40 to +150°C; R_{LT} = 60 Ω unless specified otherwise. On chip versions without V_{IO} pin, reference voltage for all digital inputs and outputs is V_{CC} instead of V_{IO}.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Impact of extended supply range of 4.5 V to 5.5 V on V_{CC} pin
BUS LINES (Pins CANH and CANL)							
$I_{LI(CANL)}$	Input leakage current to pin CANL	0 Ω < R(V_{CC} to GND) < 1 MΩ V_{CANL} = V_{CANH} = 5 V	−10	0	10	μA	NO IMPACT
$V_{o(dom)}$ (CANH)	Dominant output voltage at pin CANH	V_{TxD} = 0 V	2.75	3.5	4.5	V	Valid for: 50Ω < R_{LT} < 65 Ω. Guaranteed by design. Covered by corner simulations. (Limits changed according to ISO11898−2 [2])
$V_{o(dom)}$ (CANL)	Dominant output voltage at pin CANL	V_{TxD} = 0 V	0.5	1.5	2.25	V	Valid for: 50Ω < R_{LT} < 65 Ω. Guaranteed by design. Covered by corner simulations. (Limits changed according to ISO11898−2 [2])
$V_{o(dif)}$ (bus_dom)	Differential bus output voltage (V_{CANH} − V_{CANL})	V_{TxD} = 0 V; dominant; 45 Ω < R_{LT} < 65 Ω	1.5	2.25	3.0	V	Valid for: 50Ω < R_{LT} < 65 Ω. Guaranteed by design. Covered by corner simulations. This is fully in line with ISO11898−2 [2] which defines 1.5V minimum level for R_{LT} larger than 50Ω
$V_{o(dif)}$ (bus_rec)	Differential bus output voltage (V_{CANH} − V_{CANL})	V_{TxD} = V_{IO}; recessive; no load	−120	0	+50	mV	NO IMPACT (Note 2)
$I_{o(sc)}$ (CANH)	Short circuit output current at pin CANH	V_{CANH} = 0 V; V_{TxD} = 0 V	−100	−70	−45	mA	Guaranteed by design. Covered by corner simulations.
$I_{o(sc)}$ (CANL)	Short circuit output current at pin CANL	V_{CANL} = 36 V; V_{TxD} = 0 V	45	70	105	mA	Guaranteed by design. Covered by corner simulations. Max value 5% impacted.
$V_{i(dif)R}$ (th)	Differential receiver threshold voltage – Dominant to Recessive	−2 V < V_{CANL} < +7 V; −2 V < V_{CANH} < +7 V;	0.5	0.6	0.7	V	NO IMPACT (Derived from internal reference)
$V_{i(dif)D}$ (th)	Differential receiver threshold voltage – Recessive to Dominant	−2 V < V_{CANL} < +7 V; −2 V < V_{CANH} < +7 V;	0.7	0.8	0.9	V	NO IMPACT (Derived from internal reference)
$V_{ihcmR(dif)}$ (th)	Differential receiver threshold voltage – Dominant to Recessive	−35 V < V_{CANL} < +35 V; −35 V < V_{CANH} < +35 V;	0.4	−	0.8	V	NO IMPACT (Derived from internal reference)
$V_{ihcmD(dif)}$ (th)	Differential receiver threshold voltage – Recessive to Dominant	−35 V < V_{CANL} < +35 V; −35 V < V_{CANH} < +35 V;	0.6	−	1	V	NO IMPACT (Derived from internal reference)
$V_{ihcmD12(dif)}$ (th)	Differential receiver threshold voltage – Both transitions	−12 V < V_{CANL} < +12 V; −12 V < V_{CANH} < +12 V;	0.5	−	0.9	V	NO IMPACT (Derived from internal reference)
$V_{i(dif)}$ (hys)	Differential receiver input voltage hysteresis	−2 V < V_{CANL} < +7 V; −2 V < V_{CANH} < +7 V;	100	200	300	mV	NO IMPACT (Derived from internal reference)
$V_{i(dif)}$ (th)_STDBY	Differential receiver threshold voltage in standby mode	−12 V < V_{CANL} < +12 V; −12 V < V_{CANH} < +12 V;	0.4	0.8	1.15	V	NO IMPACT (Derived from internal reference)

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ELECTRICAL CHARACTERISTICS V_{CC} = 4.75 V to 5.25 V; V_{IO} = 2.8 V to 5.5 V (NCV7349−3 only); T_J = −40 to +150°C; R_{LT} = 60 Ω unless specified otherwise. On chip versions without V_{IO} pin, reference voltage for all digital inputs and outputs is V_{CC} instead of V_{IO}.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Impact of extended supply range of 4.5 V to 5.5 V on V_{CC} pin
BUS LINES (Pins CANH and CANL)							
$R_{i(cm)}$ (CANH)	Common−mode input resistance at pin CANH		15	26	37	kΩ	NO IMPACT
$R_{i(cm)}$ (CANL)	Common−mode input resistance at pin CANL		15	26	37	kΩ	NO IMPACT
$R_{i(cm)\ (m)}$	Matching between pin CANH and pin CANL common mode input resistance	$V_{CANH} = V_{CANL}$	−3	0	+3	%	NO IMPACT
$R_{i(dif)}$	Differential input resistance		25	50	75	kΩ	NO IMPACT
$C_{i(CANH)}$	Input capacitance at pin CANH	$V_{TxD} = V_{IO}$; (Note 1)	−	−	30	pF	NO IMPACT
$C_{i(CANL)}$	Input capacitance at pin CANL	$V_{TxD} = V_{IO}$; (Note 1)	−	−	30	pF	NO IMPACT
$C_{i(dif)}$	Differential input capacitance	$V_{TxD} = V_{IO}$; (Note 1)	−	3.75	10	pF	NO IMPACT
THERMAL SHUTDOWN							
$T_{J(sd)}$	Shutdown junction temperature	Junction temperature rising	150	170	185	°C	NO IMPACT
TIMING CHARACTERISTICS							
$t_{d(TxD-BUSon)}$	Delay TxD to bus active	C_i = 100 pF between CANH to CANL	−	50	−	ns	NA
$t_{d(TxD-BUSoff)}$	Delay TxD to bus inactive	C_i = 100 pF between CANH to CANL	−	60	−	ns	NA
$t_{d(BUSon-RxD)}$	Delay bus active to RxD	C_{RxD} = 15 pF	−	60	−	ns	NA
$t_{d(BUSoff-RxD)}$	Delay bus inactive to RxD	C_{RxD} = 15 pF	−	60	−	ns	NA
t_{pd}	Propagation delay TxD to RxD (NCV7349−0 version)	C_i = 100 pF between CANH to CANL	−	125	230 (255)	ns	NO IMPACT in range from 4.75V to 5.5V for max level. Design guranteed to stay within ISO11898−2 [2] for full extended voltage range from 4.5V. ISO limit in bracket.
	Propagation delay TxD to RxD (NCV7349−3 version)	C_i = 100 pF between CANH to CANL	−	130	250 (255)	ns	NO IMPACT in range from 4.75V to 5.5V for max level. Design guranteed to stay within ISO11898−2 [2] for full extended voltage range from 4.5V. ISO limit in bracket.
$t_{d(stb-nm)}$	Delay standby mode to normal mode		5	8	20	μs	Guaranteed by design. Covered by corner simulations. This parameter is not required by ISO11898−2.
t_{wake}	Dominant time for wake−up via bus		0.5	2.5	5	μs	Guaranteed by design. Covered by corner simulations.
$t_{dwakerd}$	Delay to flag wake event (recessive to dominant transitions)	Valid bus wake−up event, C_{RxD} = 15 pF	1	4.5	10	μs	Guaranteed by design. Covered by corner simulations. This parameter is not required by ISO11898−2.

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Impact of extended supply range of 4.5 V to 5.5 V on V_{CC} pin
TIMING CHARACTERISTICS							
$t_{dwakedr}$	Delay to flag wake event (dominant to recessive transitions)	Valid bus wake−up event, C_{RxD} = 15 pF	0.5	−	7	μs	Guaranteed by design. Covered by corner simulations. This parameter is not required by ISO11898−2.
$t_{wake(RxD)}$	Minimum pulse width on RxD	5 μs t_{WAKE}, C_{RxD} = 15 pF	0.5			μs	Guaranteed by design. Covered by corner simulations. This parameter is not required by ISO11898−2.
$t_{dom(TxD)}$	TxD dominant time for time−out	V_{TxD} = 0 V	1.2	2.6	4	ms	Guaranteed by design. Covered by corner simulations. This parameter is not required by ISO11898−2.

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Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Velio Certification

NCV7349 was tested for Velio compliance. This test was provided for 3 power supply options. VCC_min = 4.75 V, VCC_typ =5 V and VCC_max = 5.25 V.

In the table below is the summary of the results and assessment on supply range sensitivity.

NCV7349 VELIO EVALUATION SUMMARY

		Criteria			Results			Note
Section	**Subject**	**Min**	**Max**	**Unit**	**Vcc_min**	**Vcc_typ**	**Vcc_max**	
3.1	Output Differential Capacitance		30	pF	−	20,91	−	No VCC effect
3.2.1	**Transceiver Delay**							
3.2.1.1	Transmitter Delay (R>D)		140	ns	50,156	47,453	45,188	Negligible VCC effect
3.2.1.2	Transmitter Delay (D>R)		140	ns	57,109	56,219	55,734	Negligible VCC effect
3.2.1.3	Receiver Delay (R>D)		140	ns	74,078	72,078	70,609	Negligible VCC effect
3.2.1.4	Receiver Delay (D>R)		140	ns	72,500	70,891	70,000	Negligible VCC effect
3.3.1	**dV/dt characteristic**							
3.3.1.1	dV/dt characteristic (D>R), Ron		50	Ω	−	29,82	−	No VCC effect
3.3.1.1	dV/dt characteristic (D>R)	See graph			See graph			
3.3.1.2	dV/dt characteristic (R>D)	See graph			See graph			
3.3.2	R>D Distortion Delay		37	ns	10,779	11,170	11,685	Negligible VCC effect
3.3.3	D>R Distortion Delay		587	ns	146,33	145,154	144,7	Negligible VCC effect
3.4.1	**Static response of threshold voltage**							
3.4.1.1	V_Thresh dom−rec	No judgement			−	−	−	−
3.4.1.2	V_Thresh rec−dom	0,7	0,9	V	0.857/ 0.878	0.860/ 0.877	0.861/ 0.877	Negligible VCC effect
3.4.2	Frequency response of threshold voltage	See graph			See graph			Positive VCC effect − Lower VCC −> Higher margin
3.5.1	Single Ended S−Parameter |S11−S22|		0,03	−	−	Max 0.01	−	No VCC effect

Conclusion

NCV7349 can be safely used from 4.5 V to 5.5 V. Most of the parameters are guaranteed as stated in the datasheet. Few CAN parameters have small limitations versus NCV7349 datasheet [1] but still being in accordance with CAN ISO norm [1].

Velio testing performed on the device in the range of 4.75 V to 5.25 V is based on the analysis of the report well extendable to the range of 4.5 V to 5.25 V.

Referenced Documents

1. NCV7349 datasheet, December, 2014 − Rev. 1, www.onsemi.com
2. ISO11898−2, DRAFT international standard, ISO/TC 22/SC 31, 2015, 17th December

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