

NCP1631 Evaluation Board Manual

Performance of a 300 W, Wide Mains Interleaved PFC Driven by the NCP1631

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EVALUATION BOARD MANUAL

The NCP1631 is a dual phase Power Factor Correction (PFC) controller. It drives the two branches of our 300 W interleaved PFC in Frequency Clamped Critical Conduction Mode (FCCrM). Each phase operates in Critical Conduction Mode (CRM) at maximum output power, low line until the switching frequency reaches the frequency clamp where the phases enters into Discontinuous Conduction Mode (DCM). The phase-shift between the two branches is always 180° in all conditions.

To improve the efficiency at light load, a programmable frequency foldback circuit allows decreasing the switching frequency if needed.

Moreover, in order to build safe and robust PFC stages, the NCP1631 integrates various protections such as: overcurrent protection (OCP), output under and overvoltage protection, brown-out, inrush current detection

Evaluation Board (EVB) Specification

The board is designed to meet the following specifications:

- Input voltage range: 85 Vrms to 265 Vrms
- Output power: 300 W
- Output voltage: 390 V
- Full load efficiency at 115 Vrms: >96%
- Power factor at maximum load: > 0.9
- Maximum switching frequency of the PFC: 240 kHz, meaning 120 kHz per phase.

Description of the Board

The application note AND8407/D [1] describes how to calculate the component for each pin of the NCP1631, so for details on how the application is designed please refer to this document.

In the default EVB configuration, the controller must be powered by an external power supply. A minimum voltage of 13 V should be applied to allow the controller to start.

However, the NCP1631 has a very low startup current (below 100 μ A), so the Integrated Circuit (IC) can be powered using startup resistors connected to the bulk rail and an auto-supply circuit. Thus, on the demonstration board, there is also an optional charge-pump circuit formed by R47, C31, D2 and D19 and optional startup resistors (R5, R4, R3). These circuits are not connected, but if needed, the values of the component that should be used are shown on Figure 1.

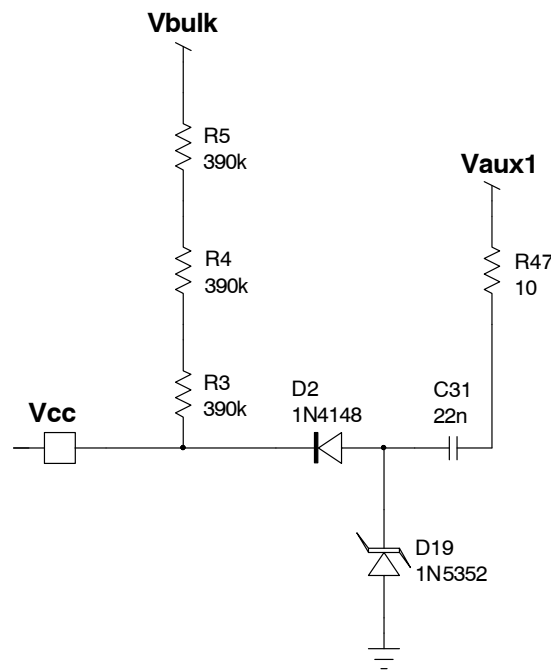


Figure 1. Optional Startup Circuit

The coils (150 μ H) are selected to have a minimum switching frequency of 80 kHz in critical conduction mode (CRM) at full load, low line.

NCP1631EVBD

Considering a maximum output power of 300 W, the input power can be as high as around 320 W (94% efficiency at lowest input voltage). Thus, in order to provide some margin, the input power capability is set 125% higher at 400 W.

The capacitor C15 connected to OSC pin (pin 4) is calculated to set the clamp frequency of the PFC stage to 240 kHz, meaning a maximum switching frequency of 120 kHz per phase. The resistor R34 placed in parallel of C15 fixes the minimum switching frequency per branch during frequency fold-back to 20 kHz.

The components around pin 5 are selected to provide a crossover frequency of 24 Hz for the PFC loop at maximum output power and a phase margin of 60°.

The frequency foldback resistor is calculated to allow the controller to start reducing the switching frequency when the output power drops below 42% of the maximum output power.

The brown-out resistors are chosen so that the circuit starts pulsing when the input voltage exceeds 82 Vrms and stops switching when the line goes below 72 Vrms.

The current limit is set to 8 A by resistors R24 and R1.

The NCP1631 also provides a latch pin: when the voltage on pin 10 exceeds 2.5 V, the controller shuts down and will be reset only by a brown-out condition or when the supply voltage of the IC drops below 5 V. We chose to implement an overvoltage protection for the IC supply voltage using this pin.

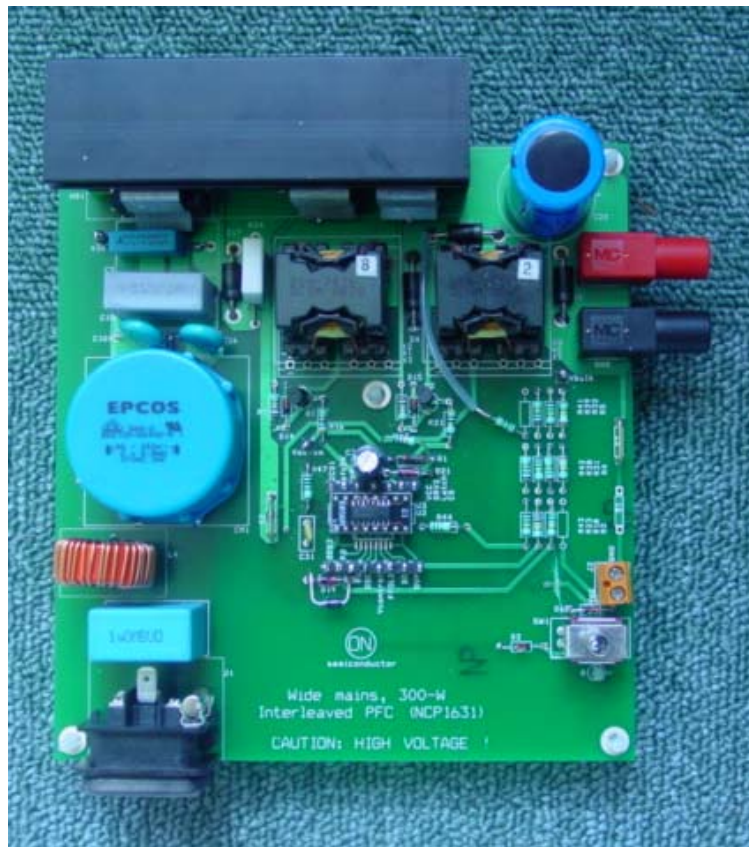


Figure 2. EVB Picture

NCP1631EVb/D

Board Schematic

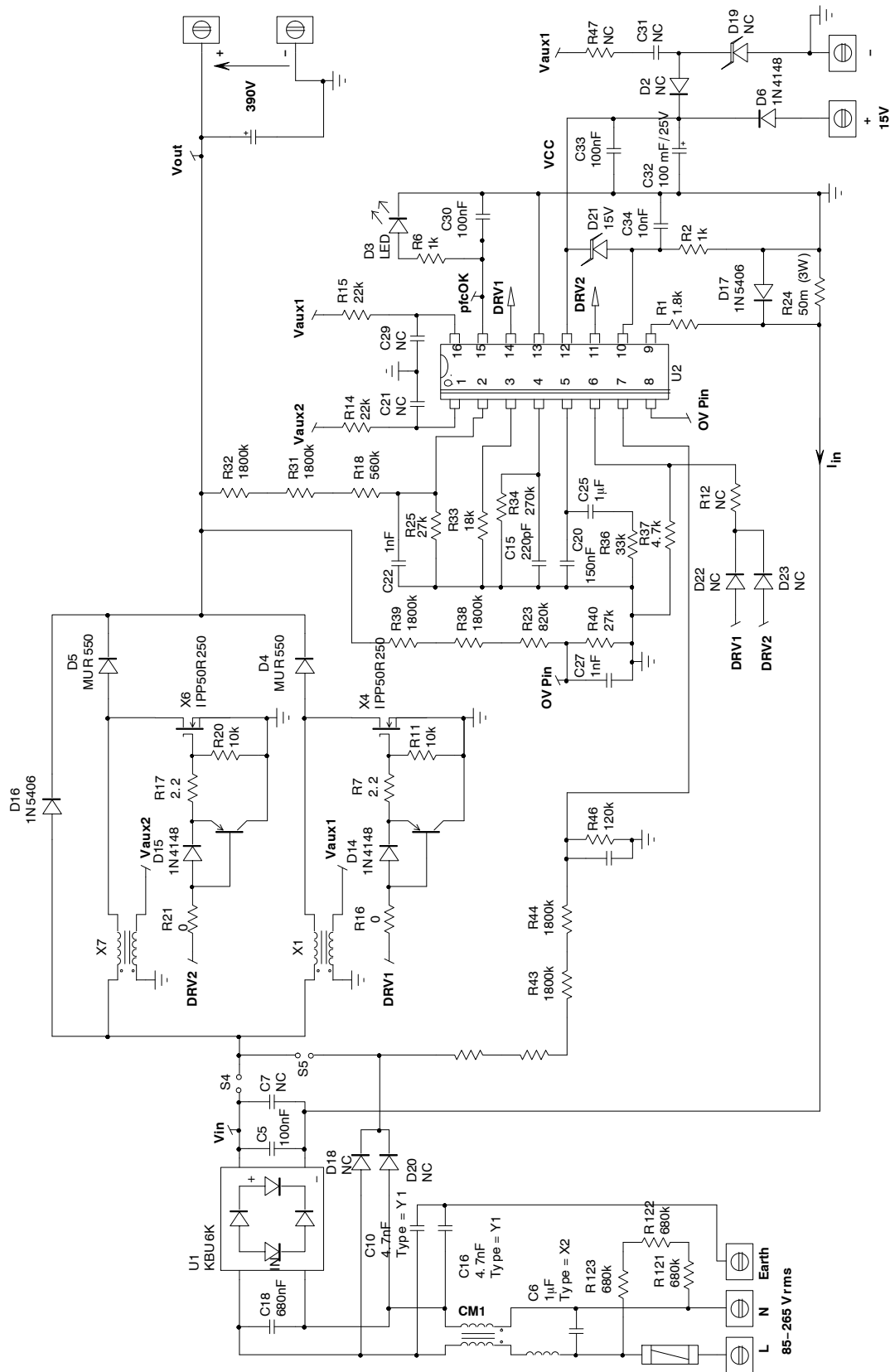


Figure 3. EVB Schematic

TYPICAL PERFORMANCE DATA

The measurements were made after the board was operating during 15mn at full load, low line, with an open frame, at ambient temperature and with no fan.

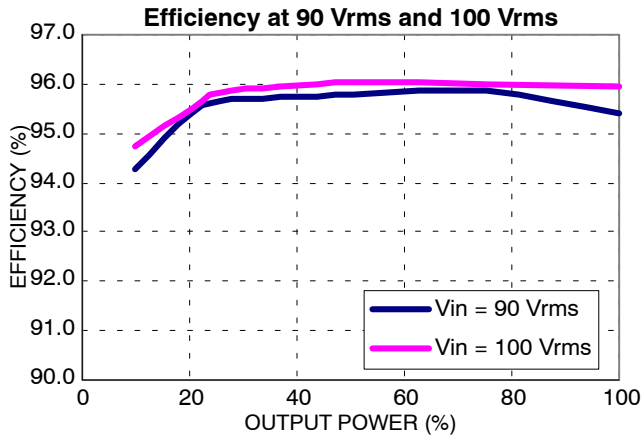


Figure 4. Efficiency at 90 Vrms and 100 Vrms

As shown by Figure 5, for the maximum output power, the efficiency is higher than 96% at 115 Vrms.

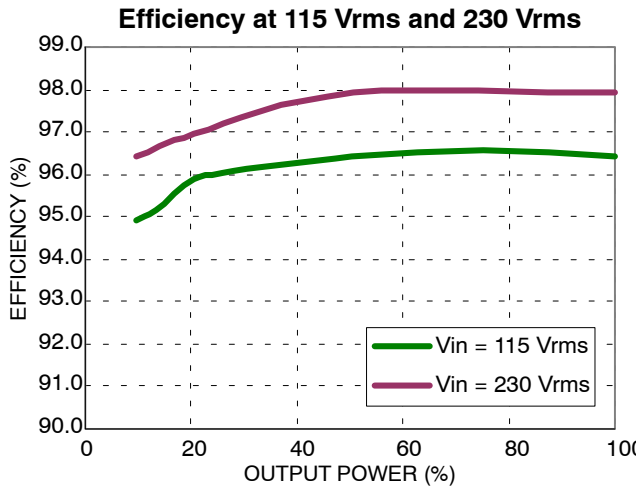


Figure 5. Efficiency at 115 Vrms and 230 Vrms

Due to the frequency clamp critical conduction mode, the efficiency is kept quite constant over the load range. Moreover, thanks to the frequency foldback, the efficiency at light load is very good.

The Total Harmonic Distortion (THD) remains very low over the output load range.

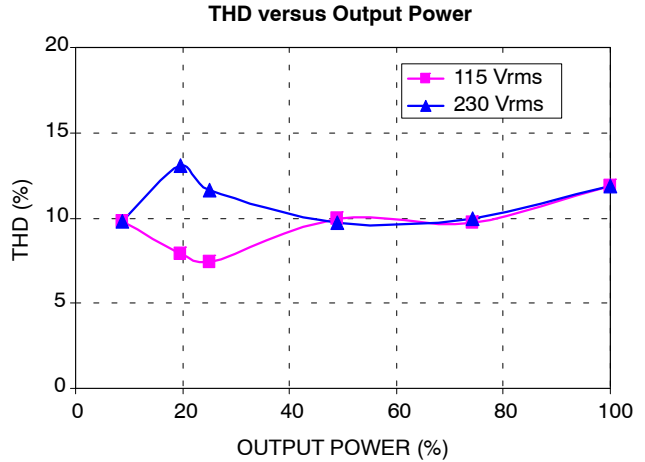


Figure 6. THD at 115 Vrms and 230 Vrms

The following table details the benefits of the frequency foldback. We measured the efficiency of our 300-W demoboard at 20% and 10% of the maximum output power with no frequency foldback ($R_{FF} = 0$), with the frequency foldback starting at 25% of the maximum output power, and with the frequency foldback starting at 50% of the maximum output power. The measurements showed that the frequency foldback allows increasing the efficiency by more than 2% at 20% of $P_{out,max}$ and 4% at 10% of $P_{out,max}$!

Table 1. EFFICIENCY AT LIGHT LOAD FOR DIFFERENT FREQUENCY FOLDBACK SETTINGS

	V _{in} (Vrms)	P _{out} (% of P _{out,max})	Efficiency (%)	F _{sw} (kHz)
R _{FF} = 0	115	20	93.3	122
	115	10	90.3	122
	230	20	94.6	122
	230	10	91.0	122
R _{FF} = 2.5 kΩ	115	20	93.8	114
	115	10	91.9	65
	230	20	94.9	95
	230	10	93.0	54
R _{FF} = 4.7 kΩ	115	20	95.9	67
	115	10	94.9	43
	230	20	96.9	63
	230	10	96.4	38

The following graph (Figure 7) illustrates the FCCrM operation.

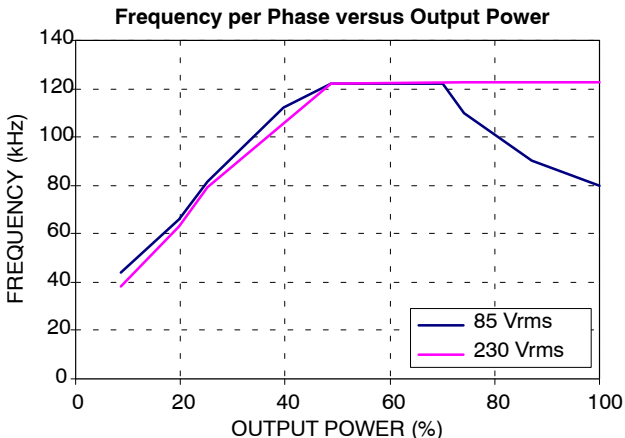


Figure 7. Switching Frequency per Phase versus Output Power at 85 Vrms and 230 Vrms

At low line and maximum output power, the PFC branches operates in CRM until the switching frequency reaches the frequency clamp (120 kHz per phase) around 70% of P_{out,max}. The controller then drives the phases in fixed frequency DCM until the frequency foldback circuit starts to reduce the frequency.

Typical Waveforms

Figure 8 and Figure 9 portray the input voltage, input current (*I_{line}*) and the sum of the inductors current (*I_{L(tot)}*) at full load, low line and high line.

Figure 10 and Figure 11 are zooms of the previous plots obtained at the sinusoid top.

As expected, the input current has the shape of a CCM current.

At low line and high line, the phase shift is well controlled and is 180°.

Each branch operates in CRM at low line and in DCM fixed frequency at high line.

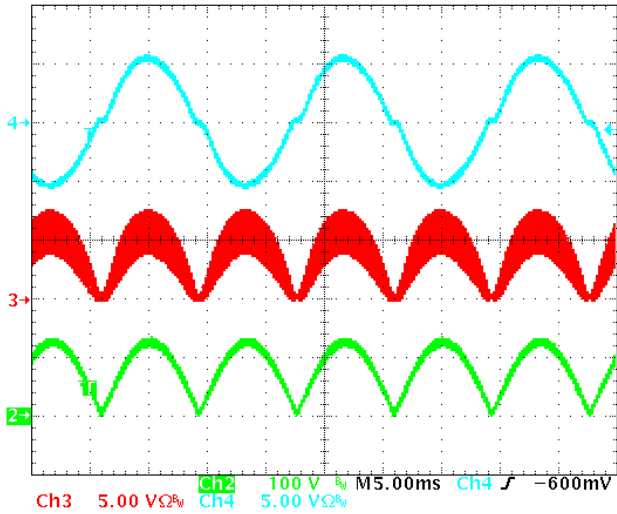


Figure 8. Input Voltage and Current at 90 Vrms

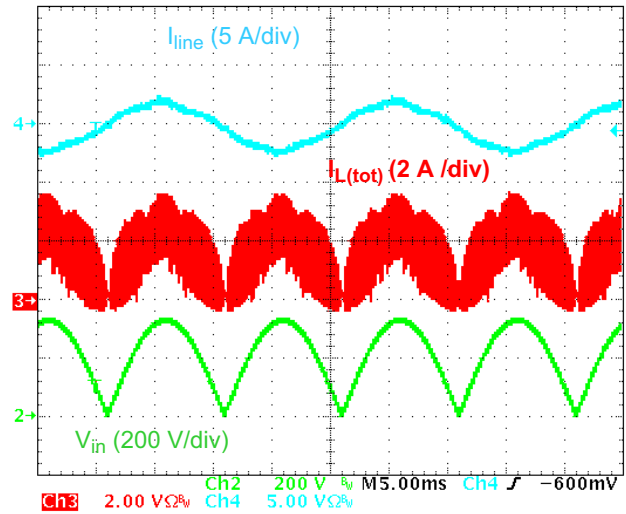


Figure 9. Input Voltage and Current at 230 Vrms

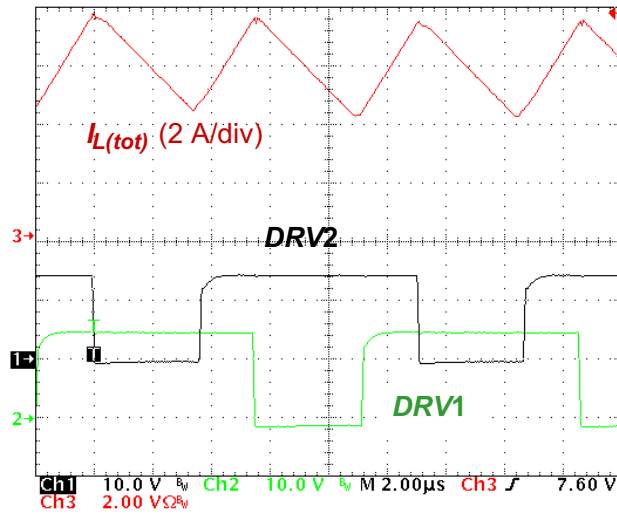


Figure 10. Inductors Current, DRV1 and DRV2 at 90 Vrms

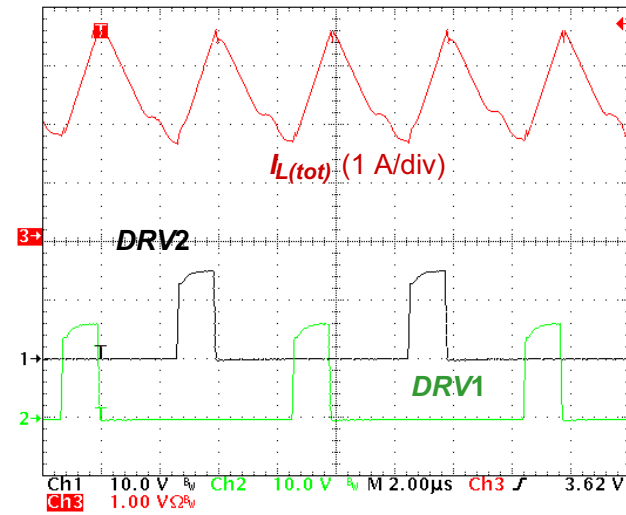


Figure 11. Inductors Current, DRV1 and DRV2 at 230 Vrms

Brown-Out Protection

In order to pass line cycle drop out test, the brown-out circuit integrates a timer that blanks the brown-out pin voltage (V_{BO}) during 50 ms typically (the minimum value being 25 ms). When V_{BO} goes below the 1-V threshold the brown-out circuit maintains a level close to the 1-V threshold on the pin in order to allow the PFC to restart at full power. Thus, no fault is detected and the pfcOK signal stays high as shown by Figure 12.

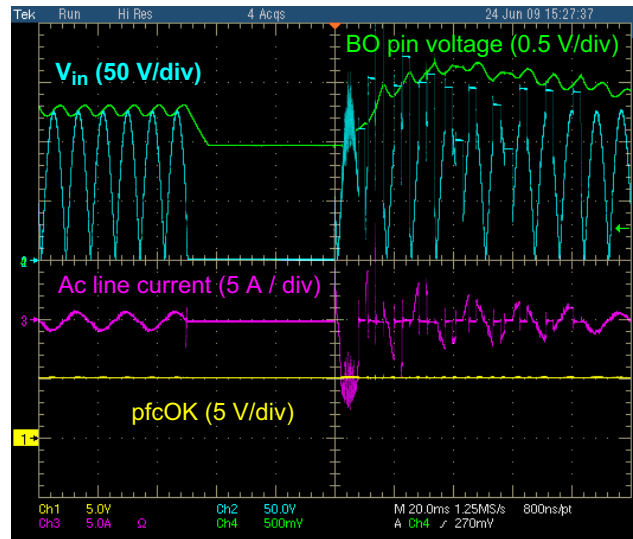


Figure 12. 40-ms Mains Interruption

Line and Load Transient

Figure 13 shows the line transient response of the interleaved PFC. The line voltage is changed abruptly from 115 V_{rms} to 230 V_{rms} and we observe that the overshoot and the undershoot are kept small by the controller.

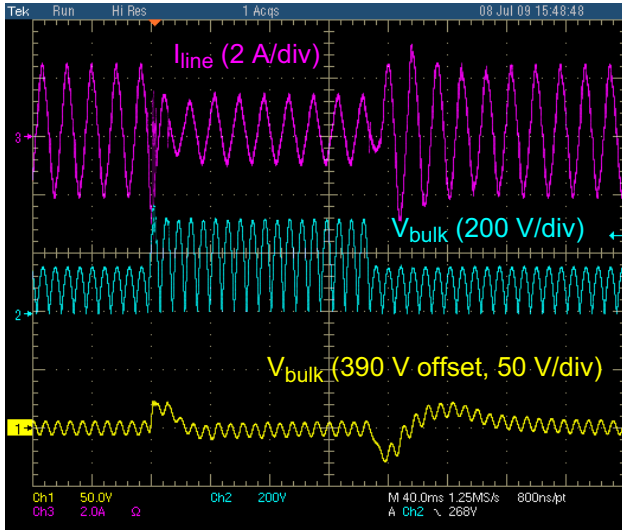


Figure 13. Line Transient at half the output load

Figure 14 and Figure 15 show an output transient load step from 20% to 100% of the maximum output power at low line and high line. The slew rate is 2 A/μs. The overshoots are contained by the programmable over voltage protection which is set to 410 V in this application.

The undershoots are limited by the boost of the error amplifier which increases its gain when the bulk voltage goes below 95.5% of its nominal value.

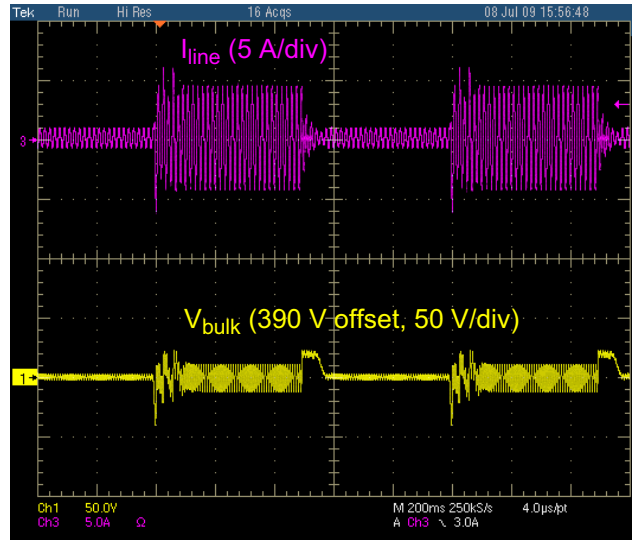


Figure 14. Transient Load Response at 115 Vrms (from 20% to 100% of P_{out,max})

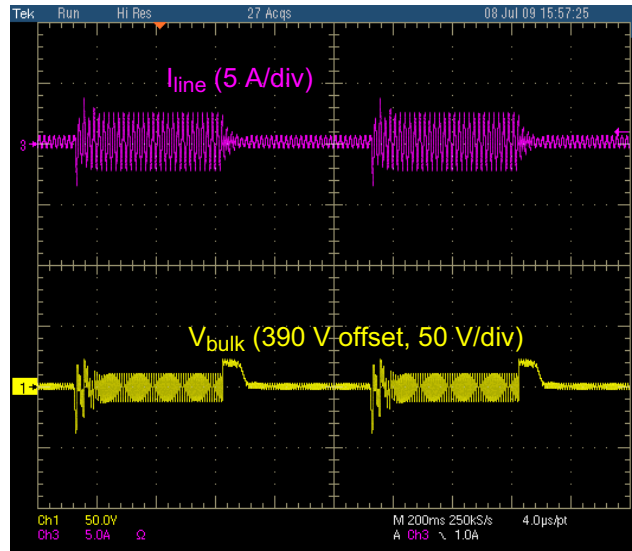


Figure 15. Transient load response at 230 Vrms (from 20% to 100% of P_{out,max})

NCP1631EV B/D

BILL OF MATERIALS

Reference	Qty	Value	Description	Manufacturer	Part number
CM1	1		CM Filter, 4 A, 2 * 6.8 mH	EPCOS	B82725
C2	1	100 μ	Electrolytic capacitor, 450 V	Standard	Standard
C5	1	100n	X2 capacitor, 275 V	RIFA	PHE840MF6680M
C6	1	1u	X2 capacitor, 275 V	RIFA	PHE840MF6680M
C10x,C16	2	4.7n	Y capacitor, 275 V	Murata	DE1E3KX472MA5B
C15	1	220p	Ceramic capacitor, SMD, 1206, 50 V	Standard	Standard
C18	1	680n	X2 capacitor, 275 V	Murata	DE1E3KX472MA5B
C20	1	150n	Ceramic capacitor, SMD, 1206, 50 V	Standard	Standard
C22,C27	2	1n	Ceramic capacitor, SMD, 1206, 50 V	Standard	Standard
C25	1	1u	Ceramic capacitor, SMD, 1206, 50 V	Standard	Standard
C28	1	220n	Ceramic capacitor, SMD, 1206, 50 V	Standard	Standard
C30,C33	2	100n	Ceramic capacitor, SMD, 1206, 50 V	Standard	Standard
C31	1	22n	Ceramic capacitor, SMD, 1206, 50 V	Standard	Standard
C32	1	100 μ F	Electrolytic capacitor, 25 V	Standard	Standard
C34	1	10n	Ceramic capacitor, SMD, 1206, 50 V	Standard	Standard
D1,D2,D6, D14,D15, D22,D23	7	D1N4148	Diode	Philips	1N4148
D3	1	LED	LED 100 D		
D4,D5	2	MUR550	DIODE, 5A, 500 V, AXIAL	ON Semi	MUR550APFG
D16,D17	2	1N5406	Standard recovery diode, 600 V	ON Semi	1N5406G
D19, D21	1		Zener diode, 15 V	Standard	Standard
HS1	1		Heatsink, 2.9°C/W	Aavid Thermalloy	437479
L4	1	150 μ H	DM Choke, 5 A, WI-FI series	Würth Electronics	
Q1,Q2	2	2N2907	PNP transistor, TO92	ON Semiconductor	P2N2907AG
R1,R2	2	1k	Axial resistor, 1/4 W	Standard	Standard
R1	1	1.8k	Axial resistor, 1/4 W	Standard	Standard
R2,R6	2	1k	SMD resistor, 1206, 1/4W	Standard	Standard
R3,R4, R5,R44	4	390k	Axial resistor, 1/4 W	Standard	Standard
R7,R17	2	2.2	Axial resistor, 1/4 W	Standard	Standard
R11, R12,R20	3	10k	SMD resistor, 1206, 1/4 W	Standard	Standard
R14,R15	2	22k	SMD resistor, 1206, 1/4 W	Standard	Standard
R16,R21	2	47	Axial resistor, 1/4 W	Standard	Standard
R18	1	560k	Axial resistor, 1/4 W	Standard	Standard
R23	1	820k	Axial resistor, 1/4 W	Standard	Standard
R24	1	50m	Axial resistor, 3 W, \pm 1%	Vishay	RLP3 0R050
R25,R40	2	27k	SMD resistor, 1206, 1/4 W	Standard	Standard
R31,R32,R38, R39,R41,R42, R43	7	1800k	Axial resistor, 1/4 W	Standard	Standard
R33	1	13k	SMD resistor, 1206, 1/4 W	Standard	Standard
R34	1	270k	SMD resistor, 1206, 1/4 W	Standard	Standard

NCP1631EV/D

BILL OF MATERIALS

Reference	Qty	Value	Description	Manufacturer	Part number
R36	1	33k	SMD resistor, 1206, 1/4 W	Standard	Standard
R37	1	4.7k	SMD resistor, 1206, 1/4 W	Standard	Standard
R45	1	0	SMD resistor, 1206, 1/4 W	Standard	Standard
R46	1	82k	SMD resistor, 1206, 1/4 W	Standard	Standard
R47	1	10	Axial resistor, 1/4 W	Standard	Standard
R121,R122, R123	3	680k	SMD resistor, 1206, 1/4 W	Standard	Standard
U1	1	KBU6K	Diode Bridge	General Semiconductor	KBU6K
U2	1	NCP1631	Interleaved PFC controller, SOIC-16	ON Semiconductor	NCP1631
X1,X5	2	150 μ H	PFC coil	Delta CME	86H-7416 OF9120
X4,X6	2	IPP50R250	MOSFET, 13 A, 500 V	Infineon	IPP50R250CP

Conclusion


This application note has described the results obtained with a 300 W Interleaved PFC stage.

It is possible to achieve efficiency higher than 96% at 115 V_{rms} with the NCP1631.

Due to the FCCrM and the frequency foldback, the efficiency is improved over a wide load range (from 100% down to 10% of the maximum output power).

References

[1] Joel Turchi, "Key steps to design an interleaved PFC stage driven by the NCP1631", Application Note AND8407/D, www.onsemi.com

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