Test Procedure for the NCN4555GEVB

ON Semiconductor®

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Table 1: Required Equipment

Description	Main Features	Example of Equipment (1)	Qty.
Regulated Power Supply	200 mA DC current capability	Tektronix PS2520G	2
Multimeter		Keitley 2000 or 2001	2
Sourcemeter		Keitley 2400	1
Oscilloscope	500 MHz Bandwidth, four channel scope, min 1Mbit memory per channel (2)	Tektronix TDS744, 754 or 784 / TDS5054 series or Lecroy WR5060	1
Voltage probe	4 probes 500 MHz Bandwidth	Tektronix or Lecroy	4
Waveform generator	10 MHz, CMOS logic signals	Agilent 81104A 80 MHz or HP8110A 150 MHz 2 outputs	1
SMB Cable		External Clock Input	1

1. Equipment used in this test procedure.
2. Scope memory per channel is relevant because it offers better resolution. The scopes voltage probe should have a picofarad rating of between 11 and 30 pF.

Test Procedure:
All the positions of switches given below refer strictly to the logical positions (High or Low) indicated Figure 1.

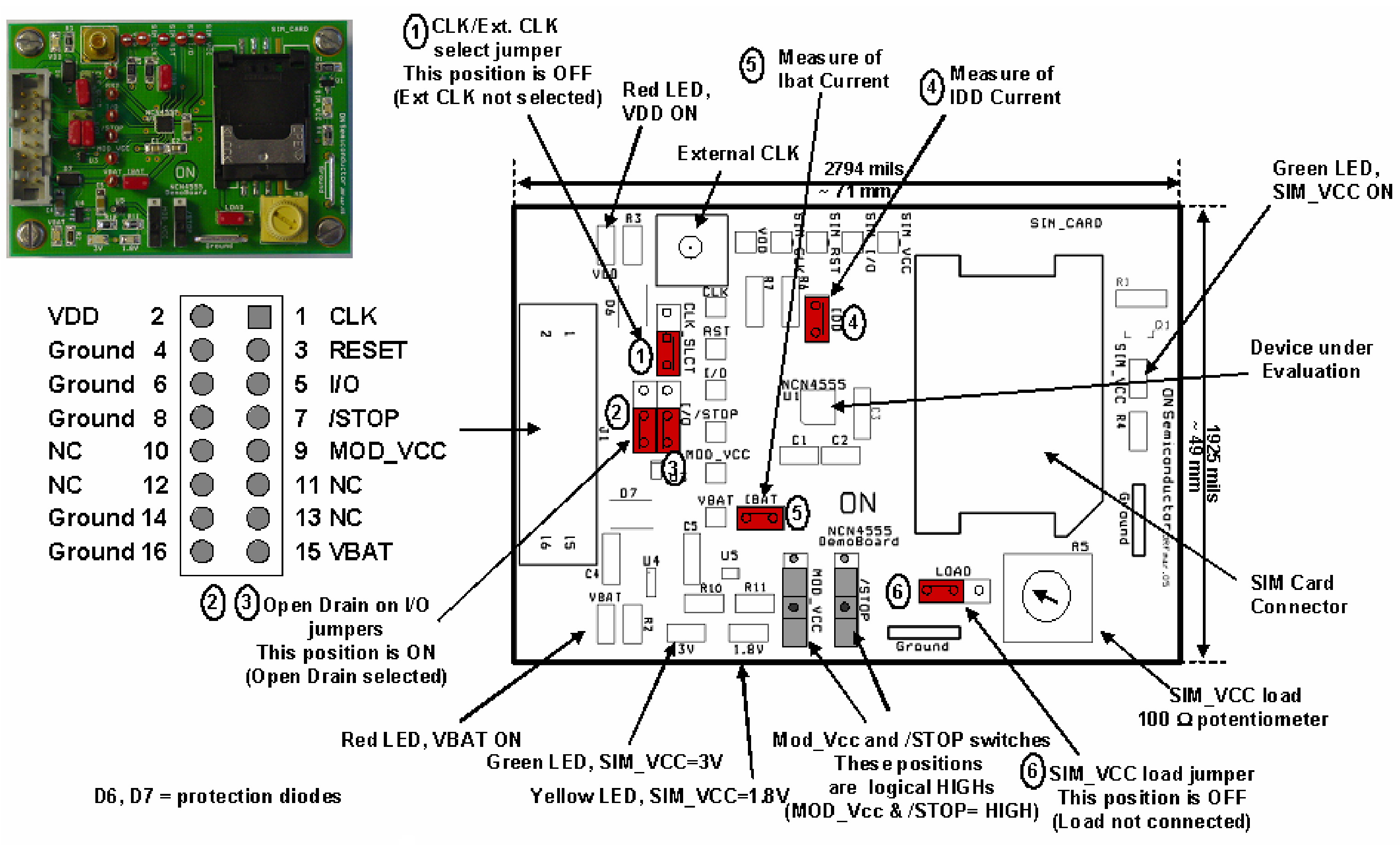


Figure 1 : NCN4555 Evaluation Board Details

1. Setup NCN4555GEVB as follows (Figure 1):
- Turn-off the /STOP switch (position LOW).
- Set the MOD_VCC switch also in a position LOW (SIM_VCC = 1.8V).
- As a precaution, turn the 100 Ω potentiometer button fully to the right. The resistor output value is 100 Ω in this case.
- Jumpers:

  Jumper 1: as shown in Figure 1, internal clock selected (through HE10 connector).
  Jumpers 2 and 3: Jumpers in off position contrary to Figure 1 where the position is on. The Open Drain will then be unconnected and the I/O signal will be applied directly to the I/O NCN4555 input through the HE10 connector.
  Jumper 4: plugged as in Figure 1.
  Jumper 5: plugged as in Figure 1.
  Jumper 6: 100 Ω potentiometer not connected, as in Figure 1.

2. Connect DC power supplies:

Two power supplies are used to bias the demo board. V_{BAT} is the input voltage of the DC/DC converter; V_{DD} is the “digital” power supply which biases the input stages of the NCN4555 device (control and signal inputs). V_{DD} and V_{BAT} must be connected to the board for correct operation.
- Connect the ground of the V_{DD} & V_{BAT} power supplies to the ground of the board (2 GND jumpers are available on the board)
- Connect the V_{DD} power supply using the HE10 connector or the V_{DD} test point.
- Connect the V_{BAT} power supply through the HE10 connector or using the V_{BAT} test point.
- **Warning:** If V_{DD} and V_{BAT} are applied through the HE10 connector the operating power supply voltages must be checked at the test points because of the voltage drops (~ 0.6 V / 0.7 V) introduced by the protection diodes D6 and D7.
- Power up V_{DD} in the range 1.8 V – 5.5 V. The corresponding red LED light should be on.
- Power up V_{BAT} in the range 2.7 V – 5.5 V. The corresponding red LED light should be on.
- The MOD_V_{CC} switch selects CRD-V_{CC} 1.8 V or 3.0 V. When CRD_V_{CC} delivers 1.8 V the yellow LED is turned on and the MOD_V_{CC} switch is in the logical position LOW. When CRD_V_{CC} provides 3 V the green LED is turned on and the MOD_V_{CC} switch is HIGH.

- By using the /STOP switch you select either the operating mode or the shutdown mode. In this last case, the SIM_V_{CC} voltage being null, the SIM_V_{CC} green LED is off.

3. Power Supply Section Evaluation:

With this evaluation board the following measurements can be made (see NCN4555 datasheet):

1. Operating and shutdown currents both on V_{DD} and V_{BAT}. See Figures 2 and 3
2. Under voltage Lockout (V_{DD})
3. Short Circuit Current ($I_{SIM\_VCC\_SC}$)
4. Max I_{SIM_VCC} current. (Figure 4)
5. dc/dc Converter Turn-on and Turn-off times (Figures 6-9)

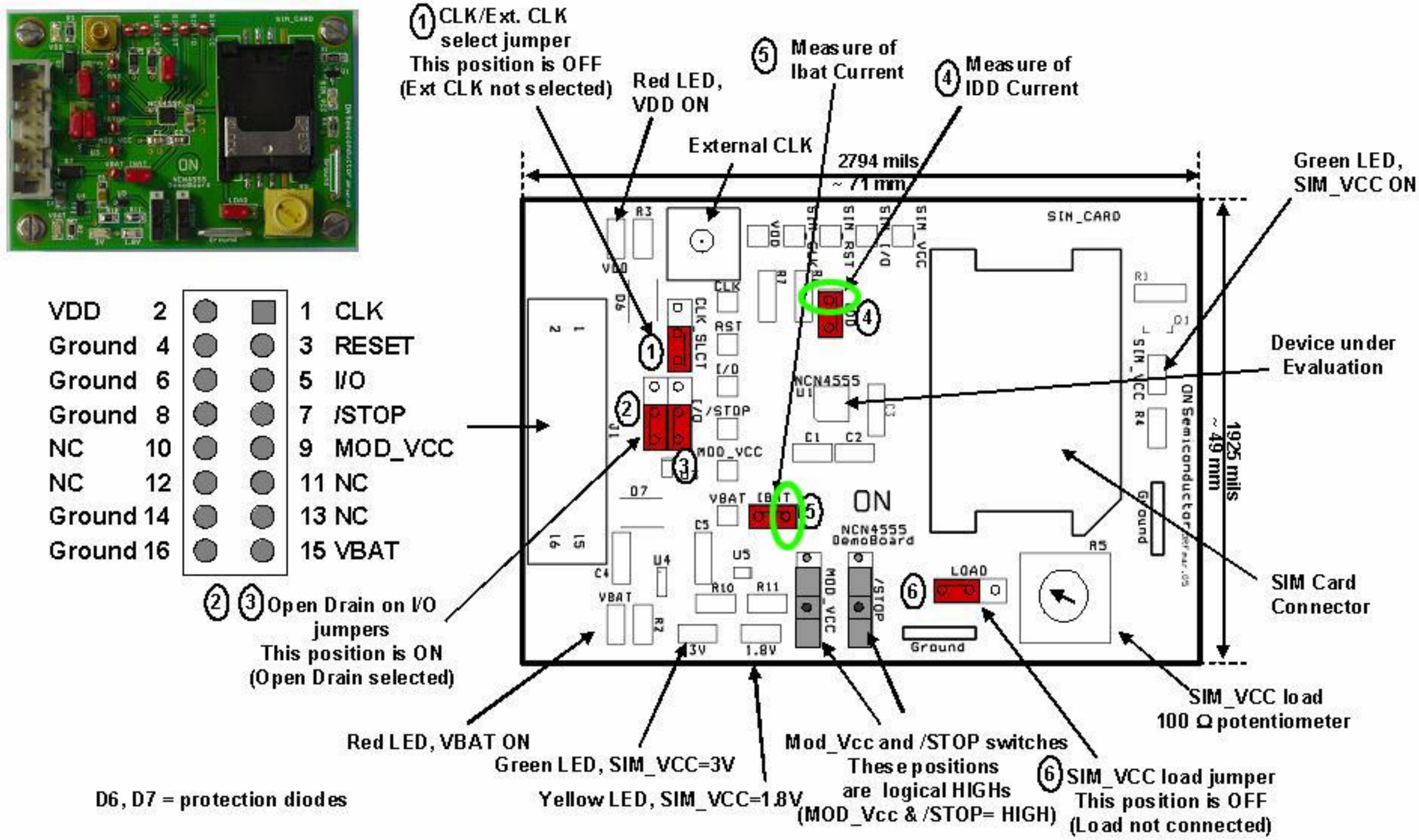
Measurement implementation:

- The evaluation board is powered up at the V_{BAT} and V_{DD} voltages specified by the application.
- The switch /STOP is in position HIGH (operating mode)
- The switch MOD_V_{CC} is fixed according to the value required by the application
- **Connect CLK and RST inputs to GND in order to avoid floating nodes.**
- Connect the oscilloscope probe and the voltmeter as follow:

Analog ground (voltmeter and scope)	→	Demo board's GROUND jumper.
Channel 1: 1MΩ and voltmeter	→	Test point SIM_V_{CC} (Smart card operating voltage).

- Connect the amp meter using jumpers 4 and 5 to measure I_{DD} and I_{BAT}.

- Using the SIM_V_{CC} load jumper the user can connect the SIM_V_{CC} output to a 100 Ω potentiometer and pull up the nominal I_{SIM_VCC} current to 50 mA. See figure on next page for current meter connection points. This potentiometer can also be used to measure the I_{SIM_VCC} Short Circuit and maximum allowable currents. See Figure 4.



NCN4555 Evaluation Board

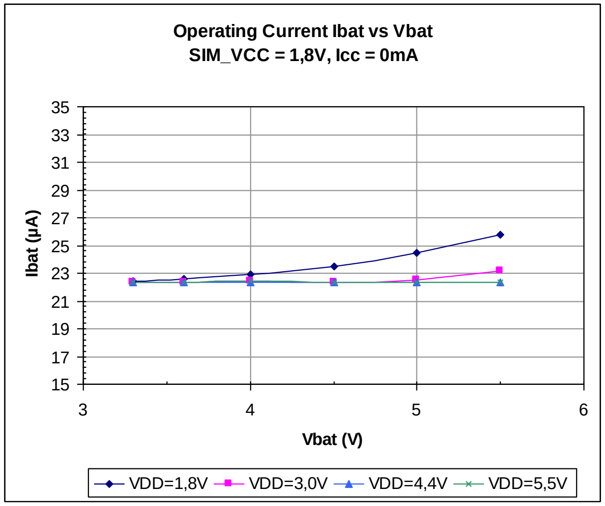


Figure 2: Typical Operating Current Ibat vs. V_{BAT} / SIM_V_{CC} = 3 V, I_{CC} = 0 mA & Temp = 25°C

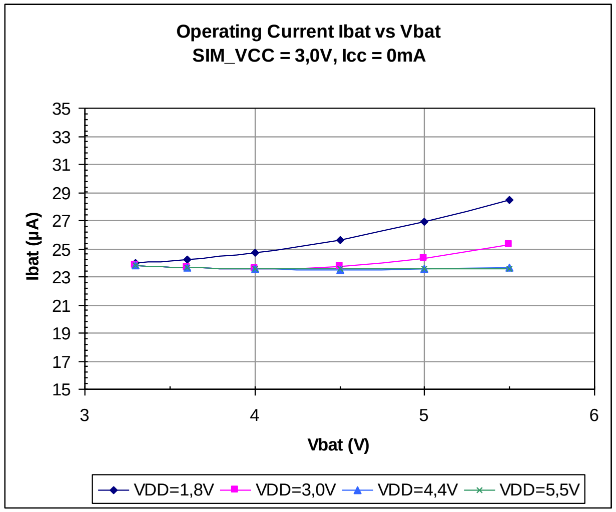


Figure 3: Typical Operating Current Ibat vs. V_{BAT} / SIM_V_{CC} = 3 V, I_{CC}= 0 mA & Temp = 25°C

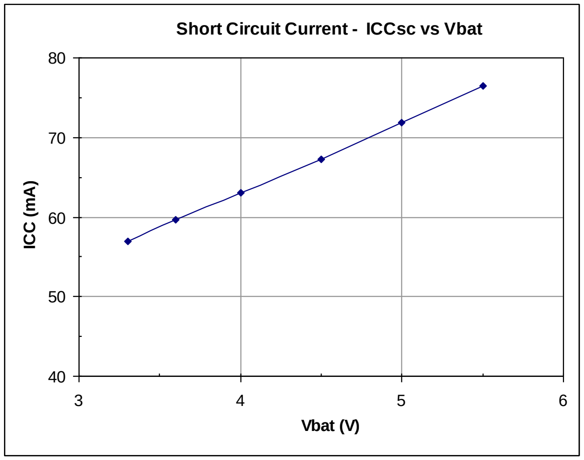


Figure 4: Short-Circuit Current / SIM_V_{CC} = 3 V (idem with 1.8 V), Temp = 25°C

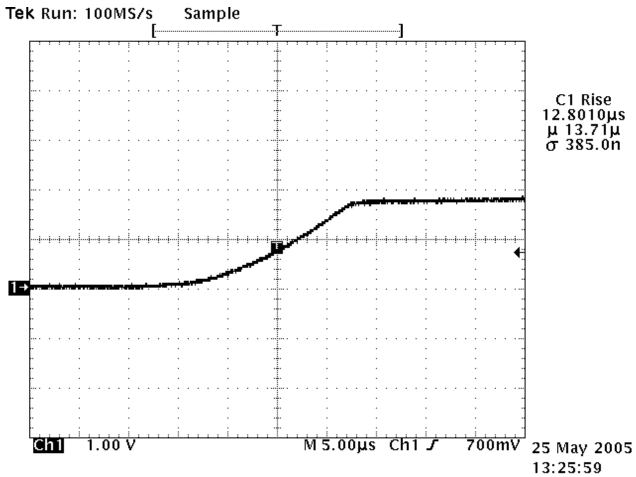


Figure 5: LDO's Turn-on time / SIM_V_{CC} = 1.8 V, V_{DD} = 1.8 V, V_{BAT} = 5.5 V & Temp = 25°C

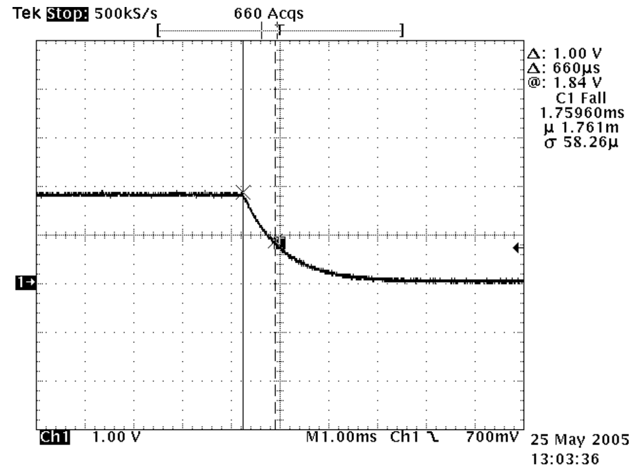


Figure 6: LDO's Turn-off time to 1 V / SIM_V_{CC} = 1.8 V, V_{DD} = 1.8 V, V_{BAT} = 5.5 V & Temp = 25°C

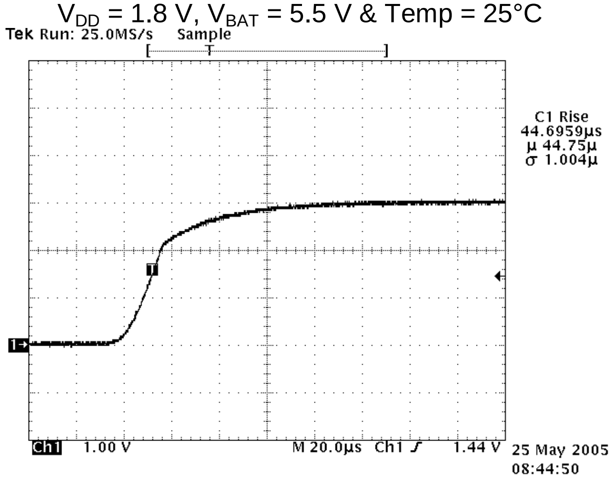


Figure 7: LDO's Turn-on time / SIM_V_{CC} = 3.0 V, V_{DD} = 1.8 V, V_{BAT} = 5.5 V & Temp = 25°C

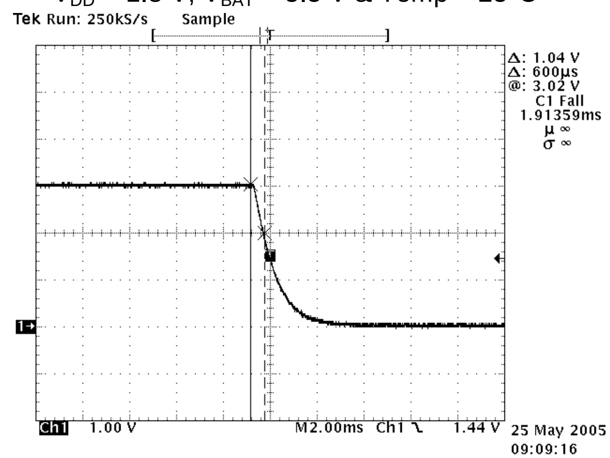


Figure 8: LDO's Turn-off time to 1V / SIM_V_{CC} = 3.0 V, V_{DD} = 1.8 V, V_{BAT} = 5.5 V & Temp = 25°C

4. Level Shifter Test:

Considering the level shifter function with this evaluation board the following measurements can be made.

1. Signal rise and fall times
2. Signal levels High and Low
3. Clock duty cycle
4. Frequency performance

Measurement implementation:

- The evaluation board is powered up at VBAT and VDD voltages specified by the application.
- The switch /STOP is in position HIGH (operating mode).
- The switch MOD_Vcc is fixed according to the value required by the application.

SIM_CLK signal:

- CLK and SIM_CLK are clock signals (Figures 9 and 10).
- **Connect the RST input to the Ground or to VDD in order to avoid floating nodes.**
- To evaluate SIM_CLK a clock signal has to be connected either using the external clock input (SMB connector) or through the HE10 connector. The selection is done using the corresponding jumper (See Figure 1). The max clock frequency will be 5 MHz and the signal will have to accommodate the specifications provided in the datasheet; the clock signal is a 50% duty cycle square wave with a peak to peak of 3.3 V and an offset of 1.65 V (this will be the clock input used for all measurements). Note the rise and fall times for SIM_CLK; they should be < 18 ns.

SIM_RST signal:

- RST and SIM_RST are Boolean-like signals (Figures 11 and 12).
- **Connect the CLK input to the Ground or to VDD in order to avoid floating nodes.**
- To evaluate SIM_RST, a RST signal accommodating the datasheet specifications will be applied either using the HE10 connector or through the corresponding test point.

SIM_I/O signal:

- I/O and SIM_I/O are data signals (Figures 13 and 14).

- To evaluate SIM_I/O, an I/O signal accommodating the datasheet specifications will be applied directly to the NCN4555 I/O device input (using either the HE10 connector or the corresponding test point and placing jumpers 2 and 3 in OFF position) or through the open drain circuit (using the pin third down on the right on the HE10 connector only and placing the I/O jumper in ON position). Typically 9600 bauds data are used through the I/O – SIM_I/O bidirectional channel. The open drain condition on the input corresponds to a worst-case situation regarding the rise and fall times and frequency performance.

For the three different signals, connect the oscilloscope probes as follow, these signals can be considered independently (in that case be careful with the floating nodes) or together. SIM_VCC will be connected to the oscilloscope's channel 1.

- Analog ground → GROUND jumper on the demo board.
- Channel 2, Channel 3, Channel 4: 1 MΩ → Corresponding Test points

Switch MOD_VCC to obtain alternatively 1.8 V CMOS logic levels or 3 V CMOS logic levels on SIM_I/O, SIM_CLK and SIM_RST.

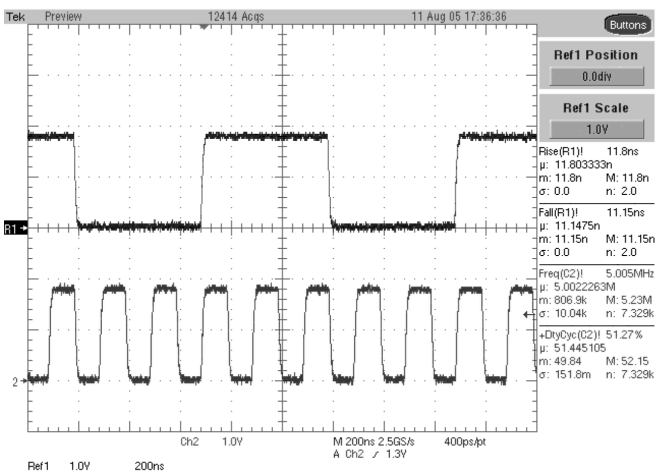


Figure 9: SIM_CLK waveforms at 1 MHz (Top) and 5 MHz (Bottom) / SIM_V_{CC} = 1.8 V & C_{OUT} > 33 pF

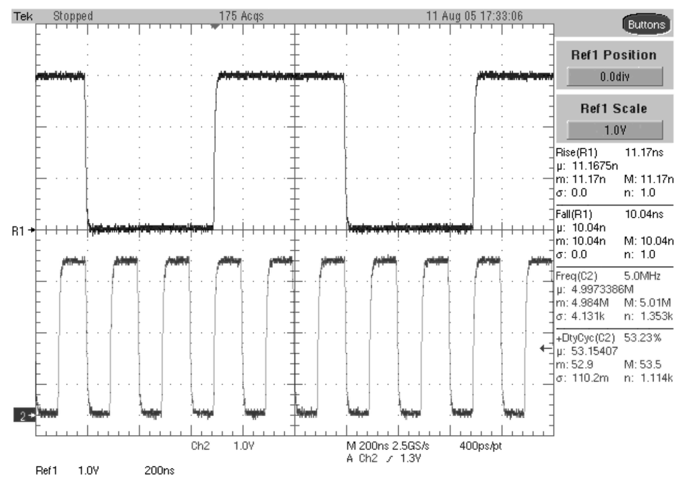


Figure 10: SIM_CLK waveforms at 1 MHz (Top) and 5 MHz (Bottom) / SIM_V_{CC} = 3.0 V & C_{OUT} > 33 pF

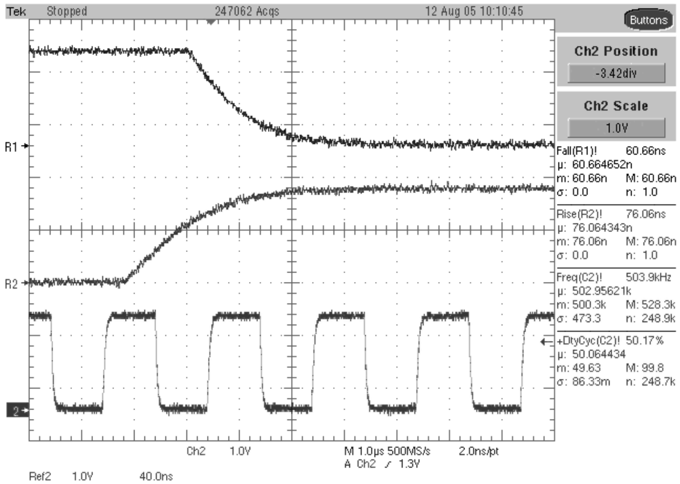


Figure 11: SIM_RST waveforms / SIM_V_{CC} = 1.8 V & C_{OUT} > 33 pF

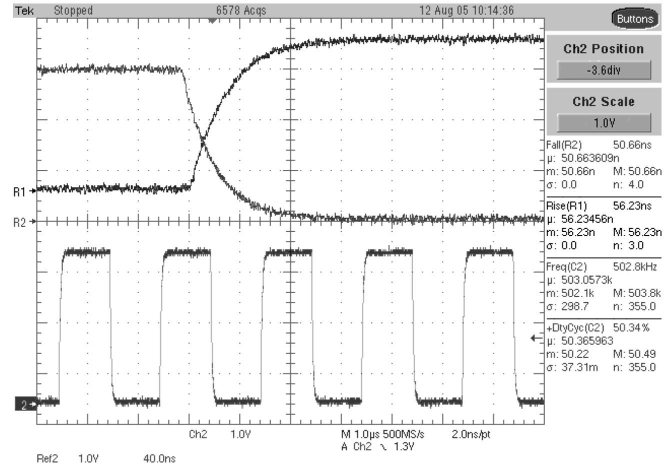


Figure 12: SIM_RST waveforms / SIM_V_{CC} = 3.0 V & C_{OUT} > 33 pF

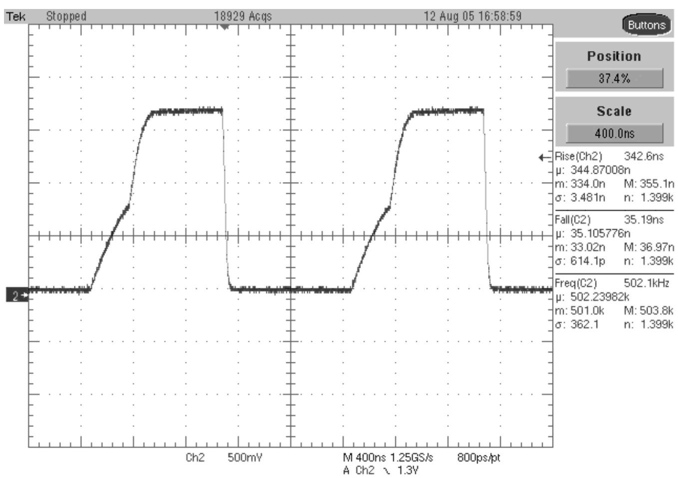


Figure 13: SIM_I/O waveforms / on-board Open-Drain configuration, SIM_V_{CC} =1.8 V & C_{OUT} > 33 pF

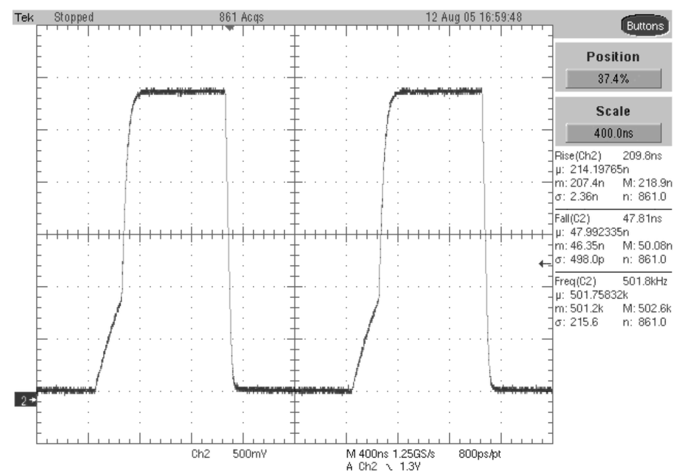


Figure 14: SIM_I/O waveforms / on-board Open-Drain configuration, SIM_V_{CC} =3 V & C_{OUT} > 33 pF